DATA HANDBOOK

Video and associated systems Bipolar, MOS

Types TDA1525 to μA733C

BOOK IC02b 1989

Philips Components

PHILIPS

VIDEO AND ASSOCIATED SYSTEMS
BIPOLAR, MOS

Part A

Part b

SELECTION GUIDE

FUNCTIONAL INDEX

NUMERICAL INDEX

MAINTENANCE TYPE LIST

The types listed below are not included in this handbook. Detailed information will be supplied on request.

SAA1056P	PLL frequency synthesizer
SAA1082	remote transmitter
SAA3027	infrared remote control transmitter
SAA5030	teletext video processor
SAB1164	1 GHz divide-by-64 prescaler
SAB1165	1 GHz divide-by-64 prescaler
SAB1256	1 GHz divide-by-256 prescaler (successor SAB6456)
SAF3019	clock/timer with serial I/O; microcontrolled
TDA2502	tacho motor speed controller
TDA2503	track sensing amplifier for VCR
TDA3540;Q	IF amplifier and demodulator; npn tuners
TDA3541;Q	IF amplifier and demodulator; pnp tuners
TDA3571B	sync combination with transmitter identification
TDA3576B	sync combination with transmitter identification
TDA3590	SECAM processor circuit (successor TDA3590A)
TDA3591	SECAM processor circuit (successor TDA3591A)
TDA3650	vertical deflection circuit
TDA3701	PAL sync processor for VCR
TDA3710	chrominance signal/mixer for VCR
TDA3720	SECAM processor for VCR (successor TDA3725)
TEA1002	PAL colour encoder and video summer (successor TEA2000)

DEVICE DATA

STEREO TONE/VOLUME CONTROL CIRCUIT

GENERAL DESCRIPTION

The TDA1525 is an active stereo tone/volume control for car radios, television receivers and mains-fed audio equipment. It includes functions for bass and treble control, volume control with built-in contour (can be switched off) and balance. All these functions can be controlled by DC voltages or by single linear potentiometers.

Features

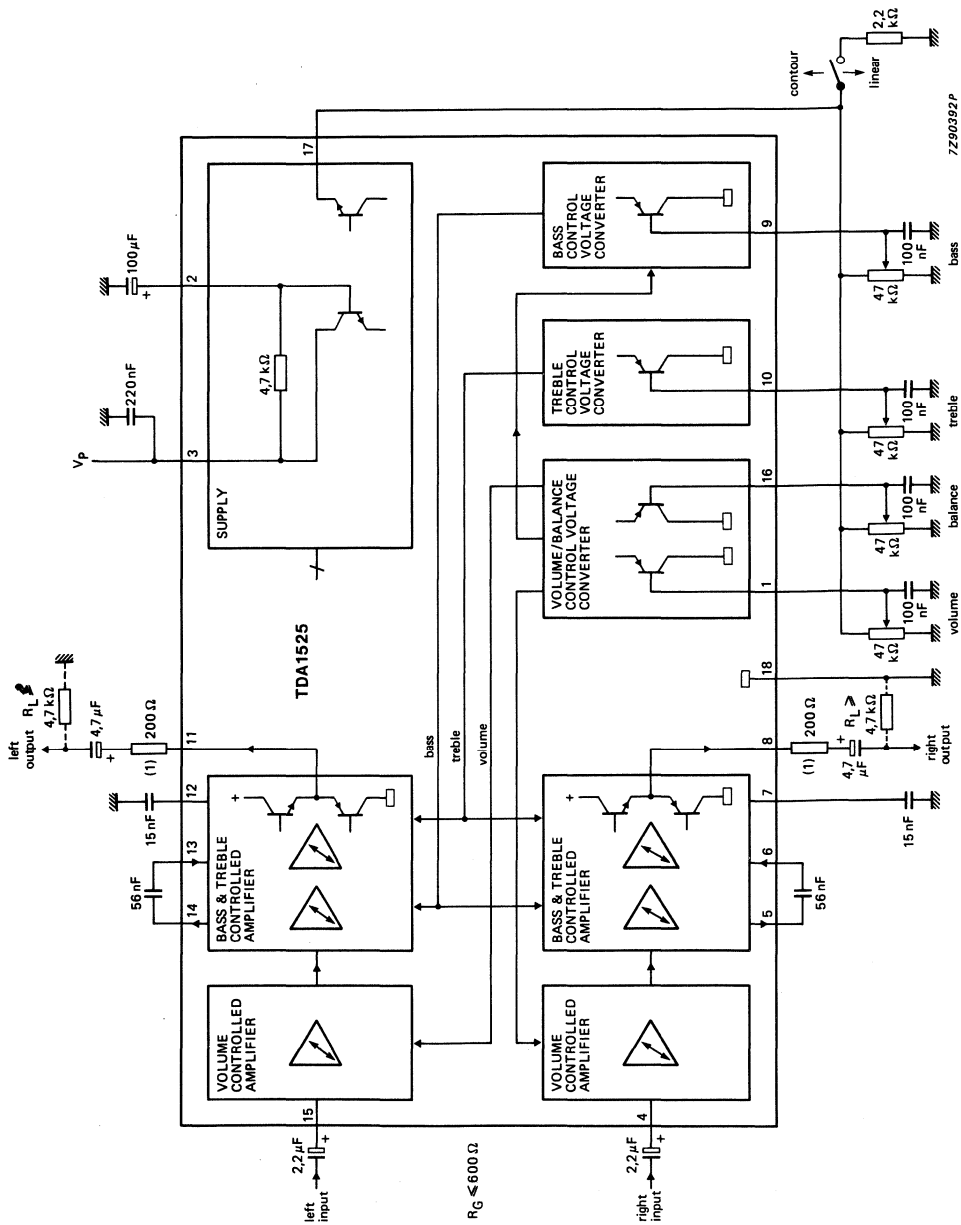
- Few external components necessary
- Low noise due to internal gain
- Bass emphasis can be increased by a double-pole low-pass filter
- Wide power supply voltage range

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 3)		$V_P = V_{3-18}$	7.5	12	16.5	V
Supply current		I_3	–	35	–	mA
Maximum input signal with DC feedback (RMS value)		$V_{i(rms)}$	–	2.5	–	V
Maximum output signal with DC feedback (RMS value)		$V_{o(rms)}$	–	3.0	–	V
Volume control range		ΔG_v	–80	–	+ 21.5	dB
Bass control range	at 40 Hz	ΔG_v	–	–19 to + 17	–	dB
Treble control range	at 16 kHz	ΔG_v	–	± 15	–	dB
Total harmonic distortion		THD	–	0.3	–	%
Output noise voltage (RMS value)	unweighted; f = 20 Hz to 20 kHz; V_P = 12 V					
for maximum voltage gain		$V_{no(rms)}$	–	310	–	μV
for voltage gain = –40 dB		$V_{no(rms)}$	–	100	–	μV
Channel separation	G_v = –20 to + 21.5 dB	α_{cs}	–	60	–	dB
Tracking between channels	G_v = –20 to + 26 dB	ΔG_v	–	–	2.5	dB
Ripple rejection	f = 100 Hz	RR	–	50	–	dB
Operating ambient temperature range		T_{amb}	–40	–	+ 85	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



(1) Series resistor is recommended in the event of the capacitive loads exceeding 200 pF.

Fig. 1 Block diagram and application circuit with single-pole filter.

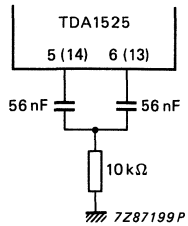


Fig.2 Double-pole low-pass filter for improved bass-boost.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 3)		$V_P = V_{3-18}$	–	18	V
Total power dissipation		P_{tot}	–	1200	mW
Storage temperature range		T_{stg}	–55	+ 150	°C
Operating ambient temperature range		T_{amb}	–40	+ 85	°C

DEVELOPMENT DATA

DC CHARACTERISTICS

$V_P = V_{3-18} = 12$ V; $T_{amb} = 25$ °C; all voltages are with reference to pin 18; measured in Fig. 1; $R_G \leqslant 600\ \Omega$; $R_L > 4.7$ kΩ; $C_L \leqslant 200$ pF; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		$V_P = V_3$	7.5	12	16.5	V
Supply current	V_P = 8.5 V	I_3	19	27	35	mA
	V_P = 9.7 V	I_3	—	—	40	mA
	V_P = 12.0 V	I_3	25	35	45	mA
	V_P = 15.0 V	I_3	30	43	56	mA
DC input levels (pins 4 and 15)	V_P = 8.5 V	$V_{4,15}$	3.8	4.25	4.7	V
	V_P = 12.0 V	$V_{4,15}$	5.3	5.9	6.6	V
	V_P = 15.0 V	$V_{4,15}$	6.5	7.3	8.2	V
DC output levels (pins 8 and 11)	all control voltage conditions					
	V_P = 8.5 V	$V_{8,11}$	3.3	4.25	5.2	V
	V_P = 12.0 V	$V_{8,11}$	4.6	6.0	7.4	V
	V_P = 15.0 V	$V_{8,11}$	5.7	7.5	9.3	V
Potentiometer supply voltage output (pin 17)	V_P = 8.5 V	V_{17}	3.25	3.6	3.85	V
Contour on/off switch (control by I_{17})						
contour	switch open	$-I_{17}$	—	—	0.5	mA
linear	switch closed	$-I_{17}$	1.5	—	10.0	mA
Application without potentiometer supply from pin 17 (contour cannot be switched off); voltage range forced to pin 17	$V_P \geqslant 10.8$ V	V_{17}	4.5	—	$\frac{V_P}{2} - V_{BE}$	V
DC voltage range for volume, bass, treble and balance controls (pins 1, 9, 10 and 16 respectively)	V_{17} = 5.0 V	$V_{1,9,10,16}$	1.0	—	4.25	V
	using supply from pin 17	$V_{1,9,10,16}$	0.25	—	3.8	V
Input current to pins 1, 9, 10 and 16		$-I_{1,9,10,16}$	—	—	5.0	μA

AC CHARACTERISTICS

$V_P = V_{3-18} = 8.5$ V; $T_{amb} = 25$ °C; all voltages are with reference to pin 18; measured in Fig. 1; contour switch closed (linear position); volume, balance, bass, and treble controls in mid-position; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4.7$ kΩ; $C_L \leqslant 200$ pF; f = 1 kHz; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Control range						
Max. gain (volume)	see Fig. 4	$G_{v\,max}$	20.5	21.5	23.0	dB
Volume control range	$G_{v\,max}/G_{v\,min}$	ΔG_v	90	100	–	dB
Balance control range	G_v = 0 dB; see Fig. 5	ΔG_v	–	–40	–	dB
Bass control range	f = 40 Hz; see Fig. 6	ΔG_v	± 12	–19 to +17	–	dB
Treble control range	f = 16 kHz; see Fig. 7	ΔG_v	± 12	± 15	–	dB
Contour characteristics			see Figs 8 and 9			
Input signals (pins 4 and 15)						
Input resistance with volume control gain	note 1					
at 20 dB	G_v = 20 dB	$R_{i4,\,15}$	10	–	–	kΩ
at –40 dB	G_v = –40 dB	$R_{i4,\,15}$	–	160	–	kΩ
Output signals (pins 8 and 11)						
Output resistance		$R_{o8,\,11}$	–	–	300	Ω
Signal processing						
Power supply ripple rejection	$V_{P(rms)} \leqslant 200$ mV; f = 100 Hz; G_v = 0 dB	RR	35	50	–	dB
Channel separation	250 Hz to 10 kHz; G_v = –20 to + 21.5 dB	α_{cs}	46	60	–	dB
Spread of volume control with constant control voltage	$V_1 = V_{17}/2$	ΔG_v	–	–	± 3	dB
Gain tolerance between left and right channels	$V_1 = V_{16} = V_{17}/2$	ΔG_{vL-R}	–	–	1.5	dB
Tracking between channels	G_v = 21.5 to –26 dB; f = 250 Hz to 6.3 kHz; balance adjusted for G_v = 10 dB	ΔG_v	–	–	2.5	dB

DEVELOPMENT DATA

AC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Signal handling						
Input signal handling (RMS value)	V_P = 8.5 V; THD = 0.5%; f = 1 kHz	$V_{i(rms)}$	1.4	–	–	V
	V_P = 8.5 V; THD = 0.7%; f = 1 kHz	$V_{i(rms)}$	1.8	2.4	–	V
	V_P = 12 V; THD = 0.5%; f = 40 Hz to 16 kHz	$V_{i(rms)}$	1.4	–	–	V
	V_P = 12 V; THD = 0.7%; f = 40 Hz to 16 kHz	$V_{i(rms)}$	2.0	3.2	–	V
	V_P = 15 V; THD = 0.5%; f = 40 Hz to 16 kHz	$V_{i(rms)}$	1.4	–	–	V
	V_P = 15 V; THD = 0.7%; f = 40 Hz to 16 kHz	$V_{i(rms)}$	2.0	3.2	–	V
Output signal handling (RMS value)	notes 2 and 3; V_P = 8.5 V; THD = 0.5%; f = 1 kHz	$V_{o(rms)}$	1.8	2.0	–	V
	V_P = 8.5 V; THD = 10%; f = 1 kHz	$V_{o(rms)}$	–	2.2	–	V
	V_P = 12 V; THD = 0.5%; f = 40 Hz to 16 kHz	$V_{o(rms)}$	2.5	3.0	–	V
	V_P = 15 V; THD = 0.5%; f = 40 Hz to 16 kHz	$V_{o(rms)}$	–	3.5	–	V

parameter	conditions	symbol	min.	typ.	max.	unit
Noise performance (V_P = 8.5 V)						
Output noise voltage; unweighted (RMS value)	see Fig. 14; f = 20 Hz to 20 kHz					
for max. voltage gain	note 4	$V_{no(rms)}$	–	260	–	μV
for G_V = −3 dB	note 4	$V_{no(rms)}$	–	70	140	μV
Output noise voltage; weighted as DIN45405 of 1981, CCIR recommendation 468-2 (peak value)						
for max. voltage gain for max. emphasis of bass and treble	note 4	$V_{no(m)}$	–	890	–	μV
	contour off; G_V = −40 dB	$V_{no(m)}$	–	360	–	μV
Noise performance (V_P = 12 V)						
Output noise voltage; unweighted (RMS value)	see Fig. 14; f = 20 Hz to 20 kHz; note 5					
for max. voltage gain	note 4	$V_{no(rms)}$	–	310	–	μV
for G_V = −16 dB	note 4	$V_{no(rms)}$	–	100	200	μV
Output noise voltage; weighted as DIN45405 of 1981, CCIR recommendation 468-2 (peak value)						
for max. voltage gain for max. emphasis of bass and treble	note 4	$V_{no(m)}$	–	940	–	μV
	contour off; G_V = −40 dB	$V_{no(m)}$	–	400	–	μV

DEVELOPMENT DATA

AC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Noise performance (V_P = 15 V)						
Output noise voltage; unweighted (RMS value)	see Fig. 14; f = 20 Hz to 20 kHz; note 5					
for max. voltage gain	note 4	$V_{no(rms)}$	–	350	–	μV
for G_v = –16 dB	note 4	$V_{no(rms)}$	–	110	220	μV
Output noise voltage; weighted as DIN45405 of 1981, CCIR recommendation 468-2 (peak value)						
for max. voltage gain for max. emphasis of bass and treble	note 4	$V_{no(m)}$	–	980	–	μV
	contour off; G_v = –40 dB	$V_{no(m)}$	–	420	–	μV

Notes to the characteristics

1. Equation for input resistance (see also Fig. 3)

$$R_i = \frac{160\ k\Omega}{1 + G_v};\ G_{v\,max} = 12.$$

2. Frequencies below 200 Hz and above 5 kHz have reduced voltage swing, the reduction at 40 Hz and at 16 kHz is 30%.
3. In the event of bass boosting the output signal handling is reduced. The reduction is 1 dB for maximum bass boost.
4. Linear frequency response.
5. For peak values add 4.5 dB to RMS values.

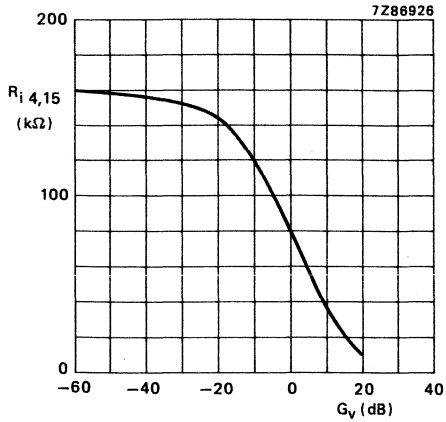


Fig. 3 Input resistance (R_i) as a function of gain of volume control (G_V). Measured in Fig. 1.

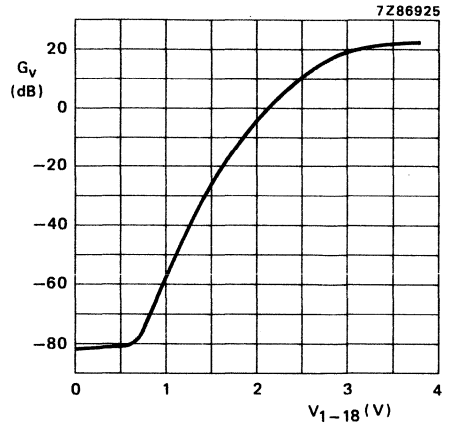


Fig. 4 Volume control curve; voltage gain (G_V) as a function of control voltage ($V_{1\text{-}18}$). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8.5 V; f = 1 kHz.

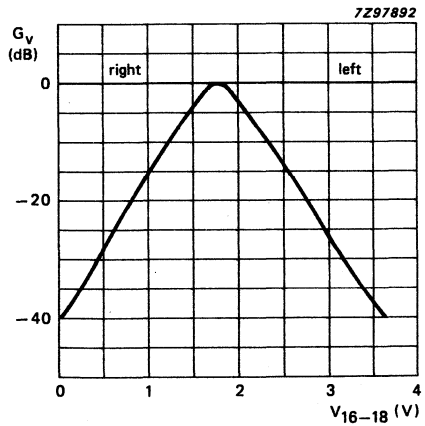


Fig. 5 Balance control curve; voltage gain (G_V) as a function of control voltage ($V_{16\text{-}18}$). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8.5 V.

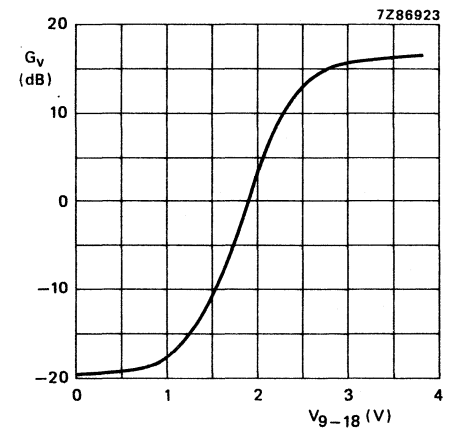


Fig. 6 Bass control curve; voltage gain (G_V) as a function of control voltage ($V_{9\text{-}18}$). Measured in Fig. 1 with single-pole filter (internal potentiometer supply from pin 17 used); V_P = 8.5 V; f = 40 Hz.

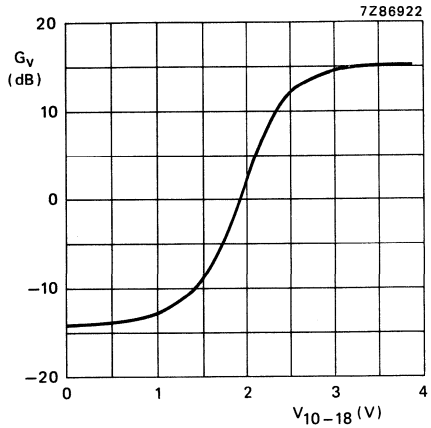


Fig. 7 Treble control curve; voltage gain (G_v) as a function of control voltage ($V_{10\text{-}18}$). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8.5 V; f = 16 kHz.

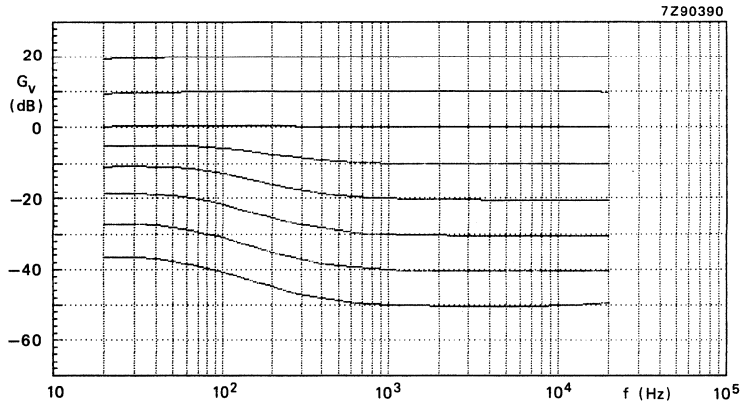


Fig. 8 Contour frequency response curves; voltage gain (G_v) as a function of audio input frequency. Measured in Fig. 1 with single-pole filter; V_P = 8.5 V.

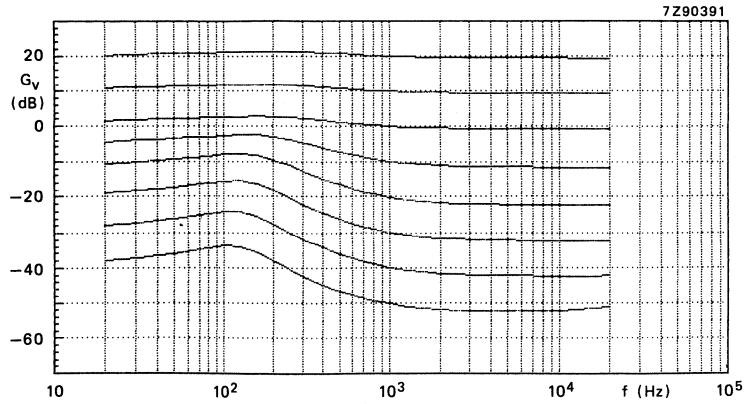


Fig. 9 Contour frequency response curves; voltage gain (G_v) as a function of audio input frequency. Measured in Fig. 1 with double-pole filter; V_P = 8.5 V.

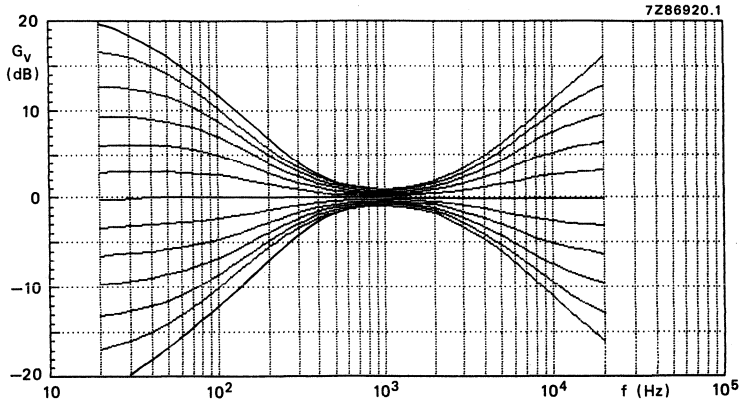


Fig. 10 Tone control frequency response curves; voltage gain (G_v) as a function of audio input frequency. Measured in Fig. 1 with single-pole filter; V_P = 8.5 V.

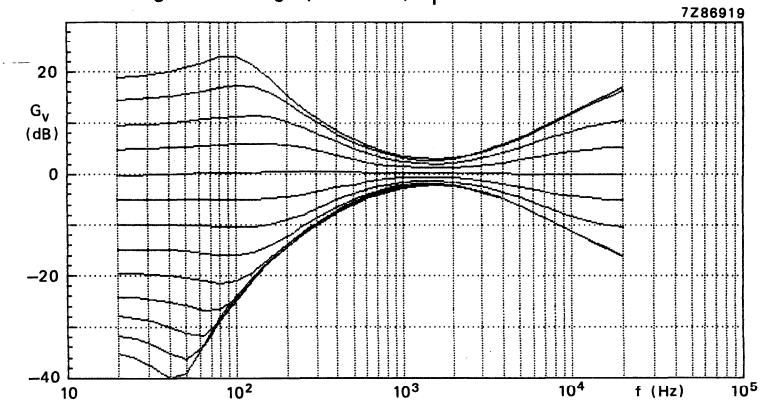


Fig. 11 Tone control frequency response curves; voltage gain (G_v) as a function of audio input frequency. Measured in Fig. 1 with double-pole filter; V_P = 8.5 V.

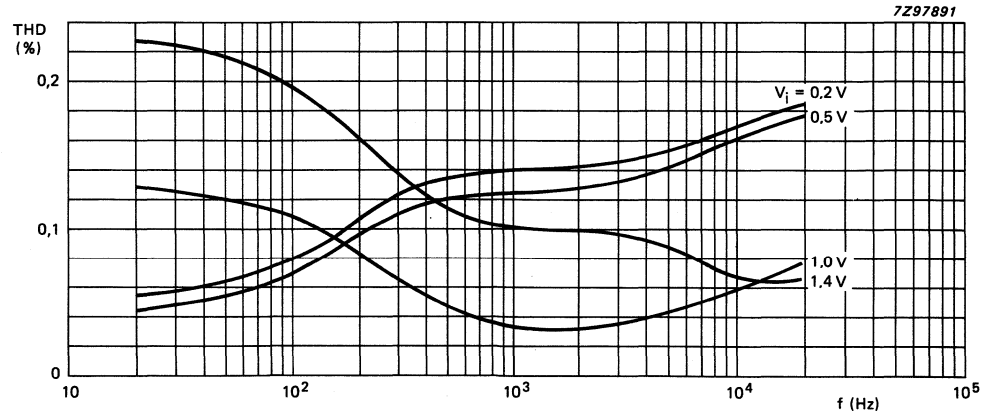


Fig. 12 Total harmonic distortion (THD) as a function of audio input frequency. Measured in Fig. 1; V_P = 8.5 V; volume control voltage gain at $G_v = 20 \log \frac{V_o}{V_i} = 0$ dB.

DEVELOPMENT DATA

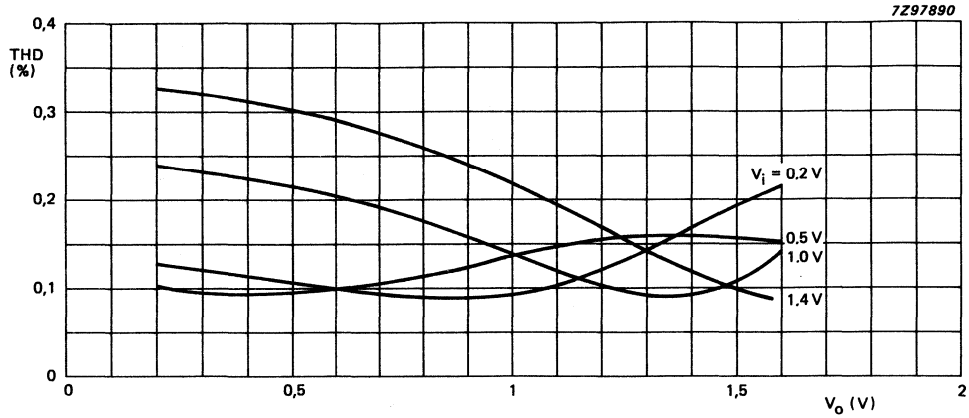
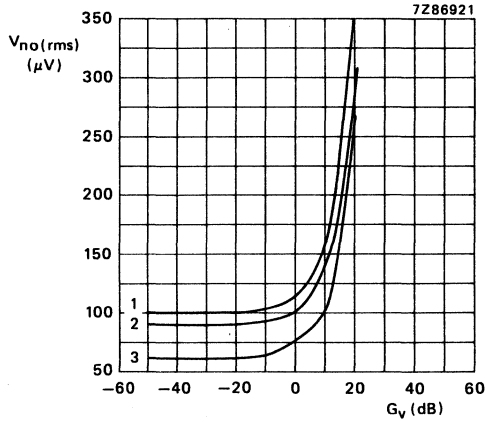


Fig. 13 Total harmonic distortion (THD) as a function of output voltage (V_O). Measured in Fig. 1; V_P = 8.5 V; f = 1 kHz.



(1) V_P = 15 V.
(2) V_P = 12 V.
(3) V_P = 8.5 V.

Fig. 14 Noise output voltage ($V_{no(rms)}$; unweighted) as a function of voltage gain (G_V). Measured in Fig. 1; f = 20 Hz to 20 kHz.

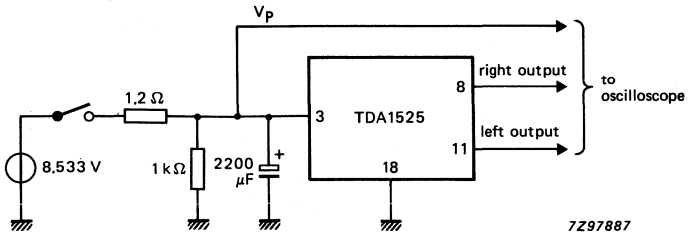
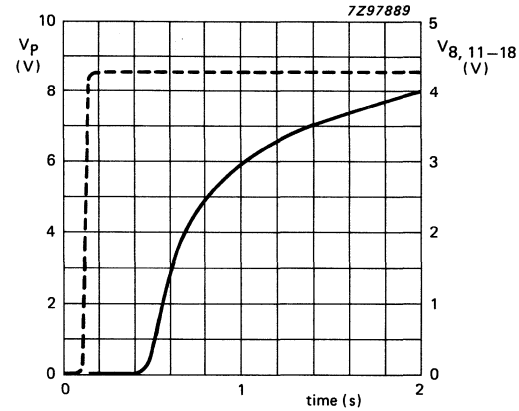


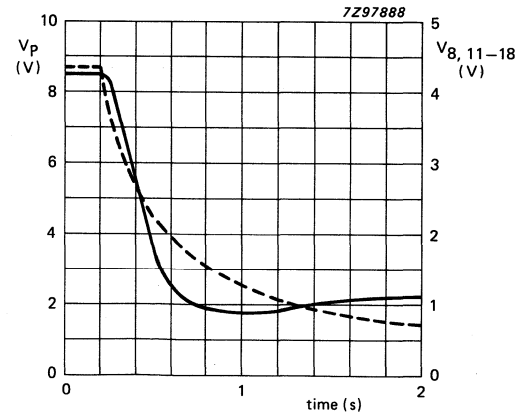
Fig. 15 Test circuit for power-on and power-off response measurements.



– – – – – represents V_P

——— represents $V_{8, 11-18}$

Fig. 16 Response at power-on. Measured in circuit of Fig. 15.



– – – – – represents V_P

——— represents $V_{8, 11-18}$

Fig. 17 Response at power-off. Measured in circuit of Fig. 15.

14-BIT ANALOGUE TO DIGITAL CONVERTER (ADC)

An integrated 14-bit analogue to digital converter (ADC) which uses the successive approximation conversion technique and includes the comparator, reference source and clock on the same chip.
The high linearity makes it very suitable for signal processing while the accurate, temperature-compensated reference source makes it applicable for instrumentation purposes.
The ADC accepts unipolar or bipolar input signals.
Digital output data is in serial form.
All digital outputs are fully TTL compatible.

QUICK REFERENCE DATA

Positive supply voltage (pin 5)	V_P	typ.	5 V
Negative supplu voltage 1 (pin 6)	$-V_{N1}$	typ.	5 V
Negative supply voltage 2 (pin 9)	$-V_{N2}$	typ.	17 V
Signal-to-noise ratio	S/N	typ.	84 dB
Linearity error		typ.	± ½ LSB
Total power dissipation	P_{tot}	typ.	500 mW
Operating ambient temperature range	T_{amb}	−20 to	+ 70 °C
Storage temperature range	T_{stg}	−55 to	+ 150 °C
Resolution			14 bits
Full scale input current	I_{FS}	typ.	4 mA

PACKAGE OUTLINE

28-lead dual in-line; plastic (with internal heat spreader) (SOT117).

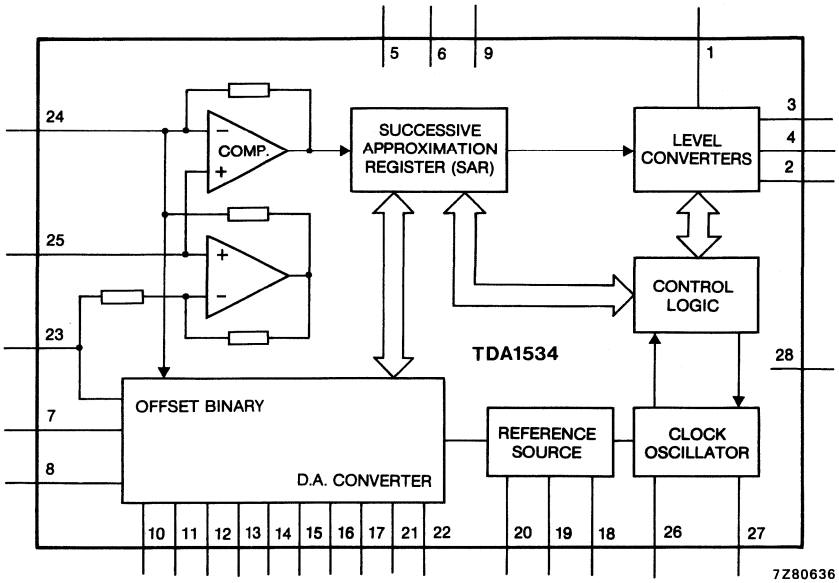


Fig. 1 Block diagram.

PIN DESIGNATION

1	start conversion
2	status out
3	data out
4	data strobe
5	positive supply voltage
6	negative supply voltage 1
7	oscillator input
8	oscillator input
9	negative supply voltage 2
10, 11, 12, 13, 14	decoupling binary weighted current sources
15, 16, 17	decoupling binary weighted current sources
18	I_{ref1}
19	I_{ref2}
20	I_{ref3}
21, 22	decoupling binary weighted current sources
23	offset binary input
24	analogue signal input
25	analogue ground
26	oscillator
27	oscillator
28	digital ground

FUNCTIONAL DESCRIPTION

The circuit consists of the following parts:

14-bit D/A converter

Using "dynamic element matching", which results in high accuracy, linearity and longterm stability, without the need of trimming. The main parts of the DAC are the binary wieghted current sources and the bit switches. The DAC also delivers an offset binary current for bipolar operation of the ADC.

Fast settling comparator/substractor

Consisting of a high speed, clamped operational amplifier with special frequency compensation system.

Successive approximation register (SAR)

This register is an array of fourteen addressable latches, with the outputs connected to the bit switches of the D/A converter.

Logic-level converters

Converting the internally used current-mode-logic (CML) levels to TTL levels, for easy interface of the ADC with standard logic families.

Clock oscillator and control logic

Delivering the pulses and timing for the SAR and takes care of the communication with the peripheral circuits.

Reference source

Based on the bandgap voltage of silicon, with extra temperature compensation circuit.

For the timing of the output signals see Fig. 3. At the leading edge of the start conversion (SC) pulse the ADC starts converting the input voltage. During the conversion cycle the following signals appear at the output pins:

Status (pin 2)

This signal can be used to force the Sample-Hold-Circuit, in front of the ADC, in hold mode.

Data strobe (pin 4)

This signal is used to clock the data-out signal into the peripheral devices.

Data out (pin 3)

The 14 bits serial, binary, output code of the A/D converter starting with the most significant bit (MSB). The data must be considered valid at the trailing edge of the data-strobe signal.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Positive supply (pin 5)	V_P	0 to 7 V
Negative supply voltage (pin 6)	$-V_{N1}$	0 to 7 V
Negative supply voltage (pin 9)	$-V_{N2}$	0 to 20 V
Storage temperature	T_{stg}	−55 to + 150 °C
Operating ambient temperature range	T_{amb}	−20 to + 70 °C
Total power dissipation	P_{tot}	derating curve (Fig. 2)

CHARACTERISTICS (see application circuit Fig. 4)

V_P = 5 V; $-V_{N1}$ = 5 V; $-V_{N2}$ = 17 V; T_{amb} = + 25 °C, unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Positive supply voltage (pin 5)	V_P	4	5	6	V
Negative supply voltage 1 (pin 6)	$-V_{N1}$	–	5	–	V
Negative supply voltage 2 (pin 9)	$-V_{N2}$	16,5	17	18	V
Positive supply current	I_P	–	30	40	mA
Negative supply current	$-I_{N1}$	–	37	45	mA
Negative supply current	$-I_{N2}$	–	10	13	mA
Total power dissipation	P_{tot}	–	500	–	mW
Resolution		–	14	–	bits
Analogue input					
Full scale input current offset-binary current switched off	I_{FS}	3,8	4,0	4,2	mA
Temperature coefficient pin 23 short-circuited	TC	–	t.b.f.	–	10^{-6}/K
Zero-offset offset-binary current switched off					
Offset voltage	$-V_o$	10	20	30	mV
Temperature coefficient	TC	–	t.b.f.	–	μV/K
Offset current	I_o	–	500	–	nA
Temperature coefficient	TC	–	t.b.f.	–	nA/K
Linearity					
Linearity error		–	± ¼	–	LSB
Linearity from −20 to + 70 °C		–	± ½	–	LSB
Offset binary current	I_{BO}	$0{,}45 \cdot I_{FS}$	$0{,}50 \cdot I_{FS}$	$0{,}55 \cdot I_{FS}$	mA
Temperature coefficient	TC	–	t.b.f.	–	10^{-6}/K
Signal to noise ratio*	S/N	80	84	–	dB

parameter	symbol	min.	typ.	max.	unit
Start conversion (pin 1)					
Input current					
V_{IL} (< 0,8 V)	$-I_1$	–	–	1,6	mA
V_{IH} (> 2,0 V)	I_1	–	–	40	μA
Data, strobe, status (pins 3, 4 and 2)					
Output current					
V_{OL} (< 0,6 V)	$I_{3, 4, 2}$	6,4	16	–	mA
V_{OH} (> 2,4 V)	$-I_{3, 4, 2}$	160	400	–	μA
Conversion time					
$C_{26\text{-}27}$ = 220 pF ± 1%	t_C	–	8,5	–	μs
Signal width (pin 1)					
start conversion	t_{SC}	0,2	–	t_C	μs
Delay time (pin 2)					
status out	t_{SD}	–	60	–	ns
Set-up time (pin 3)					
data out	t_{DS}	–	25	–	ns
Pulse duration (pin 4)					
data strobe high	t_{DSH}	–	125	–	ns

* Signal-to-noise ratio within 10 Hz and 20 kHz bandwidth of a 1 kHz full scale sinewave, generated at a sample rate of 44 kHz.

DEVELOPMENT DATA

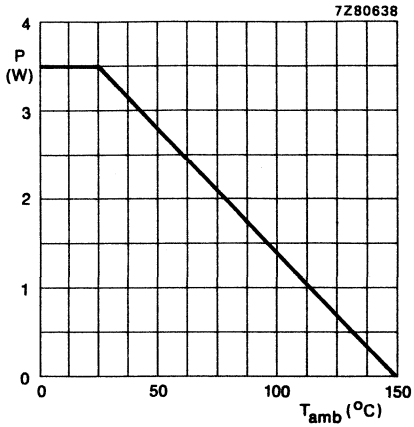


Fig. 2 Power derating curve.

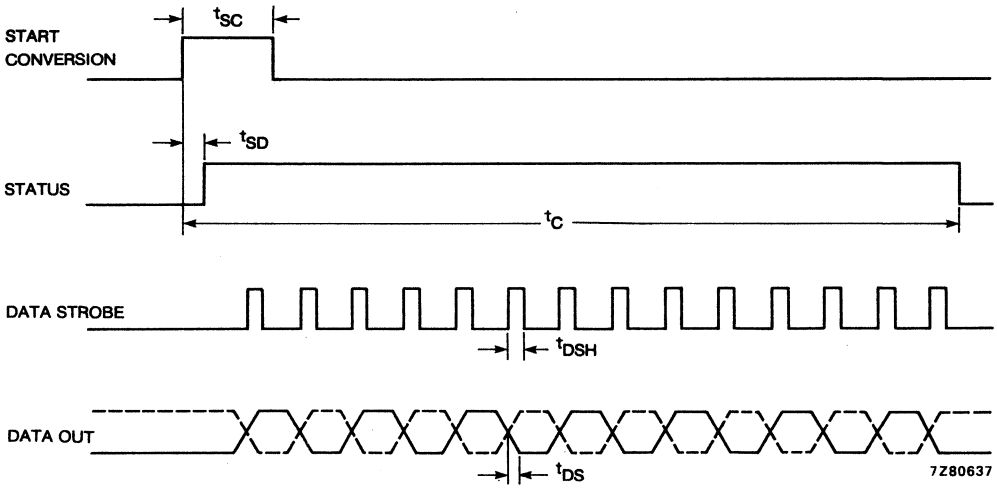


Fig. 3 Switching times waveforms.

DEVELOPMENT DATA

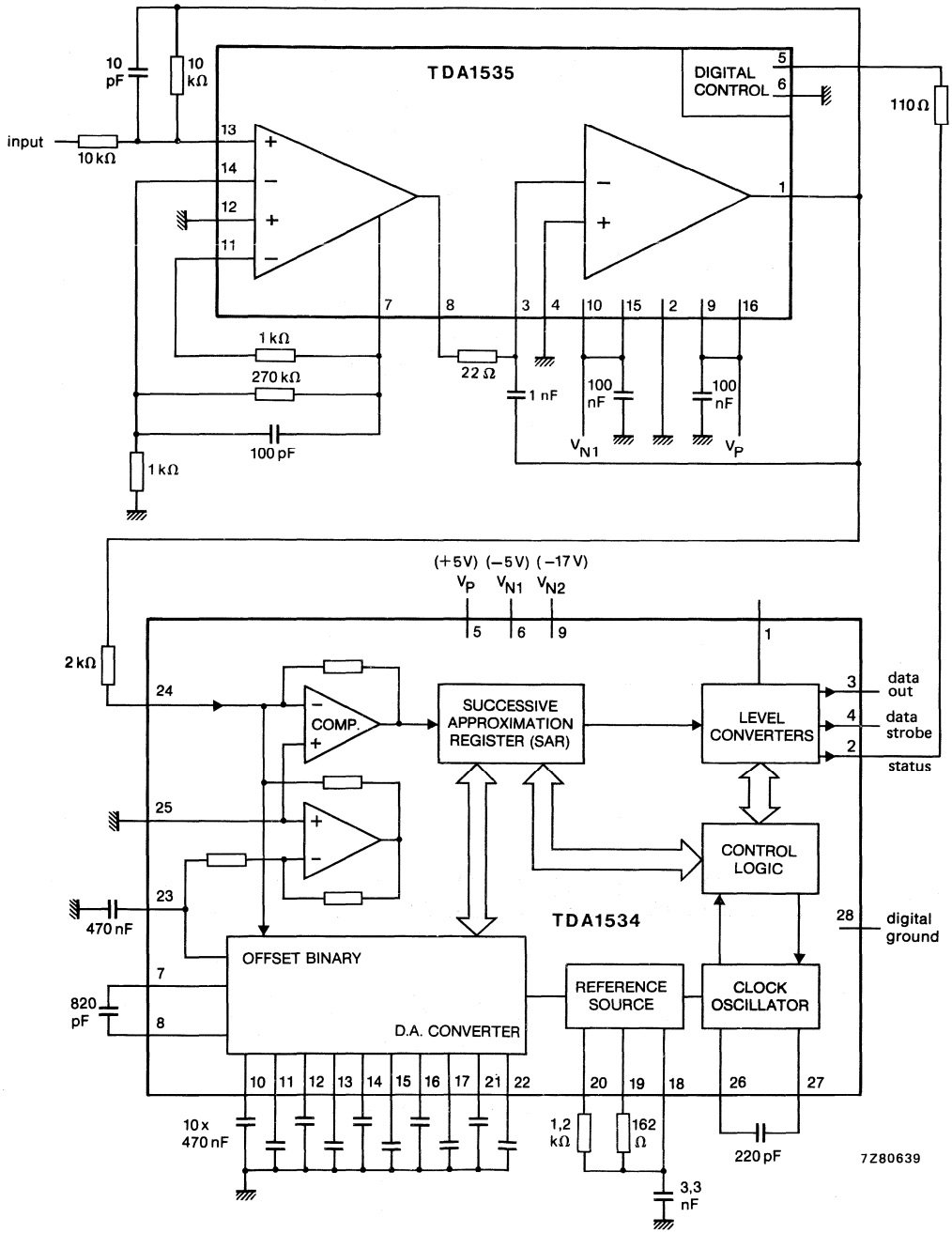


Fig. 4 Application and test circuit.

All earthed components connected to analogue ground (pin 25).

DUAL 16-BIT DAC

GENERAL DESCRIPTION

The TDA1541A is a monolithic integrated dual 16-bit digital-to-analogue converter (DAC) designed for use in hi-fi digital audio equipment such as Compact Disc players, digital tape or cassette recorders.

Features

- Selectable two-channel input format: offset binary or two's complement
- Internal timing and control circuit
- TTL compatible digital inputs
- High maximum input bit-rate and fast settling time
- No requirement for external deglitcher circuitry

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltages					
pin 28	V_{DD}	4,5	5,0	5,5	V
pin 26	$-V_{DD1}$	4,5	5,0	5,5	V
pin 15	$-V_{DD2}$	14,0	15,0	16,0	V
Supply currents					
pin 28	I_{DD}	–	27	40	mA
pin 26	$-I_{DD1}$	–	37	50	mA
pin 15	$-I_{DD2}$	–	25	35	mA
Signal-to-noise ratio (including THD) (full-scale sinewave) at analogue outputs (AOL; AOR)	S/(N + D)	90	95	–	dB
Non-linearity at T_{amb} = −20 to + 85 °C	NL	–	0,5	1,0	LSB
Current settling time to ± 1 LSB	t_{cs}	–	0,5	–	μs
Input bit rate at data input (pins 3 and 4)	BR	–	–	6,4	Mbits/s
Clock frequency at clock input (pin 2)	f_{BCK}	–	–	6,4	MHz
Full scale temperature coefficient at analogue outputs (AOL; AOR)	TC_{FS}	–	± 200 x 10^{-6}	–	K^{-1}
Operating ambient temperature range	T_{amb}	−40	–	+ 85	°C
Total power dissipation	P_{tot}	–	700	–	mW

PACKAGE OUTLINE

28-lead DIL; plastic with internal heat spreader (SOT-117).

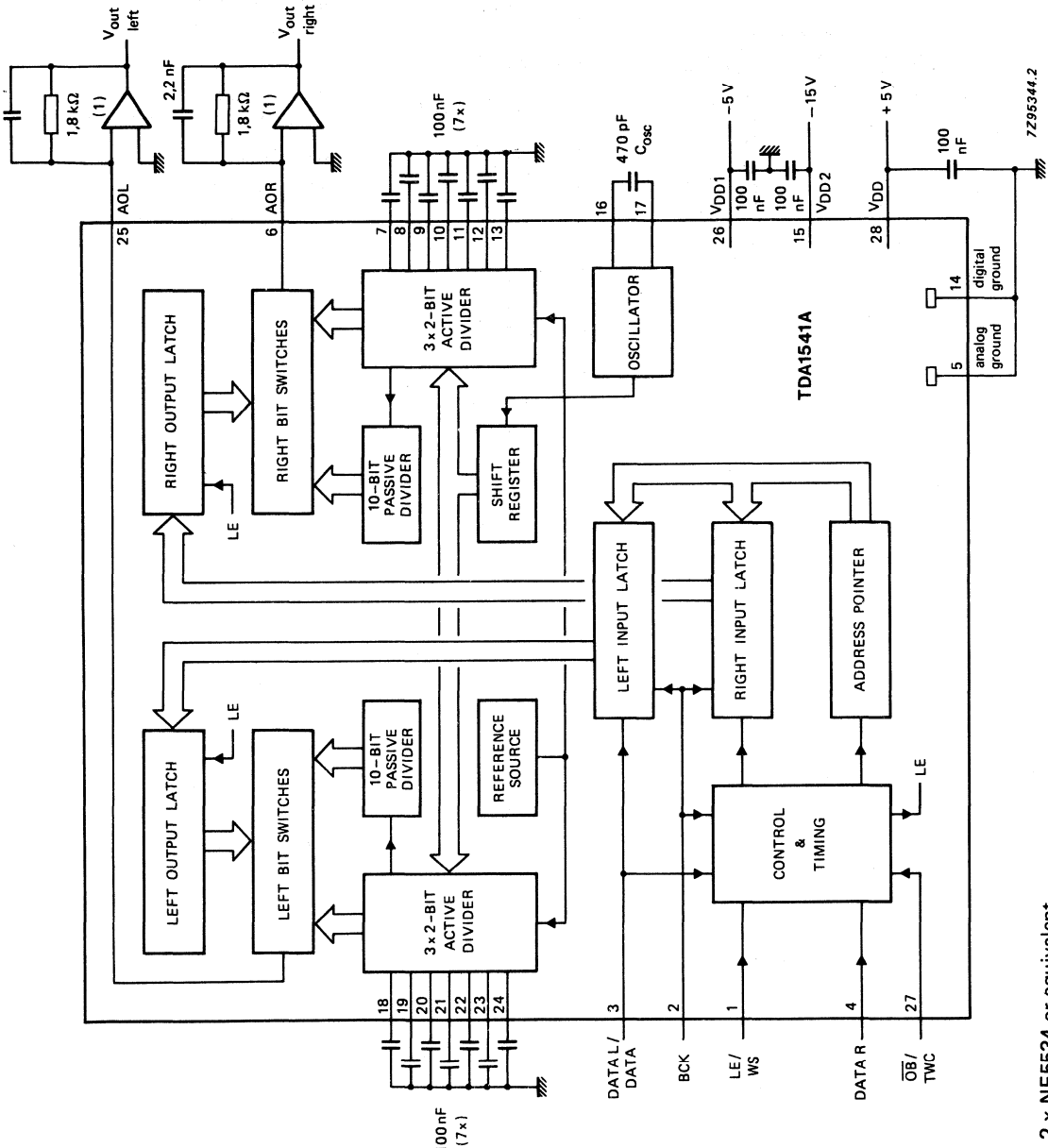


Fig. 1 Block diagram.

(1) TDA1542, 2 x NE5534 or equivalent.

DEVELOPMENT DATA

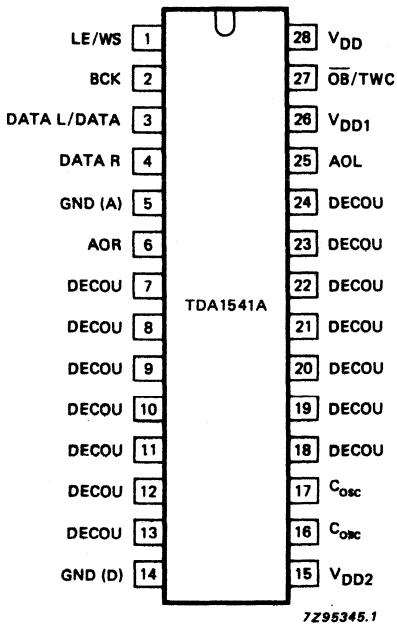


Fig. 2 Pinning diagram.

PINNING

1	LE/WS*	latch enable input word select input
2	BCK*	bit clock input
3	DATA L/DATA*	data left channel input data input (selected format)
4	DATA R*	data right channel input
5	GND (A)	analogue ground
6	AOR	right channel output
7	DECOU	decoupling
8	DECOU	
9	DECOU	
10	DECOU	
11	DECOU	
12	DECOU	
13	DECOU	
14	GND (D)	digital ground
15	V_{DD2}	−15 V supply voltage
16	COSC	oscillator
17	COSC	
18	DECOU	decoupling
19	DECOU	
20	DECOU	
21	DECOU	
22	DECOU	
23	DECOU	
24	DECOU	
25	AOL	left channel output
26	V_{DD1}	−5 V supply voltage
27	$\overline{OB}$/TWC*	mode selection input
28	V_{DD}	+ 5 V supply voltage

* See Table 1 data selection input.

FUNCTIONAL DESCRIPTION

The TDA1541A accepts input sample formats in time multiplexed mode or simultaneous mode with any bit length. The most significant bit (MSB) must always be first.
This flexible input data format allows easy interfacing with signal processing chips such as interpolation filters, error correction circuits, pulse code modulation adaptors and audio signal processors (ASP).

The high maximum input bit-rate and fast settling time facilitates application in 4 x oversampling systems (44,1 kHz to 176,4 kHz or 48 kHz to 192 kHz) with the associated simple analogue filtering function (low order, linear phase filter).

Input data selection (see also Table 1)

With input $\overline{OB}$/TWC connected to ground, data input (offset binary format) must be in time multiplexed mode. It is accompanied with a word select (WS) and a bit clock input (BCK) signal. The converted samples appear at the output, at the first positive going transition of the bit clock signal after a negative going transition of the word select signal.

With $\overline{OB}$/TWC connected to V_{DD} the mode is the same but the data format must be in two's complement.

When input $\overline{OB}$/TWC is connected to V_{DD1} the two channels of data (L/R) are input simultaneously via DATA L and DATA R, accompanied with BCK and a latch-enable input (LE). With this mode selected the data must be in offset binary. The converted samples appear at the output at the positive going transition of the latch enable signal.

The format of data input signals is shown in figures 3 and 4.

True 16-bit performance is achieved by each channel using three 2-bit active dividers, operating on the dynamic element matching principle, in combination with a 10-bit passive current-divider, based on emitter scaling.
All digital inputs are TTL compatible.

Table 1 Input data selection

$\overline{OB}$/TWC	mode	pin 1	pin 2	pin 3	pin 4
−5 V	simultaneous	LE	BCK	DATA L	DATA R
0 V	time MUX OB	WS	BCK	DATA OB	not used
+ 5 V	time MUX TWC	WS	BCK	DATA TWC	not used

Where:

LE = latch enable
WS = word select, LOW = left channel; HIGH = right channel
BCK = bit clock
DATA L = data left
DATA R = data right
DATA OB = data offset binary
DATA TWC = data two's complement
MUX OB = multiplexed offset binary
MUX TWC = multiplexed two's complement = I^2S – format.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage ranges				
pin 28	V_{DD}	0	7	V
pin 26	$-V_{DD1}$	0	7	V
pin 15	$-V_{DD2}$	0	17	V
Storage temperature range	T_{stg}	−65	+ 150	°C
Operating ambient temperature range	T_{amb}	−40	+ 85	°C
Electrostatic handling*	V_{es}	−1000	+ 1000	V

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 30 K/W

DEVELOPMENT DATA

* Equivalent to discharging a 250 pF capacitor through a 1 kΩ series resistor.

CHARACTERISTICS

V_{DD} = 5 V; $-V_{DD1}$ = 5 V; $-V_{DD2}$ = 15 V; T_{amb} = + 25 °C; measured in the circuit of Fig. 1; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage ranges						
pin 28		V_{DD}	4,5	5,0	5,5	V
pin 26		$-V_{DD1}$	4,5	5,0	5,5	V
pin 15		$-V_{DD2}$	14,0	15,0	16,0	V
Voltage difference between analogue and digital ground		$V_{GND(A)} - V_{GND(D)}$	−0,3	0	+ 0,3	V
Supply currents						
pin 28		I_{DD}	–	27	40	mA
pin 26		$-I_{DD1}$	–	37	50	mA
pin 15		$-I_{DD2}$	–	25	35	mA
Inputs						
Input current pins (1, 2, 3 and 4)						
digital inputs LOW	0,8 V	$-I_{IL}$	–	–	0,4	mA
digital inputs HIGH	2,0 V	I_{IH}	–	–	20	μA
Digital input current (pin 27)						
+ 5 V		$\|I_{\overline{OB}/TWC}\|$	–	–	1	μA
0 V		$\|I_{\overline{OB}/TWC}\|$	–	–	20	μA
−5 V		$\|I_{\overline{OB}/TWC}\|$	–	–	40	μA
Input frequency/bit rate						
clock input pin 2		f_{BCK}	–	–	6,4	MHz
data inputs pins 3 and 4		f_{DAT}	–	–	6,4	Mbits/s
word select input pin 1		f_{WS}	–	–	200	kHz
latch enable pin 1		f_{LE}	–	–	200	kHz
Input capacitance of digital inputs		C_I	–	12	–	pF
Oscillator (pins 16 and 17)						
Oscillator frequency	C_{osc} = 470 pF	f_{osc}	150	200	275	kHz
Analogue outputs (note 1) (AOL, AOR)						
Resolution		Res	–	16	–	bits
Full scale current		I_{FS}	3,4	4,0	4,6	mA
Zero scale current		$\|I_{ZS}\|$	–	25	50	nA
Full scale temperature coefficient	T_{amb} = − 20 to + 85 °C	TC_{FS}	–	± 200 x 10^{-6}	–	K^{-1}

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Linearity error integral	T_{amb} = 25 °C	E_L	–	0,5	1,0	LSB
	T_{amb} = –20 to + 85 °C	E_L	–	–	1,0	LSB
Linearity error differential	T_{amb} = 25 °C	E_{dL}	–	0,5	1,0	LSB
	T_{amb} = –20 to + 85 °C	E_{dL}	–	–	1,0	LSB
Total harmonic distortion		THD	–	–100	–	dB
Signal-to-noise ratio (including THD)	note 2	S/(N + D)	90	95	–	dB
Settling time ± 1 LSB		t_{cs}	–	0,5	–	μs
Channel separation		α	90	98	–	dB
Unbalance between outputs		$\|\Delta\|FS\|$	–	0,1	0,3	dB
Time delay between outputs		t_d	–	–	0,2	μs
Supply voltage ripple rejection	note 3					
V_{DD} = + 5 V		SVRR	–	–76	–	dB
V_{DD1} = –5 V		SVRR	–	–84	–	dB
V_{DD2} = –15 V		SVRR	–	–58	–	dB
Signal-to-noise ratio						
at bipolar zero		S/N	–	110	–	dB
at full scale		S/N	98	104	–	dB
Timing	Figs 3 and 4					
Rise time		t_r	–	–	32	ns
Fall time		t_f	–	–	32	ns
Bit clock cycle time		t_{CY}	156	–	–	ns
Bit clock HIGH time		t_{HB}	46	–	–	ns
Bit clock LOW time		t_{LB}	46	–	–	ns
Bit clock fall time to latch enable rise time		t_{FBRL}	0	–	–	ns
Bit clock rise time to latch enable fall time		t_{RBFL}	0	–	–	ns
Data set-up time		$t_{SU;DAT}$	32	–	–	ns
Data hold time to bit clock		$t_{HD;DAT}$	0	–	–	ns
Word select hold time		$t_{HD;WS}$	0	–	–	ns
Word select set-up time		$t_{SU;WS}$	32	–	–	ns

Notes to the characteristics

1. To ensure no performance losses, permitted output voltage compliance is ± 25 mV maximum.
2. Signal-to-noise ratio + THD with 1 kHz full scale sinewave generated at a sampling rate of 176,4 kHz.
3. V_{ripple} = 100 mV and f_{ripple} = 100 Hz.

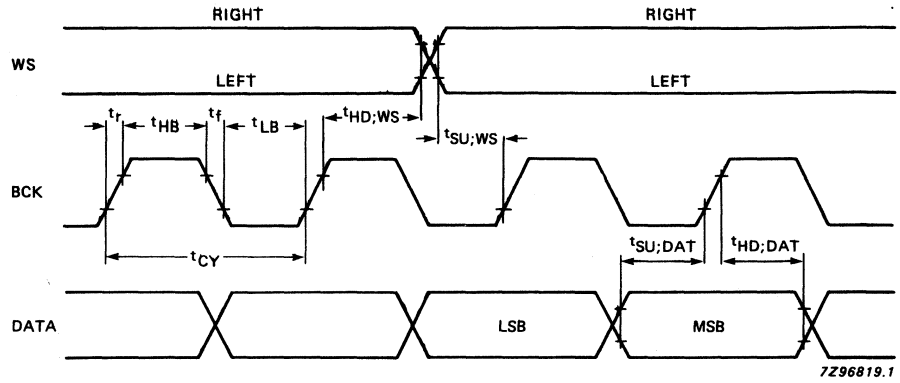


Fig. 3 Format of input signals; time multiplexed (I^2S format).

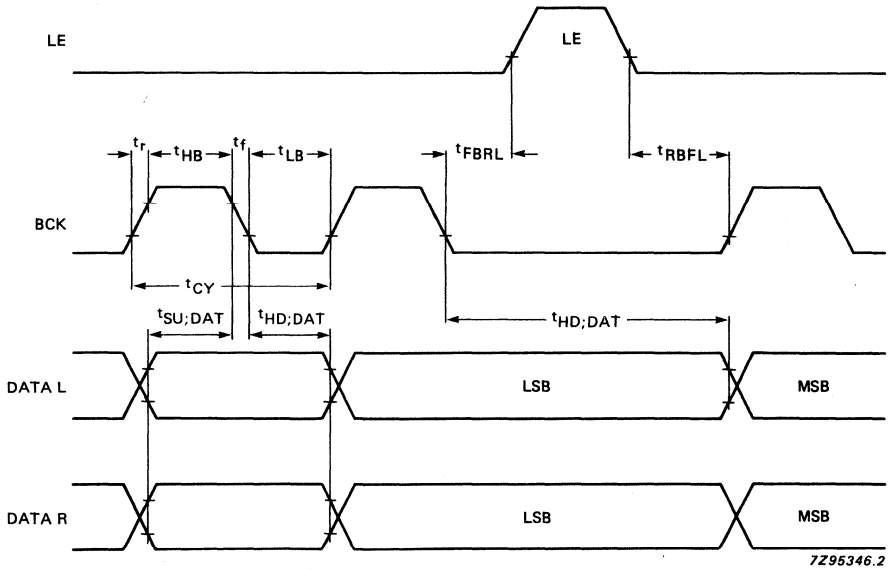


Fig. 4 Format of input signals; simultaneous data.

DUAL 16—BIT DAC (ECONOMY VERSION)

GENERAL DESCRIPTION

The TDA1543 is a monolithic integrated dual 16-bit digital-to-analogue converter (DAC) designed as an economy version for use in hi-fi digital audio equipment such as Compact Disc players, digital tape or cassette recorders.

Features

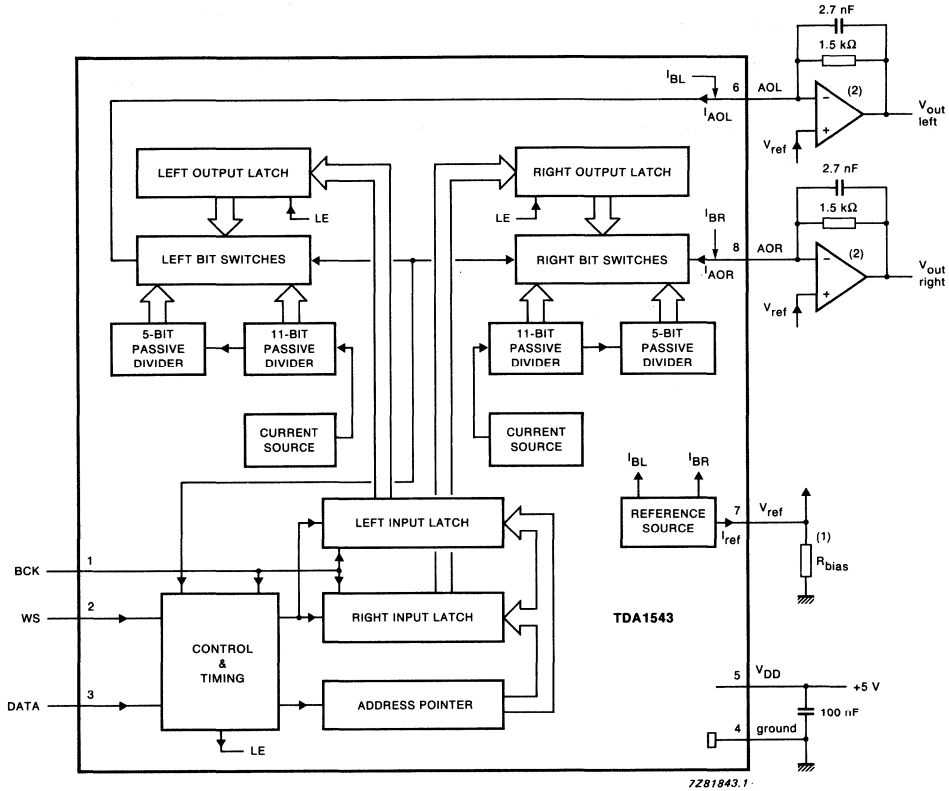
- Low distortion
- 16-bit dynamic range
- 4 x oversampling possible
- Single 5 V power supply
- No external components required
- No requirement for external deglitcher circuitry due to fast settling output current
- Adjustable bias current
- Internal timing and control circuits
- I^2S input format: time multiplexed, two's complement, TTL

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{DD}	3.0	5.0	8.0	V
Supply current	I_{DD}	–	50	60	mA
Signal-to-noise ratio (including THD) (full-scale sinewave) at analogue outputs (AOL; AOR)	S/(N + D)	70	75	–	dB
Current settling time to ± 1 LSB	t_{cs}	–	0.5	–	μs
Input bit rate at data input (pin 3)	BR	–	–	6.4	Mbits/s
Clock frequency at clock input (pin 1)	f_{BCK}	–	–	6.4	MHz
Full scale temperature coefficient at analogue outputs (AOL; AOR)	TC_{FS}	–	$\pm 400 \times 10^{-6}$	–	K^{-1}
Operating ambient temperature range	T_{amb}	–30	–	+ 85	°C
Total power dissipation	P_{tot}	–	250	–	mW
Bias current	I_{bias}	–0.5	–	1.8	mA

PACKAGE OUTLINE

8-lead DIL; plastic (SOT97).



(1) Optional.
(2) 2 x 1/2 NE5532.

Fig. 1 Block diagram.

PINNING

1	BCK	bit clock input
2	WS	word select input
3	DATA	data input
4	GND	ground
5	V_{DD}	+ 5 V supply voltage
6	AOL	left channel output
7	V_{ref}	reference voltage output
8	AOR	right channel output

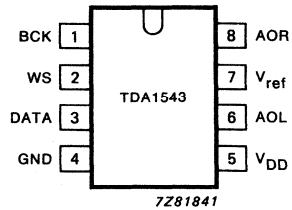
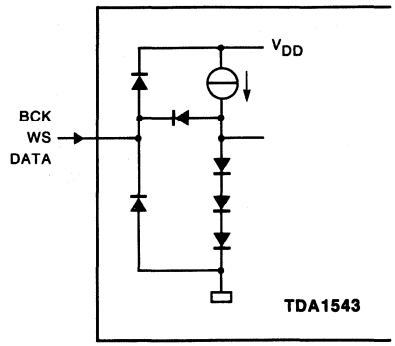
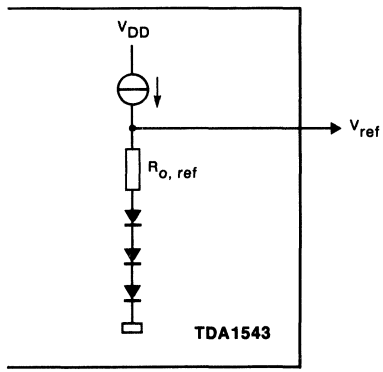


Fig. 2 Pinning diagram.

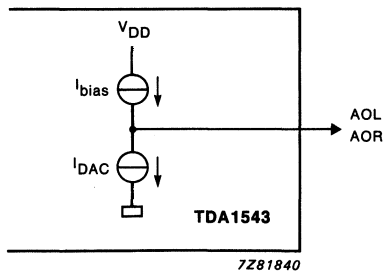
DEVELOPMENT DATA



(a) input pins BCK, WS and DATA.



(b) output pin V_{ref}.



(c) output pins AOL and AOR.

Fig. 3 Circuits at the input and output pins.

FUNCTIONAL DESCRIPTION

The TDA1543 accepts input serial data formats in two's complement with any bit length. Left and right data words are time multiplexed. The most significant bit (bit 1) must always be first. The format of data input is shown in Fig. 4.

This flexible input data format (I^2S) allows easy interfacing with signal processing chips such as interpolation filters, error correction circuits and audio signal processors (ASP).

The high maximum input bit-rate and fast settling current facilitates application in 4 x oversampling systems. An adjustable current is added to the output currents to bias output operational amplifiers (OP1; OP2) for maximum dynamic range (see Fig. 1).

With a LOW level on the word select (WS) input data is placed in the left input register and with a HIGH level on the WS input data is placed in the right input register. The data in the input registers is simultaneously latched in the output registers which control the bit switches.

The output current of the DAC is a sink current. The current I_{ref} at the V_{ref} output is adjusted by a resistor or a current source. The current I_{ref} is amplified with gain A_{Ibias} to the bias currents (I_{BL}; I_{BR}) which are added to the output currents.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	0	9	V
Crystal temperature	T_{XTAL}	–	150	°C
Storage temperature range	T_{stg}	−65	+ 150	°C
Operating ambient temperature range	T_{amb}	−30	+ 85	°C
Electrostatic handling *	V_{es}	−1000	+ 1000	V

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$		110	K/W

DEVELOPMENT DATA

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = + 25 °C; I_{ref} = 0; measured in the circuit of Fig. 1; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_{DD}	3.0	5.0	8.0	V
Supply current	note 1	I_{DD}	–	50	60	mA
Ripple rejection	note 2	RR	–	*	–	dB
Inputs						
Input current pins (1, 2 and 3)						
digital inputs LOW	V_I = 0.8 V	I_{IL}	–	–	–0.4	mA
digital inputs HIGH	V_I = 2.0 V	I_{IH}	–	–	20	μA
Input frequency/bit rate						
clock input pin 1		f_{BCK}	–	–	6.4	MHz
bit rate data input pin 3		BR	–	–	6.4	Mbits/s
word select input pin 2		f_{WS}	–	–	200	kHz
Input capacitance of digital inputs		C_I	–	*	–	pF
Analogue outputs (AOL; AOR)						
Resolution		Res	–	–	16	bits
Output voltage compliance						
AC		$V_{OC(AC)}$	–	± 25	–	mV
DC		$V_{OC(DC)}$	1.8	–	V_{DD}–1.2	V
Full scale current		I_{FS}	1.6	2.0	2.4	mA
Full scale temperature coefficient		TC_{FS}	–	$\pm 400 \times 10^{-6}$	–	K^{-1}
Offset current	I_{ref} = 0	I_{offset}	–0.1	0	0.1	mA
Bias current (adjustable)		I_{bias}	–0.5	–	1.8	mA
Bias current gain		AI_{bias}	1.9	2.0	2.1	

* Value to be fixed.

parameter	conditions	symbol	min.	typ.	max.	unit
Analogue output (V_{ref})						
Reference voltage output		V_{ref}	*	2.3	*	V
Reference current output		I_{ref}	−0.3	−	0.9	mA
Reference output impedance		$R_{o,\ ref}$	−	250	−	Ω
Signal-to-noise ratio (including THD)	note 3, Fig. 4	S/(N + D)	70	75	−	dB
Settling time ± 1 LSB		t_{cs}	−	0.5	−	μs
Channel separation		α	−	90	−	dB
Unbalance between outputs	note 3	$\|d_{IO}\|$	−	< 0.2	0.5	dB
Time delay between outputs		t_d	−	< 0.2	−	μs
Signal-to-noise ratio at bipolar zero	note 4	S/N	90	95	−	dB
Timing	Fig. 5					
Rise time		t_r	−	−	32	ns
Fall time		t_f	−	−	32	ns
Bit clock cycle time		t_{CY}	156	−	−	ns
Bit clock HIGH time		t_{HB}	46	−	−	ns
Bit clock LOW time		t_{LB}	46	−	−	ns
Data set-up time		$t_{SU;\ DAT}$	32	−	−	ns
Data hold time to bit clock		$t_{HD;\ DAT}$	0	−	−	ns
Word select hold time		$t_{HD;\ WS}$	0	−	−	ns
Word select set-up time		$t_{SU;\ WS}$	32	−	−	ns

DEVELOPMENT DATA

Notes to the characteristics

1. Measured at I_{AOL} = 0 mA and I_{AOR} = 0 mA (code 8000H) and I_{bias} = 0 mA.
2. V_{ripple} = 1% of supply voltage and f_{ripple} = 100 Hz.
3. With 1 kHz full scale sinewave generated at a sampling rate of 192 kHz.
4. At code 0000H.

* Value to be fixed.

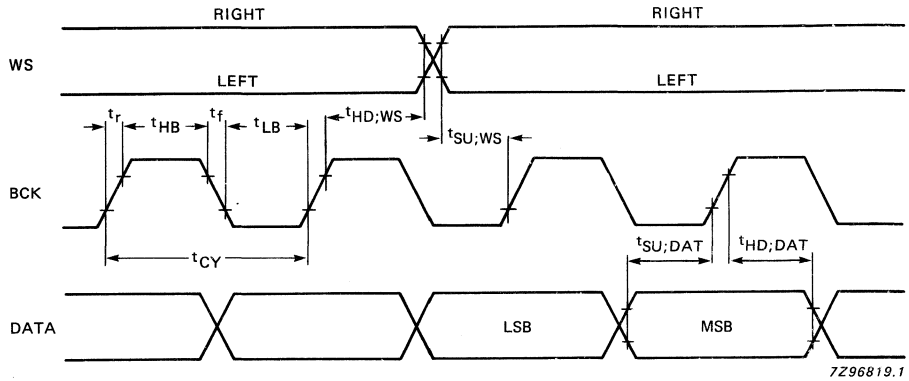


Fig. 4 Format of input signals (I^2S format).

PAL — NTSC ENCODER

GENERAL DESCRIPTION

The TDA2501 encodes two colour-difference signals R-Y and B-Y onto one subcarrier. Quadrature modulation allows the coding to be in accordance with either the PAL or NTSC system.

Features

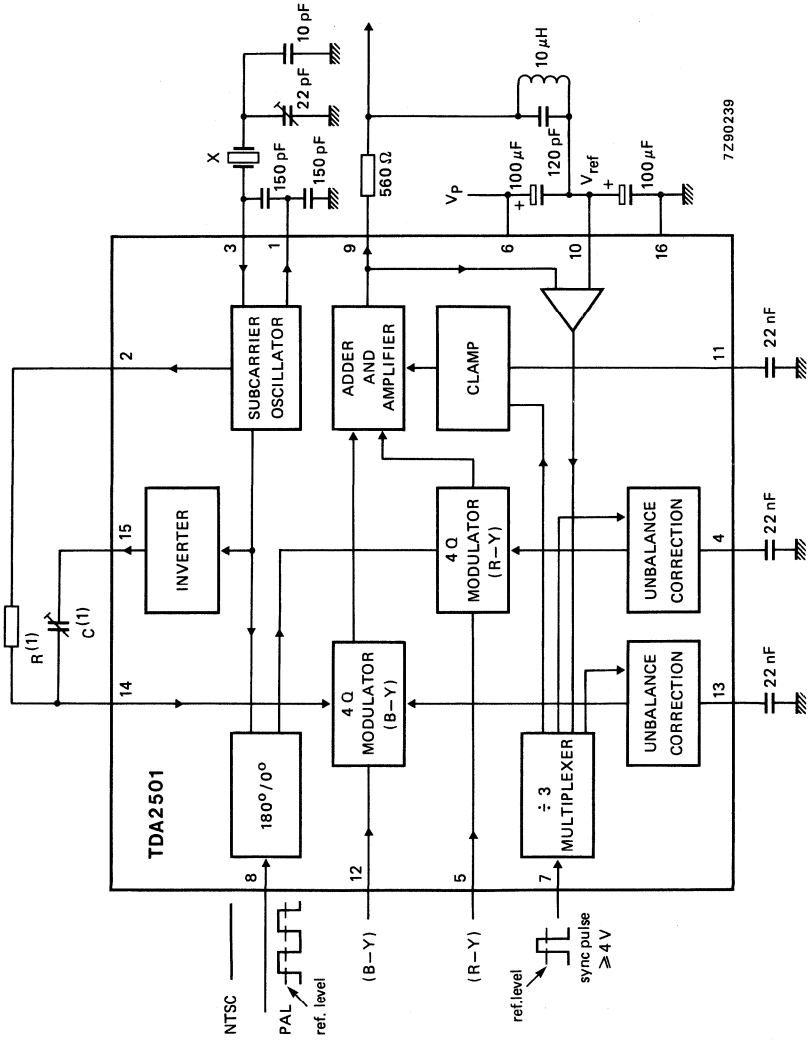
- Generates two sinusoidal subcarriers with a relative phase of 90° (also accepts external subcarriers)
- Modulates the two subcarriers with the colour difference signals
- Inverts the output from one modulator on command of an external signal (as in case of PAL)
- Sums the output from the modulators to obtain a quadrature modulated output signal
- Clamps the output DC level to a reference voltage
- Divides the frequency of horizontal sync pulses by three so that the output level can be clamped and the balance of the two modulators sequentially controlled during the line-blanking minus burst-key period

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range (pin 6)	V_P	5.5	6.8	10	V
Supply current range (pin 6)	I_P	28	40	64	mA
Chrominance output voltage (pin 9) (peak-to-peak value)	$V_{9(p-p)}$	–	–	1.4	V
Operating ambient temperature range	T_{amb}	−25	–	+70	°C

PACKAGE OUTLINES

TDA2501 : 16-lead DIL; plastic (with internal heat spreader) (SOT38).
TDA2501T: 16-lead mini-pack; plastic (SO16L; SOT162A).



(1) R = 0.885 (2 π fC); for PAL f = 4.433 619 MHz, R = 963 Ω and C = 33 pF.

Fig.1 Block diagram; also test and application diagram.

DESCRIPTION

The colour difference signals B-Y and R-Y with a maximum amplitude of 1.4 volt are to be applied at pin 12 and pin 5. DC-coupling of the input signals is allowed if their DC levels are within specified limits from the DC level at pin 10 (V_{ref}). The following table shows these limits as a function of supply voltage. The table also shows the limits of the reference voltage range as a function of the supply voltage.

supply voltage V_{6-16} (V)	input DC (R-Y) (B-Y) min. (V)*	V_{5-16} V_{12-16} (V) max. (V)**	reference voltage ▲ V_{10-16} (V)		
			min	typ.	max.
5.5	2.4	3.3	2.3	3.0	3.5
6.0	$> V_{ref} - 1.4$ V	3.8	2.4	3.3	3.9
7.0	$> V_{ref} - 1.4$ V	4.8	2.6	4.0	4.7
8.0	$> V_{ref} - 1.4$ V	5.8	2.8	4.8	5.5
9.0	$> V_{ref} - 1.4$ V	6.8	3.0	5.5	6.3
10.0	$> V_{ref} - 1.4$ V	7.8	3.2	6.3	7.1

* Minimum 2.4 V.
** At $V_S - 2.2$ V.
▲ Minimum values at $0.2\ V_S + 1.2$ V.
Typical values without pull-up or pull-down resistor.
Maximum values at $0.8\ V_S - 0.9$ V.

The inputs (B-Y) and (R-Y) should be zero, independent of their (limited) DC-levels, during the line-blanking minus burst-key period (LB – BK). Clamping the output and correcting the out-of-balance of the modulators, is achieved by applying a HIGH level to pin 7 within the (LB–BK) period (e.g. line sync pulse).

Modulation at output:
V_8 = LOW; output = sc x (B-Y) + sc' x (R-Y)
V_8 = HIGH; output = sc x (B-Y) – sc' x (R-Y)
in which sc' = subcarrier
sc = 90° phase-shifted subcarrier to sc' (sc lags).

The bandpass filter at the output suppresses the DC components of the (R-Y) + (B-Y) signal. Luminance (Y) is not processed by this circuit.

Internal subcarrier

The internal subcarrier oscillator is crystal controlled. The oscillator generates a sinewave with low harmonic distortion and an amplitude of about 500 mV peak-to-peak. The amplitude can be changed if necessary with a current input at pin 1. The adjustment range is 0 to 800 mV, with a corresponding current range of +250 to –150 μA.

Phase shift

To obtain a 90° phase-shifted carrier, two low impedance subcarrier outputs are provided, pins 2 and 15, the last being the inverse of the first. Between pins 2 and 15 an external RC combination must be used to obtain the desired 90° shift. The capacitor value must be limited to 33 pF to minimize subcarrier distortion.

The resistor required between pins 2 and 14 is 0.885 (2π fC).

External subcarrier

The (B-Y) and (R-Y) signals can also be multiplied with an external subcarrier. In this event the external subcarrier is connected to pin 1. For maximum input impedance at pin 1 $V_3 = V_{16}$ ($Z_{mi} > 1400\ \Omega$). The same RC network generates the 90° phase-shifted subcarrier. For the use of an externally generated subcarrier, applied at pin 14, the DC level must be the same as that of an RC-network generated one.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 6 to pin 16)	V_P	–	13.2	V
Total power dissipation	P_{tot}	see Fig.2		W
Operating ambient temperature range	T_{amb}	−25	+70	°C
Storage temperature range	T_{stg}	−65	+150	°C

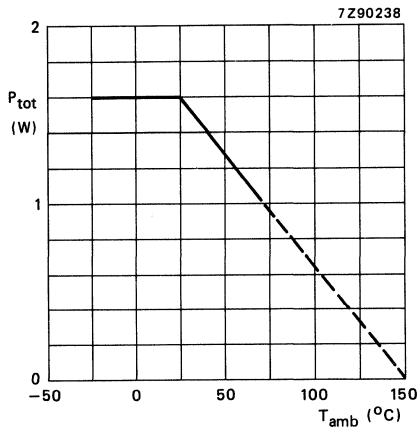


Fig.2 Power derating curve.

CHARACTERISTICS

$V_P = V_{6-10} = -V_{16-10} = 3$ V; $T_{amb} = 25$ °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Single supply voltage	V_{6-16}	5.5	6.8	10	V
Dual supply voltage					
positive (pin 6)	V_{6-10}	2.0	3.0	5.0	V
negative (pin 16)	$-V_{16-10}$	2.3	3.0	5.0	V
Supply current (pin 10)	I_{10}	−1	0	3.5	mA
positive (pin 6)	I_6	28	40	64	mA
negative (pin 16)	$-I_{16}$	28	40	64	mA
Limitation DC level					
oscillator feedback	V_1	−30	0	+30	mV
Nominal amplitude input signal (peak-to-peak value)					
pin 5	$V_{5(p-p)}$	–	1	1.4	V
pin 12	$V_{12(p-p)}$	–	1	1.4	V
Input voltages (R-Y) and (B-Y) zero DC level					
pin 5	V_5	2.4	3.3	3.9	V
pin 12	V_{12}	2.4	3.3	3.9	V
Required level of sync input					
HIGH	V_7	4	–	V_P	V
LOW	V_7	–	–	V_{10}	V
Required level of PAL pulse (H/2)					
HIGH	V_8	$V_{10}+0.8$	–	V_P	V
LOW	V_8	$-V_P$	–	0	V
Sync input current					
$V_7 = V_P + 1$ V	I_7	–	4	15	μA
PAL input current (H/2)					
$V_8 = V_{10} + 0.8$ V	I_8	–	1.5	5	μA
Chrominance output voltage swing (R-Y) = (B-Y) = 1.4 V; subcarrier pulse = 0.5 V (peak-to-peak value)	$V_{9(p-p)}$	–	–	1.4	V
Amplitude of suppressed subcarrier	V_9	0	7	16	mV
Input currents					
$V_4 = V_{10}$	I_4	0	1.5	5	μA
$V_{11} = V_{10}$	I_{11}	0	1.5	5	μA
$V_{13} = V_{10}$	I_{13}	0	1.5	5	μA
$V_5 = V_{10}$	I_5	0	9	30	μA
$V_{12} = V_{10}$	I_{12}	0	9	30	μA
$V_{14} = V_{16} + 2.3$ V	I_{14}	–	6	–	μA
Input impedance					
(R-Y)	Z_5	–	160	–	kΩ
(B-Y)	Z_{12}	–	160	–	kΩ

SECAM ENCODER

GENERAL DESCRIPTION

The TDA2506 converts colour-difference signals (D'_R and D'_B) into sequential, frequency modulated signals according to the SECAM system. The signals (D'_R) and (D'_B) are the colour difference signals before low-frequency pre-emphasis; D'_R = -1,9 (R-Y) and D'_B = ∓1,5(B-Y). The circuit is intended for use in video cameras, games, recorders and players, PAL-SECAM transcoding circuits and SECAM test signal generators.

Synchronizing pulses required for operation of the TDA2506 may be obtained from a universal sync generator SAA1043 or other pulse generator. All pulses are to be active HIGH and are as follows:

Horizontal sync pulses to pin 11
Half-rate horizontal sync (H/2) pulses to pin 9
Vertical sync pulses to pin 12
Chrominance blanking pulses to pin 13 (may include colour-killer pulses)

Frequency modulation is performed in conjunction with modulator-controller TDA2507.

Features

- Chrominance processor
- Vertical identification signal generator
- Timing pulse output to TDA2507
- Sample and hold circuit for control signal from TDA2507
- No adjustments of external components required (except high-frequency pre-emphasis (bell filter) stage)

QUICK REFERENCE DATA

Supply voltage	V_{4-2}	typ.	5 V
Supply current	I_4	typ.	45 mA
Reference voltage	V_{7-2}, V_{22-24}	typ.	3,5 V
Operating ambient temperature range	T_{amb}	−25 to	+70 °C
Storage temperature range	T_{stg}	−65 to	+150 °C

PACKAGE OUTLINES

24-lead DIL; plastic (with internal heat spreader) (SOT101B).

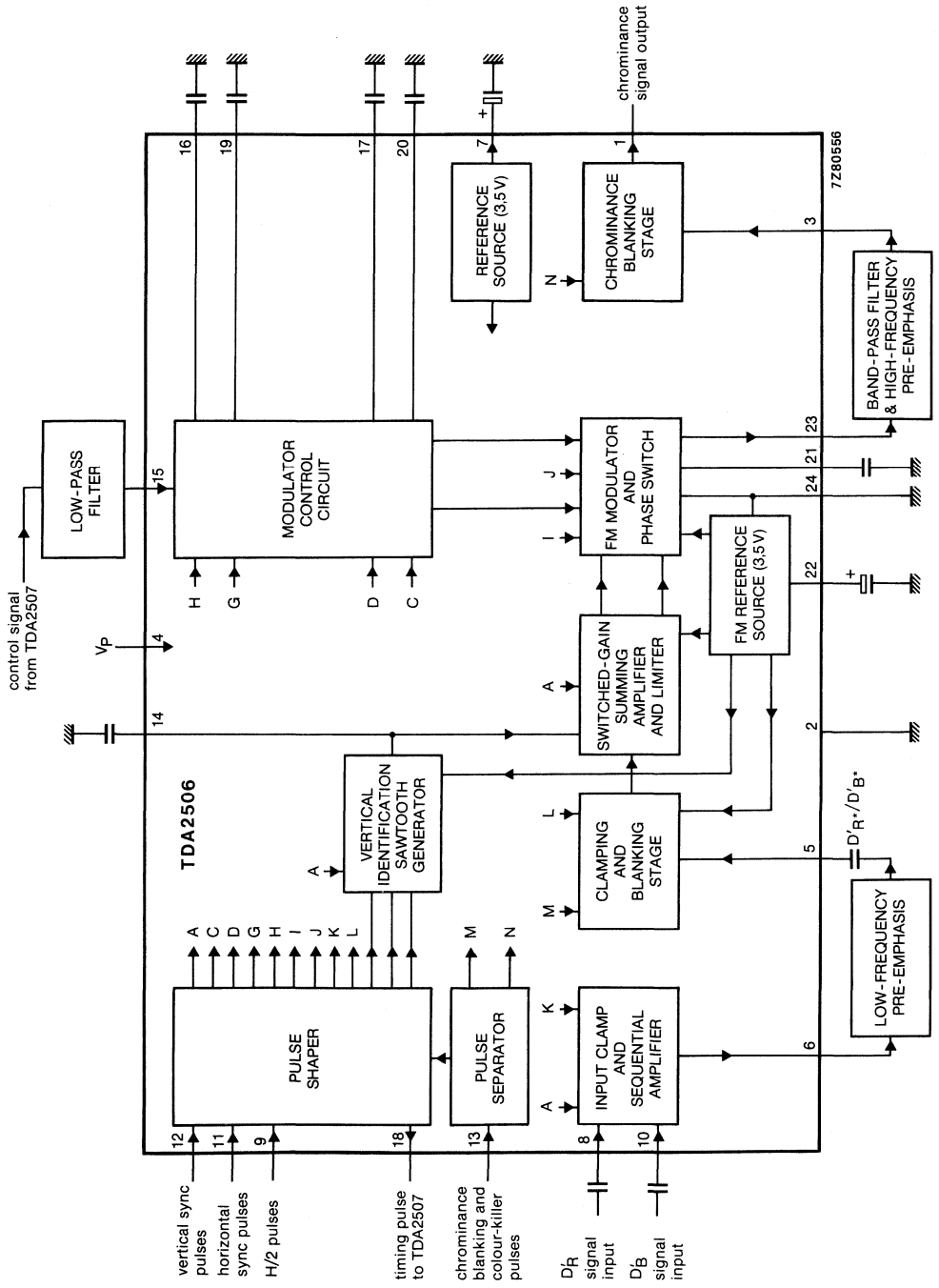


Fig. 1 Block diagram.

Pin functions

1. Chrominance signal output.
2. Ground.
3. Input to chrominance blanking stage from high-frequency pre-emphasis and band-pass filter.
4. Positive supply voltage.
5. Input to clamping and blanking stage from low-frequency pre-emphasis filter.
6. Output from sequential amplifier to low-frequency pre-emphasis filter.
7. Reference voltage output.
8. D'_R signal input.
9. H/2 pulse input (required only if specific phase sequencing is desired).
10. D'_B signal input.
11. Horizontal sync pulse input.
12. Vertical sync pulse input.
13. Chrominance blanking and colour-killer pulse input.
14. Capacitor for vertical identification sawtooth.
15. Control signal input from TDA2507 via low-pass filter.
16. 4 406,250 kHz frequency adjustment.
17. (R-Y) control.
18. Timing pulse output to TDA2507.
19. 4 250,000 kHz frequency adjustment.
20. (B-Y) control.
21. FM modulator tuning capacitor (fixed).
22. FM reference voltage output.
23. FM modulator output to high frequency pre-emphasis and band-pass filter.
24. Ground connection for FM modulator.

FUNCTIONAL DESCRIPTION

Input clamp and sequential amplifier

This circuit clamps the zero levels of the D'_R and D'_B input signals (pins 8 and 10) to the reference voltage from pin 7. The input signals are switched into the amplifier sequentially by an internally delayed H/2 waveform. The amplifier output at pin 6 is D'_R when the delayed H/2 waveform is HIGH and D'_B when it is LOW. The stage gain is 1,5.

Clamping and blanking stage

After external low-frequency pre-emphasis, the sequential $D'_R{}^*$ and $D'_B{}^*$ signals are returned to the IC at pin 5. The signal amplitude at pin 5 is typically 0,5 V (peak-to-peak value) for 75% colour bar (EBU). Black levels are clamped to the FM reference voltage (pin 22). Blanking takes place during the chrominance blanking pulse and, if required, during the video blanking and/or colour killing pulses.

FUNCTIONAL DESCRIPTION (continued)

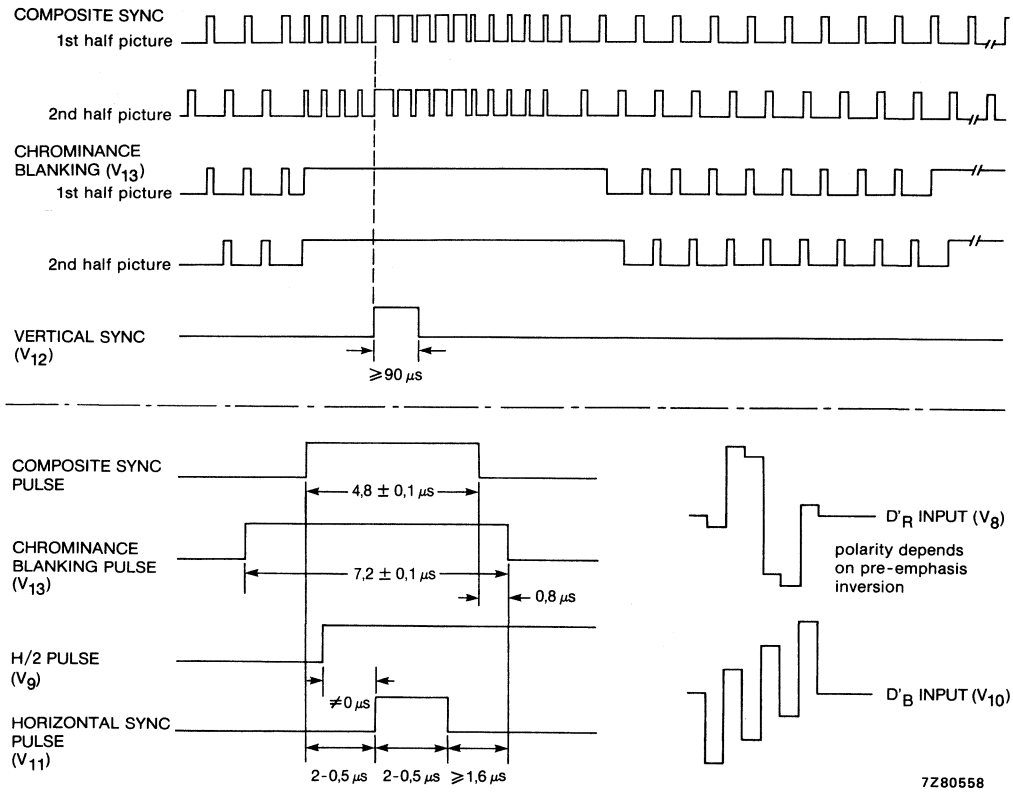


Fig. 2 Survey of input signals in relation to composite sync.

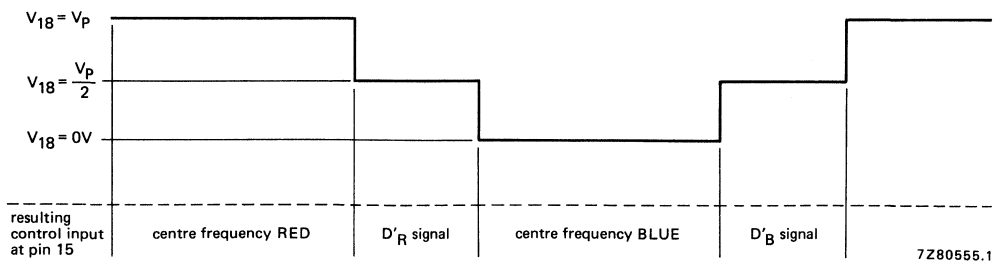


Fig. 3 Timing pulse output (pin 18) and resulting control input (pin 15).

Switched-gain summing amplifier and limiter

Inputs into the summing amplifier are the sequential D'_R* and D'_B* signals, the vertical identification sawtooth waveform and reference d.c. levels. The gain of the amplifier is switched by the internally delayed H/2 waveform to give the correct input amplitudes for the FM modulator (D'_R* gain = 280/230 x D'_B* gain). An offset is also introduced between the black levels of the D'_R* and D'_B* signals which corresponds to the upper and lower thresholds of the limiter.

FM modulator and phase switch

The FM modulator provides accurate FM modulation which follows the amplitude envelopes of the sequential D'_R* and D'_B* waveforms. The centre frequencies of 4 406,250 kHz for the D'_R* signal and 4 250,000 kHz for the D'_B* signal are controlled by d.c. levels from the sample and hold circuit (which in turn are controlled by the TDA2507). The upper and lower frequency limits are 4 756,000 ± 35 kHz and 3 900,000 ± 35 kHz.

Reference d.c. levels are switched within the FM modulator to define the starting phase of the modulator output (pin 23) at the initiation of each horizontal and vertical scan. The starting phase sequence is as follows:

vertical scan (frame to frame) 0^o, 180^o, 0^o, 180^o, repeating;

horizontal scan (line to line) 0^o, 0^o, 180^o, 0^o, 0^o, 180^o, repeating.

Chrominance blanking stage

The frequency modulated colour difference signals are passed via high-frequency pre-emphasis and band-pass filters to the chrominance blanking input at pin 3. The d.c. level of this input should be equal to the reference voltage at pin 7. Blanking occurs during the chrominance blanking pulse. The stage gain is 1,75.

Vertical identification sawtooth generator

Vertical sync, horizontal sync and chrominance blanking pulses are used to determine vertical identification (see Fig. 4). The vertical identification sawtooth generator is driven in opposite directions for identification signals IdR and IdB; the capacitor for the generator is connected at pin 14. If no vertical identification is required, pin 14 should be connected to the FM reference voltage at pin 22.

Pulse shaper

This stage developes all pulses that are required within the TDA2506 and also the timing pulses required for the modulator controller TDA2507 (see Fig. 3). Internal H/2 pulses are generated by a flip-flop working from the horizontal sync input (pin 11), this makes the H/2 input at pin 9 necessary only if it is required to lock the modulator into a specific phase sequence. If the H/2 input is not required, pin 9 should be connected to ground. A pulse separator at the chrominance blanking/colour-killer input (pin 13) allows this input to be used for blanking the sequential D'_R*/D'_B* signal.

Sample and hold circuit

This circuit provides reference voltages to the FM modulator which set the centre modulation frequencies for the sequential D'_R* and D'_B* signals. The reference voltage levels are supplied to pin 15 from the TDA2507 in a sequence that is time-related to D'_R*/D'_B* switching. The levels are sampled and then held for D'_R* using capacitors at pins 16 and 17, and for D'_B* using capacitors at pins 19 and 20.

FUNCTIONAL DESCRIPTION (continued)

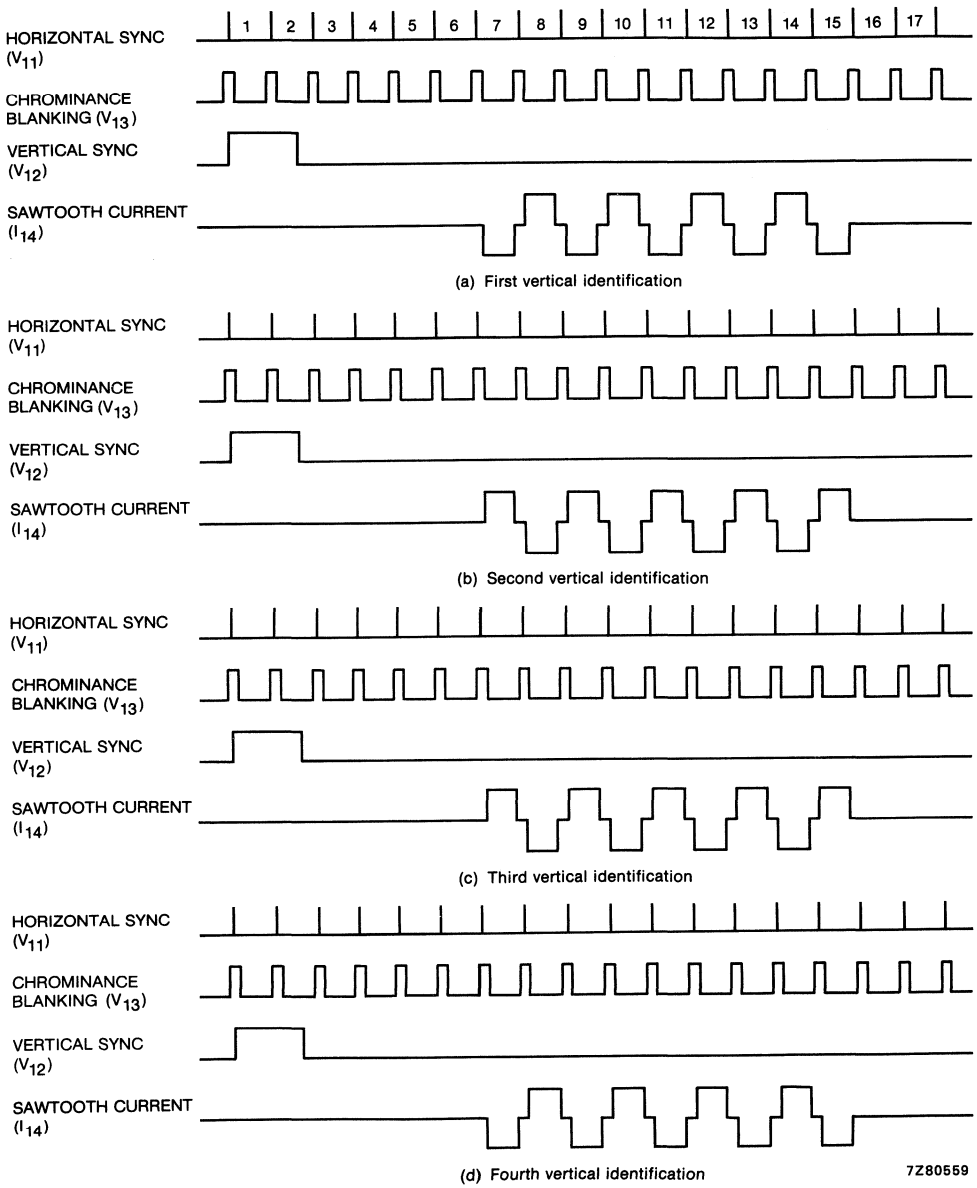


Fig. 4 Vertical identification generation.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating system IEC 134

Supply voltage	V_{4-1}	max. 13,2 V
Total power dissipation	P_{tot}	see Figs 5 and 6
Operating ambient temperature range	T_{amb}	−25 to +70 °C
Storage temperature range	T_{stg}	−65 to +150 °C

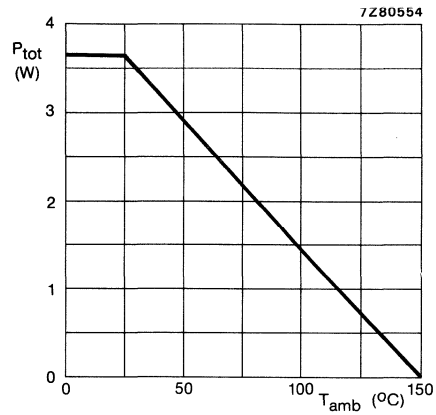


Fig. 5 Power derating curve for DIL package (SOT-101B).

CHARACTERISTICS

$V_p = V_{4-2} = 5$ V; $T_{amb} = 25$ °C; all voltages are with reference to ground (pins 2 and 24); all currents stated are positive into the IC; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage (pin 4)	$V_p = V_{4-2}$	4,75	5	7	V
Supply current	$I_p = I_4$	30	45	60	mA
Reference voltage (pin 7)	V_{7-2}	3,35	3,5	3,65	V
Reference voltage (pin 22)	V_{22-24}	3,35	3,5	3,65	V
Pulse shaper (pins 9,11 and 12, emitter follower inputs; pin 18, collector output)					
Bias current (pin 9,11,12)	I_9, I_{11}, I_{12}	–	–	10	μA
Input resistance (pin 9,11,12)	R_9, R_{11}, R_{12}	200	–	–	kΩ
Input pulse amplitude (pin 9,11,12)	V_9, V_{11}, V_{12}	2	–	–	V
Timing pulse output (pin 18) high level	V_{18}	4,7	–	–	V
intermediate ($V_p/2$) level	V_{18}	2,3	–	2,7	V
low level	V_{18}	–	–	0,3	V
Pulse separator (pin 13, emitter follower)					
Input resistance	R_{13}	100	–	–	kΩ
Chrominance blanking pulse amplitude	V_{13}	3,6	–	–	V
D'_R*/D'_B* blanking pulse amplitude (colour killing)	V_{13}	1,7	1,8	1,9	V
Vertical identification sawtooth generator (pin 14)					
Voltage clamping level	V_{14}	V_{22}–7 mV	V_{22}	V_{22}+7 mV	V
Ramp current (occurs in lines 7 to 15 after vertical sync)	$\pm I_{14}$	50	70	85	μA
Maximum voltage level	V_{14}	V_{22}+0,6	V_{22}+0,7	V_{22}+0,8	V
Minimum voltage level	V_{14}	V_{22}–0,8	V_{22}–0,7	V_{22}–0,6	V
Voltage level during line blanking	V_{14}	V_{22}–7 mV	V_{22}	V_{22}+7 mV	V
Inputs D'_R*, D'_B* (pins 8 and 10)					
Signal level during clamping ($I_8, I_{10} = \pm 50$ μA)	V_8, V_{10}	V_7–20 mV	V_7	V_7+20 mV	V
Input bias current	I_8, I_{10}	–	–	1,5	μA

parameter	symbol	min.	typ.	max.	unit
Sequential amplifier output (pin 6)					
(Pins 8 and 10 a.c. coupled to fixed d.c. voltage)					
D.C. output	V_6	1,6	$\frac{V_7}{2}$ – 10 mV	1,85	V
Output resistance	R_6	–	12	16	Ω
Amplifier voltage gain (pin 8 or 10 to pin 6)	$G_{8,10\text{-}6}$	1,46	1,5	1,54	
Clamping and blanking stage (pin 5)					
Input voltage (clamped; $I_5 = \pm 50\ \mu A$)	V_5	V_{22} – 10 mV	V_{22}	V_{22} + 10 mV	V
Input bias current	I_5	–	–	1,0	μA
Modulator control circuit (pin 15, buffer amplifier non-inverting input)					
Bias current	I_{15}	–	–	1,25	μA
Permitted input signal d.c. levels	V_{15}	2	–	4,3	V
FM modulator output (pin 23, emitter follower)					
Output resistance	R_{23}	–	50	70	Ω
High d.c. output level at $V_{21} = 4$ V	V_{23}	V_{22} – 0,85	–	V_{22} – 0,7	V
Output signal amplitude	V_{23}	0,9	1,0	1,1	V

CHARACTERISTICS (Continued)

parameter	symbol	min.	typ.	max.	unit
Chrominance blanking stage (pin 3, emitter follower input; pin 1, amplifier output)					
Input current	I_3	–	–	15	μA
Input resistance	R_3	300	–	–	kΩ
Required d.c. level of input signal	V_3	–	V_7	–	V
Output resistance	R_1	–	–	5	Ω
Temperature coefficient of output d.c. level	TC	–	1,8	–	mV/K
Amplifier gain	G_{3-1}	1,70	1,75	1,80	
Output d.c. level during blanking(V_{13} = HIGH)	V_1	V_7–0,76	V_7–0,70	V_7–0,60	V
Output d.c. level unblanked ($V_3 = V_7$; V_{13} = LOW)	V_1	V_7–0,76	V_7–0,70	V_7–0,60	V

A.C. CHARACTERISTICS

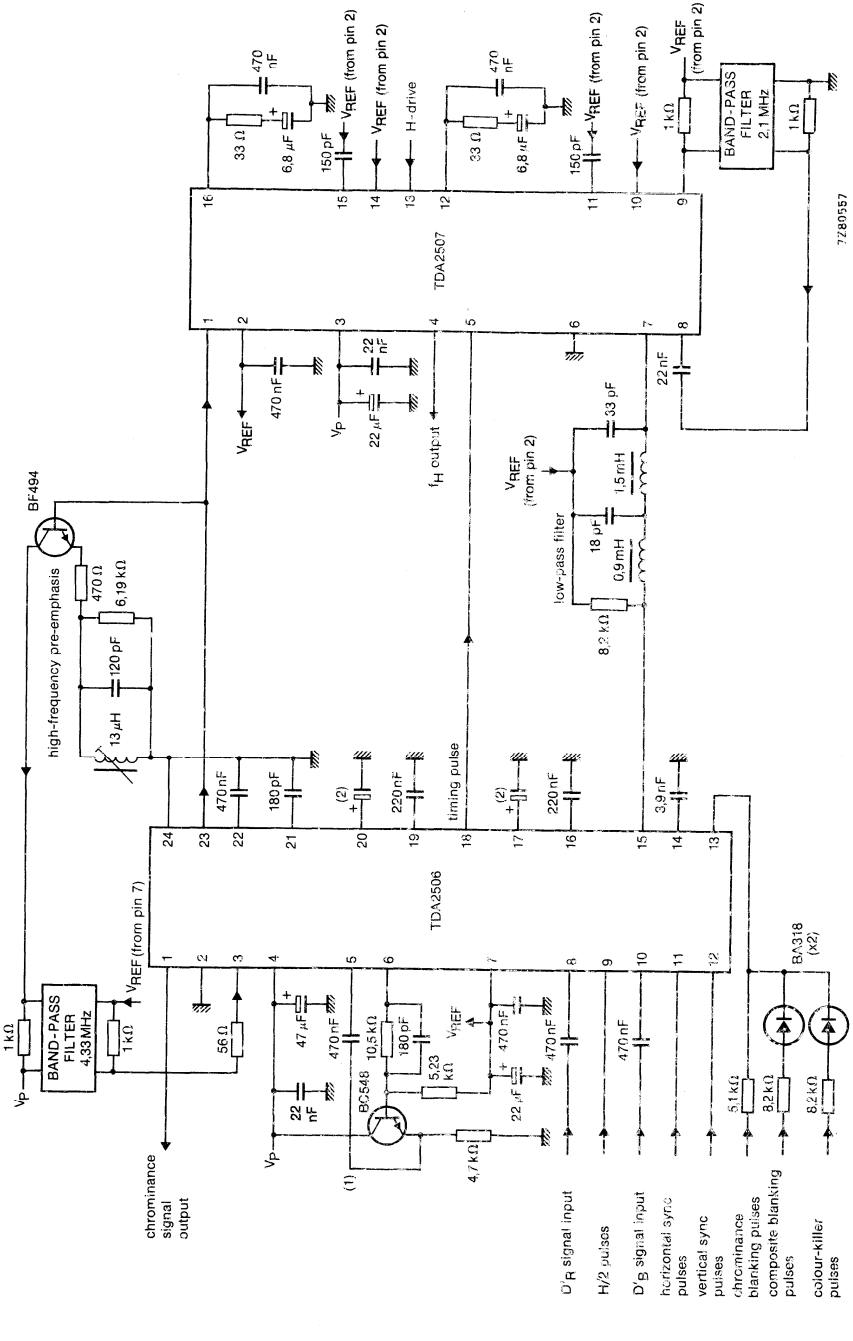
Values are valid for TDA2506 operating with TDA2507. Horizontal frequency (f_H) = 15 625 Hz.

parameter	symbol	min.	typ.	max.	unit
Centre frequency RED	f_{0R}	–	4 406,250 ± 2	–	kHz
Centre frequency BLUE	f_{0B}	–	4 250,000 ± 2	–	kHz
Ident. frequency RED *	f_{IdR}	–	4 756,250 ± 35	–	kHz
Ident. frequency BLUE *	f_{IdB}	–	3 900,000 ± 35	–	kHz
Minimum frequency RED **	$-f_R$	–	4 126,250 ± 10	–	kHz
Maximum frequency RED **	$+f_R$	–	4 686,250 ± 10	–	kHz
Minimum frequency BLUE **	$-f_B$	–	4 020,000 ± 10	–	kHz
Maximum frequency BLUE **	$+f_B$	–	4 480,000 ± 10	–	kHz

* The ident. frequencies are also the maximum and minimum output frequencies of the encoder.

** Values are valid for 75% colour bar saturation (EBU) (V_5 = ± 250 mV deviation from clamping level).

APPLICATION INFORMATION



(1) Signal amplitude for 75% colour bar (EBU) = 0,5 V (peak-to-peak value).
(2) For $V_P = 4{,}75$ to 5,3 V, $C_{17} = C_{20} = 0{,}68\ \mu F$; for $V_P > 5{,}3$ V, $C_{17} = C_{20} = 2{,}2\ \mu F$.

Fig. 6 Application using TDA2507 with PLL tuning: $V_P = 5$ V.

SECAM ENCODER

GENERAL DESCRIPTION

The TDA2506 converts colour-difference signals (D'_R and D'_B) into sequential, frequency modulated signals according to the SECAM system. The signals (D'_R) and (D'_B) are the colour difference signals before low-frequency pre-emphasis; $D'_R = -1{,}9\ (R-Y)$ and $D'_B = \pm 1{,}5(B-Y)$. The circuit is intended for use in video cameras, games, recorders and players, PAL-SECAM transcoding circuits and SECAM test signal generators.

Synchronizing pulses required for operation of the TDA2506 may be obtained from a universal sync generator SAA1043 or other pulse generator. All pulses are to be active HIGH and are as follows:

Horizontal sync pulses to pin 11
Half-rate horizontal sync (H/2) pulses to pin 9
Vertical sync pulses to pin 12
Chrominance blanking pulses to pin 13 (may include colour-killer pulses)

Frequency modulation is performed in conjunction with modulator-controller TDA2507.

Features

- Chrominance processor
- Vertical identification signal generator
- Timing pulse output to TDA2507
- Sample and hold circuit for control signal from TDA2507
- No adjustments of external components required (except high-frequency pre-emphasis (bell filter) stage)

QUICK REFERENCE DATA

Supply voltage	V_{4-2}	typ.	5 V
Supply current	I_4	typ.	45 mA
Reference voltage	V_{7-2}, V_{22-24}	typ.	3,5 V
Operating ambient temperature range	T_{amb}	−25 to +70	°C
Storage temperature range	T_{stg}	−65 to +150	°C

PACKAGE OUTLINES

24-lead mini-pack ; plastic (SO24; SOT137A).

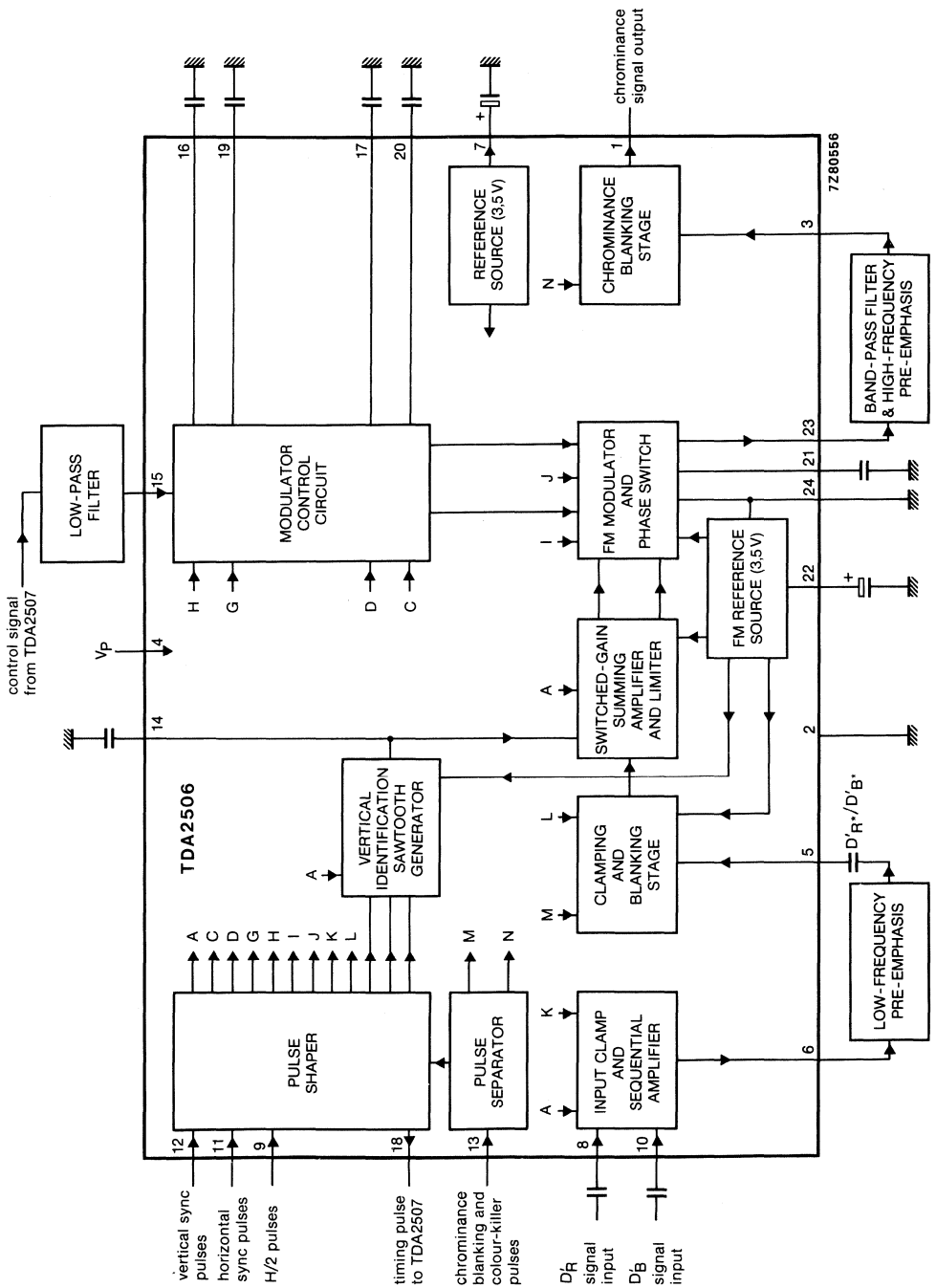


Fig. 1 Block diagram.

Pin functions

1. Chrominance signal output.
2. Ground.
3. Input to chrominance blanking stage from high-frequency pre-emphasis and band-pass filter.
4. Positive supply voltage.
5. Input to clamping and blanking stage from low-frequency pre-emphasis filter.
6. Output from sequential amplifier to low-frequency pre-emphasis filter.
7. Reference voltage output.
8. D'_R signal input.
9. H/2 pulse input (required only if specific phase sequencing is desired).
10. D'_B signal input.
11. Horizontal sync pulse input.
12. Vertical sync pulse input.
13. Chrominance blanking and colour-killer pulse input.
14. Capacitor for vertical identification sawtooth.
15. Control signal input from TDA2507 via low-pass filter.
16. 4 406,250 kHz frequency adjustment.
17. (R-Y) control.
18. Timing pulse output to TDA2507.
19. 4 250,000 kHz frequency adjustment.
20. (B-Y) control.
21. FM modulator tuning capacitor (fixed).
22. FM reference voltage output.
23. FM modulator output to high frequency pre-emphasis and band-pass filter.
24. Ground connection for FM modulator.

FUNCTIONAL DESCRIPTION

Input clamp and sequential amplifier

This circuit clamps the zero levels of the D'_R and D'_B input signals (pins 8 and 10) to the reference voltage from pin 7. The input signals are switched into the amplifier sequentially by an internally delayed H/2 waveform. The amplifier output at pin 6 is D'_R when the delayed H/2 waveform is HIGH and D'_B when it is LOW. The stage gain is 1,5.

Clamping and blanking stage

After external low-frequency pre-emphasis, the sequential D'_R* and D'_B* signals are returned to the IC at pin 5. The signal amplitude at pin 5 is typically 0,5 V (peak-to-peak value) for 75% colour bar (EBU). Black levels are clamped to the FM reference voltage (pin 22). Blanking takes place during the chrominance blanking pulse and, if required, during the video blanking and/or colour killing pulses.

FUNCTIONAL DESCRIPTION (continued)

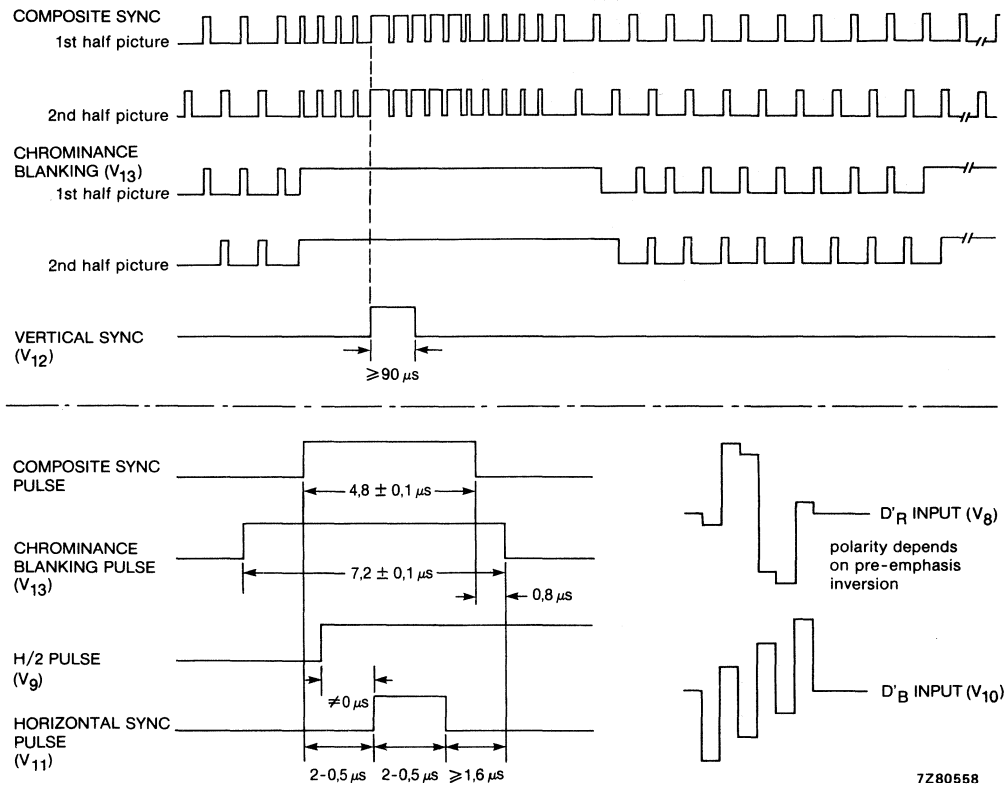


Fig. 2 Survey of input signals in relation to composite sync.

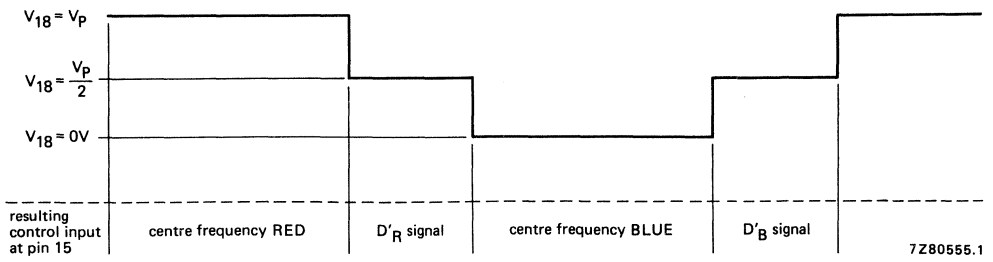


Fig. 3 Timing pulse output (pin 18) and resulting control input (pin 15).

Switched-gain summing amplifier and limiter

Inputs into the summing amplifier are the sequential D'_R* and D'_B* signals, the vertical identification sawtooth waveform and reference d.c. levels. The gain of the amplifier is switched by the internally delayed H/2 waveform to give the correct input amplitudes for the FM modulator (D'_R* gain = 280/230 x D'_B* gain). An offset is also introduced between the black levels of the D'_R* and D'_B* signals which corresponds to the upper and lower thresholds of the limiter.

FM modulator and phase switch

The FM modulator provides accurate FM modulation which follows the amplitude envelopes of the sequential D'_R* and D'_B* waveforms. The centre frequencies of 4 406,250 kHz for the D'_R* signal and 4 250,000 kHz for the D'_B* signal are controlled by d.c. levels from the sample and hold circuit (which in turn are controlled by the TDA2507). The upper and lower frequency limits are 4 756,250 ± 35 kHz and 3 900,000 ± 35 kHz.

Reference d.c. levels are switched within the FM modulator to define the starting phase of the modulator output (pin 23) at the initiation of each horizontal and vertical scan. The starting phase sequence is as follows:

vertical scan (frame to frame) 0^o, 180^o, 0^o, 180^o, repeating;

horizontal scan (line to line) 0^o, 0^o, 180^o, 0^o, 0^o, 180^o, repeating.

Chrominance blanking stage

The frequency modulated colour difference signals are passed via high-frequency pre-emphasis and band-pass filters to the chrominance blanking input at pin 3. The d.c. level of this input should be equal to the reference voltage at pin 7. Blanking occurs during the chrominance blanking pulse. The stage gain is 1,75.

Vertical identification sawtooth generator

Vertical sync, horizontal sync and chrominance blanking pulses are used to determine vertical identification (see Fig. 4). The vertical identification sawtooth generator is driven in opposite directions for identification signals IdR and IdB; the capacitor for the generator is connected at pin 14. If no vertical identification is required, pin 14 should be connected to the FM reference voltage at pin 22.

Pulse shaper

This stage developes all pulses that are required within the TDA2506 and also the timing pulses required for the modulator controller TDA2507 (see Fig. 3). Internal H/2 pulses are generated by a flip-flop working from the horizontal sync input (pin 11), this makes the H/2 input at pin 9 necessary only if it is required to lock the modulator into a specific phase sequence. If the H/2 input is not required, pin 9 should be connected to ground. A pulse separator at the chrominance blanking/colour-killer input (pin 13) allows this input to be used for blanking the sequential D'_R*/D'_B* signal.

Sample and hold circuit

This circuit provides reference voltages to the FM modulator which set the centre modulation frequencies for the sequential D'_R* and D'_B* signals. The reference voltage levels are supplied to pin 15 from the TDA2507 in a sequence that is time-related to D'_R*/D'_B* switching. The levels are sampled and then held for D'_R* using capacitors at pins 16 and 17, and for D'_B* using capacitors at pins 19 and 20.

FUNCTIONAL DESCRIPTION (continued)

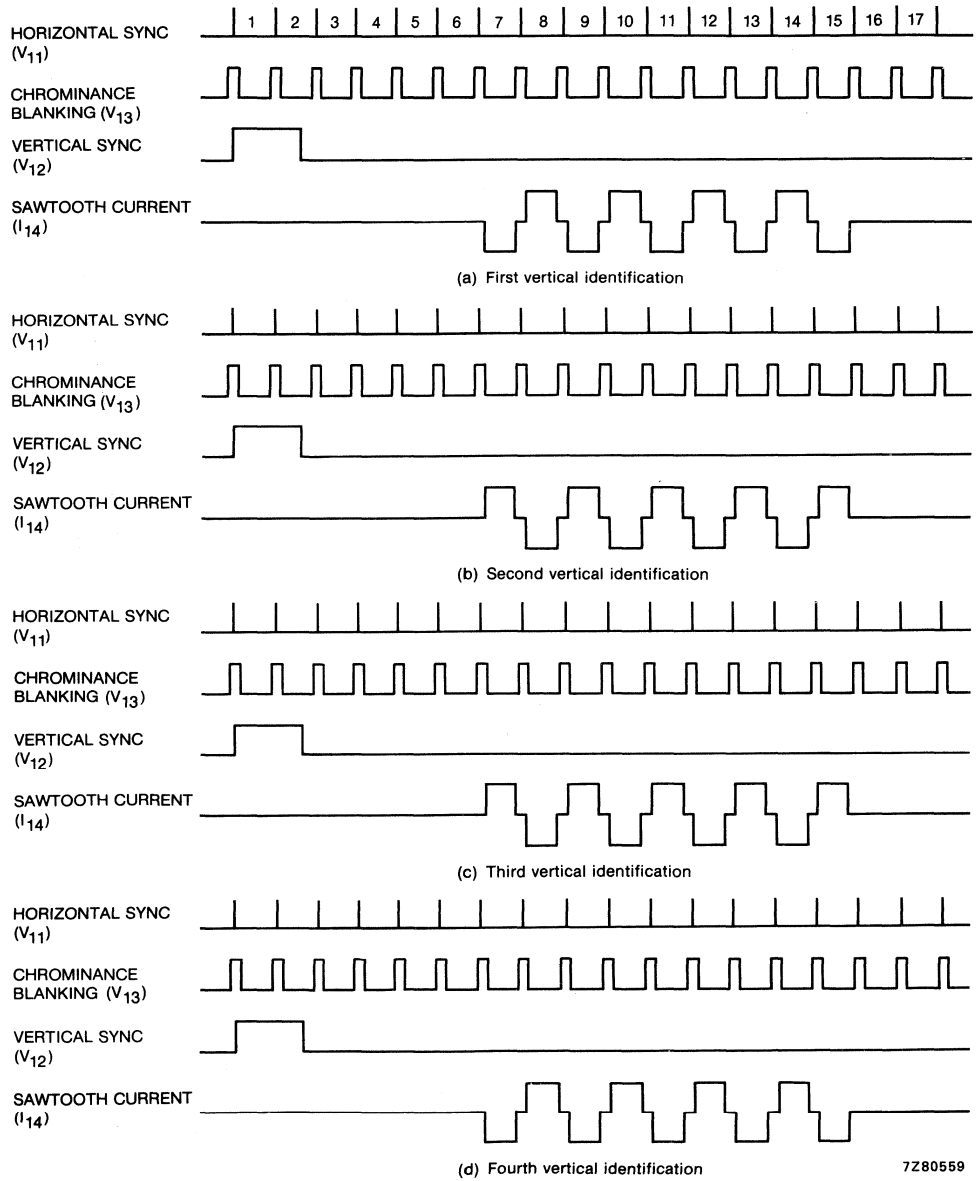


Fig. 4 Vertical identification generation.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating system IEC 134

Supply voltage	V_{4-1}	max. 13,2 V
Total power dissipation	P_{tot}	see Fig. 5
Operating ambient temperature range	T_{amb}	−25 to +70 °C
Storage temperature range	T_{stg}	−65 to +150 °C

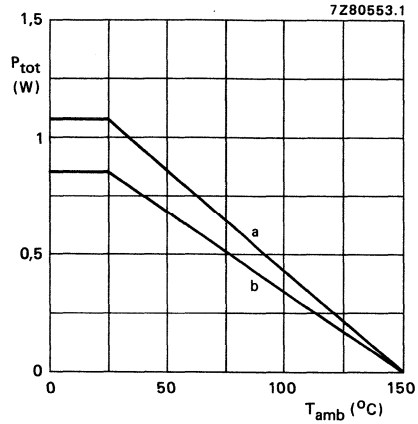


Fig. 5 Power derating curve.

a = device mounted on a ceramic substrate.
b = device mounted on a printed circuit board.

CHARACTERISTICS

$V_p = V_{4-2} = 5$ V; $T_{amb} = 25$ °C; all voltages are with reference to ground (pins 2 and 24); all currents stated are positive into the IC; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage (pin 4)	$V_p = V_{4-2}$	4,75	5	7	V
Supply current	$I_p = I_4$	30	45	60	mA
Reference voltage (pin 7)	V_{7-2}	3,35	3,5	3,65	V
Reference voltage (pin 22)	V_{22-24}	3,35	3,5	3,65	V
Pulse shaper (pins 9,11 and 12, emitter follower inputs; pin 18, collector output)					
Bias current (pin 9,11,12)	I_9, I_{11}, I_{12}	–	–	10	μA
Input resistance (pin 9,11,12)	R_9, R_{11}, R_{12}	200	–	–	kΩ
Input pulse amplitude (pin 9,11,12)	V_9, V_{11}, V_{12}	2	–	–	V
Timing pulse output (pin 18) high level	V_{18}	4,7	–	–	V
intermediate (V_p/2) level	V_{18}	2,3	–	2,7	V
low level	V_{18}	–	–	0,3	V
Pulse separator (pin 13, emitter follower)					
Input resistance	R_{13}	100	–	–	kΩ
Chrominance blanking pulse amplitude	V_{13}	3,6	–	–	V
D'_R*/D'_B* blanking pulse amplitude (colour killing)	V_{13}	1,7	1,8	1,9	V
Vertical identification sawtooth generator (pin 14)					
Voltage clamping level	V_{14}	V_{22}–7 mV	V_{22}	V_{22}+7 mV	V
Ramp current (occurs in lines 7 to 15 after vertical sync)	$\pm I_{14}$	50	70	85	μA
Maximum voltage level	V_{14}	V_{22}+0,6	V_{22}+0,7	V_{22}+0,8	V
Minimum voltage level	V_{14}	V_{22}–0,8	V_{22}–0,7	V_{22}–0,6	V
Voltage level during line blanking	V_{14}	V_{22}–7 mV	V_{22}	V_{22}+7 mV	V
Inputs D'_R*, D'_B* (pins 8 and 10)					
Signal level during clamping ($I_8, I_{10} = \pm 50$ μA)	V_8, V_{10}	V_7–20 mV	V_7	V_7+20 mV	V
Input bias current	I_8, I_{10}	–	–	1,5	μA

parameter	symbol	min.	typ.	max.	unit
Sequential amplifier output (pin 6)					
(Pins 8 and 10 a.c. coupled to fixed d.c. voltage)					
D.C. output	V_6	1,6	$\frac{V_7}{2}$ – 10 mV	1,85	V
Output resistance	R_6	–	12	16	Ω
Amplifier voltage gain (pin 8 or 10 to pin 6)	$G_{8,10\text{-}6}$	1,46	1,5	1,54	
Clamping and blanking stage (pin 5)					
Input voltage (clamped; $I_5 = \pm 50\ \mu A$)	V_5	V_{22} – 10 mV	V_{22}	V_{22} + 10 mV	V
Input bias current	I_5	–	–	1,0	μA
Modulator control circuit (pin 15, buffer amplifier non-inverting input)					
Bias current	I_{15}	–	–	1,25	μA
Permitted input signal d.c. levels	V_{15}	2	–	4,3	V
FM modulator output (pin 23, emitter follower)					
Output resistance	R_{23}	–	50	70	Ω
High d.c. output level at $V_{21} = 4$ V	V_{23}	V_{22} – 0,85	–	V_{22} – 0,7	V
Output signall amplitude	V_{23}	0,9	1,0	1,1	V

CHARACTERISTICS (Continued)

parameter	symbol	min.	typ.	max.	unit
Chrominance blanking stage (pin 3, emitter follower input; pin 1, amplifier output)					
Input current	I_3	–	–	15	μA
Input resistance	R_3	300	–	–	kΩ
Required d.c. level of input signal	V_3	–	V_7	–	V
Output resistance	R_1	–	–	5	Ω
Temperature coefficient of output d.c. level	TC	–	1,8	—	mV/K
Amplifier gain	G_{3-1}	1,70	1,75	1,80	
Output d.c. level during blanking(V_{13} = HIGH)	V_1	V_7–0,76	V_7–0,70	V_7–0,60	V
Output d.c. level unblanked ($V_3 = V_7$; V_{13} = LOW)	V_1	V_7–0,76	V_7–0,70	V_7–0,60	V

A.C. CHARACTERISTICS

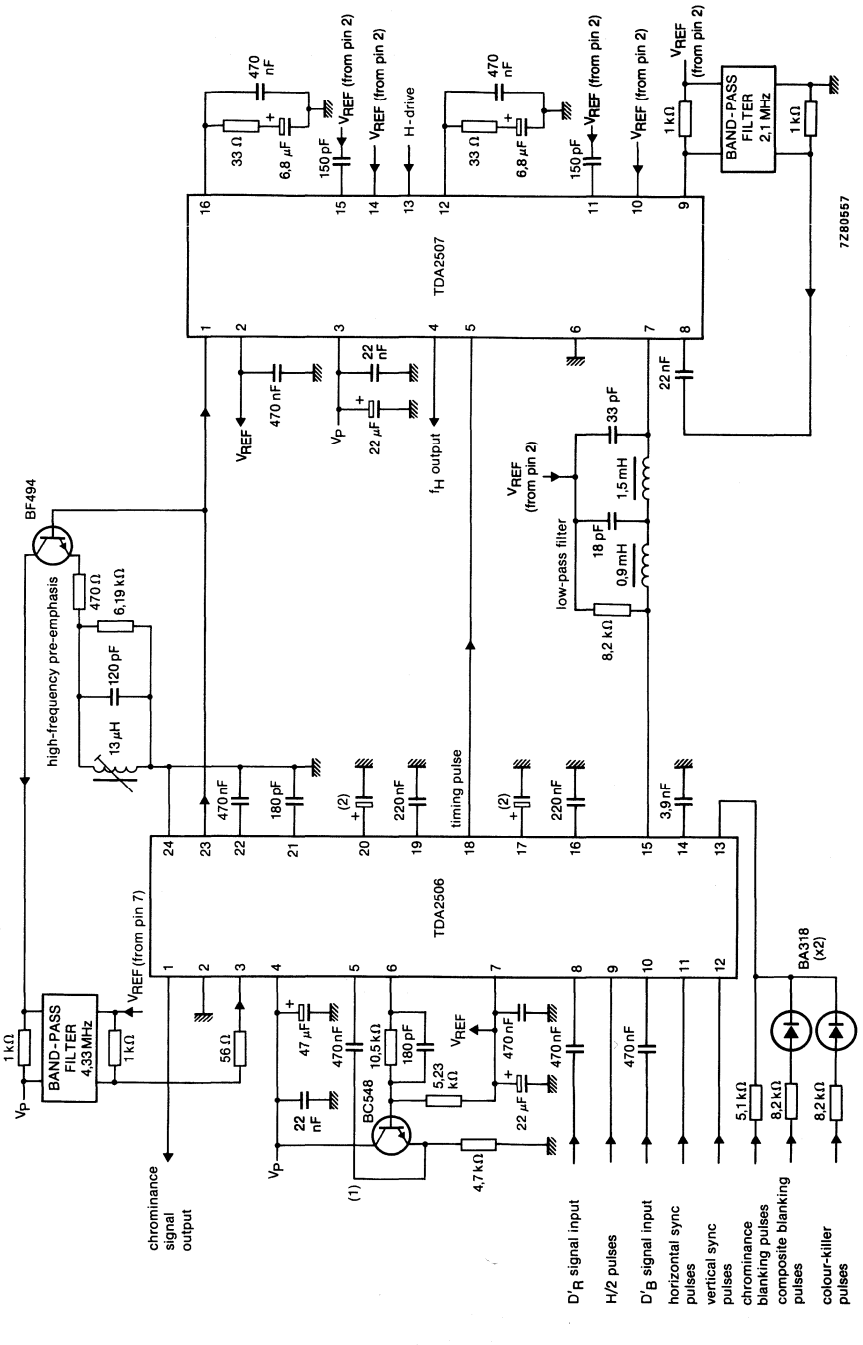
Values are valid for TDA2506 operating with TDA2507. Horizontal frequency (f_H) = 15 625 Hz.

parameter	symbol	min.	typ.	max.	unit
Centre frequency RED	f_{0R}	–	4 406,250 ± 2	–	kHz
Centre frequency BLUE	f_{0B}	–	4 250,000 ± 2	–	kHz
Ident. frequency RED *	f_{IdR}	–	4 756,250 ± 35	–	kHz
Ident. frequency BLUE *	f_{IdB}	–	3 900,000 ± 35	–	kHz
Minimum frequency RED **	$-f_R$	–	4 126,250 ± 10	–	kHz
Maximum frequency RED **	$+f_R$	–	4 686,250 ± 10	–	kHz
Minimum frequency BLUE **	$-f_B$	–	4 020,000 ± 10	–	kHz
Maximum frequency BLUE **	$+f_B$	–	4 480,000 ± 10	–	kHz

* The ident. frequencies are also the maximum and minimum output frequencies of the encoder.

** Values are valid for 75% colour bar saturation (EBU) (V_5 = ± 250 mV deviation from clamping level).

APPLICATION INFORMATION



(1) Signal amplitude for 75% colour bar (EBU) = 0,5 V (peak-to-peak value).
(2) For $V_P = 4{,}75$ to 5,3 V, $C_{17} = C_{20} = 0{,}68\ \mu F$; for $V_P > 5{,}3$ V, $C_{17} = C_{20} = 2{,}2\ \mu F$.

Fig. 6 Application using TDA2507 with PLL tuning: $V_P = 5$ V.

FM MODULATOR CONTROLLER

GENERAL DESCRIPTION

The TDA2507 accepts FM signals that are sequentially modulated by two alternating subcarrier frequencies (SECAM signals) and provides sequential DC output levels to control the FM modulator.

The IC is intended for use with the SECAM encoder TDA2506 but can be adapted for other applications. Timing reference pulses from the modulator are required.

Two frequency reference phase-lock loops are contained within the IC; one for 4.40625 MHz, and one for 4.250 MHz. Other frequencies can be accomplished by using external reference sources.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 3)		$V_P = V_{3-6}$	4.75	5.0	7.0	V
Supply current	V_P = 5 V; both PLL circuits on	I_3	–	40	–	mA
Reference voltage		V_{2-6}	3.38	3.5	3.6	V
Storage temperature range		T_{stg}	−65	–	+150	°C
Operating ambient temperature range		T_{amb}	−25	–	+70	°C

PACKAGE OUTLINES

TDA2507 : 16-lead DIL; plastic (with internal heat spreader) (SOT38).
TDA2507T: 16-lead mini-pack; plastic (SO16L; SOT162A).

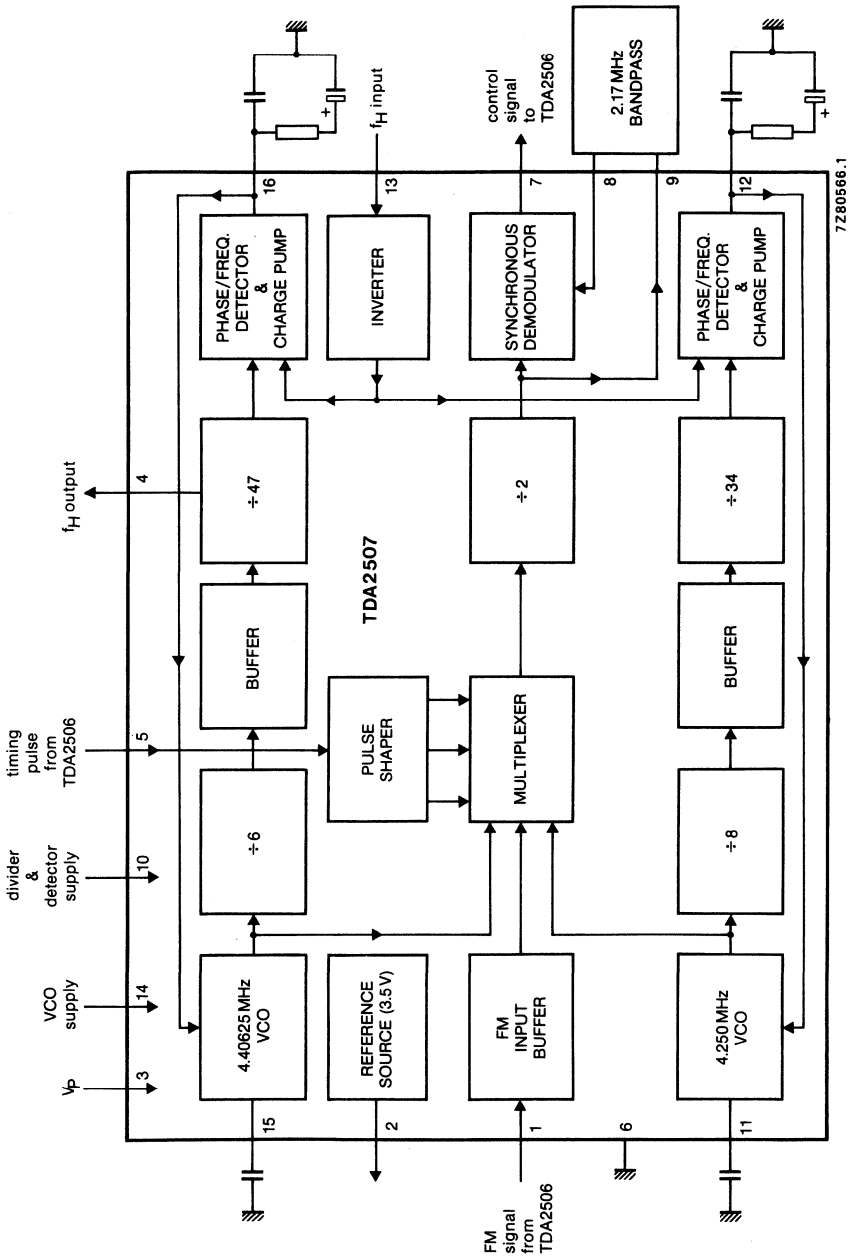


Fig.1 Block diagram.

PINNING

Pin functions

pin	description
1	FM signal input (from TDA2506)
2	Reference voltage output
3	Positive supply voltage
4	Horizontal sync output (f_H = 4 406.250/282 = 15.625 kHz)
5	Timing pulse input (from TDA2506)
6	Ground
7	Control signal output to TDA2506 via low-pass filter
8	Input to synchronous demodulator from band-pass filter
9	Output to band-pass filter
10	Supply voltage for the divider stages and phase/frequency detectors of the two phase-lock loops (PLL)
11	Tuning capacitor for the 4.250 MHz reference oscillator
12	Filter for the phase/frequency detector of the 4.250 MHz phase-lock loop
13	Horizontal sync input (f_H)
14	Supply voltage for the two reference oscillators
15	Tuning capacitor for the 4.40625 MHz reference oscillator
16	Filter for the phase/frequency detector of the 4.40625 MHz phase-lock loop.

FUNCTIONAL DESCRIPTION

Phase-lock loops

The two phase-lock loops each comprise a voltage-controlled reference oscillator, two frequency divider stages and a phase/frequency detector circuit. The loops are closed by charge pumping the reference oscillators from the phase/frequency detector outputs. The centre frequencies of the loops are set by external capacitors at pin 15 (4.40625 MHz) and pin 11 (4.250 MHz). The divider stages which follow the reference oscillators reduce the frequencies of both the loops to 15.625 kHz (f_H) at their respective inputs to the phase/frequency detectors. The reference signals to both phase/frequency detectors are obtained from the horizontal sync input at pin 13.

The divider and phase/frequency detector circuits can be switched off by connecting pin 10 to ground. This leaves only the VCO of each PLL in circuit and allows external signals to be injected at pins 15 and 11, or crystals to be used for tuning the oscillators.

The accuracy of crystal tuning using only one crystal can be obtained by connecting pins 10, 14 and 16 to the reference voltage at pin 2 and connecting a 4.40625 MHz crystal to pin 15. The 4.250 MHz PLL will follow the crystal-derived f_H reference from pin 4 via pin 13 and its phase/frequency detector.

Multiplexer and pulse shaper

The multiplexer receives the 4.40625 and 4.250 MHz reference frequencies from the two VCOs and the FM signals D'_R* and D'_B* from the TDA2506 modulator. The signals are gated one at a time to the multiplexer output in a sequence determined by the timing pulses from TDA2506. The levels of the timing pulses (pin 5) are used in the pulse shaper to generate enable pulses for the multiplexer (see Figs 2 and 3). The multiplexer output sequence is as follows:

4.40625 MHz (2 lines); D'_R* FM signal (1 line); 4.250 MHz (2 lines); D'_B* FM signal (1 line); repeating. The selection of D'_R* or D'_B* FM signal is a feature of the timing of the input at pin 5.

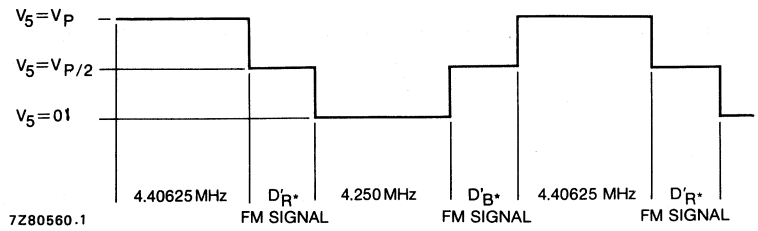


Fig.2 Timing pulse waveform for multiplexer output sequence.

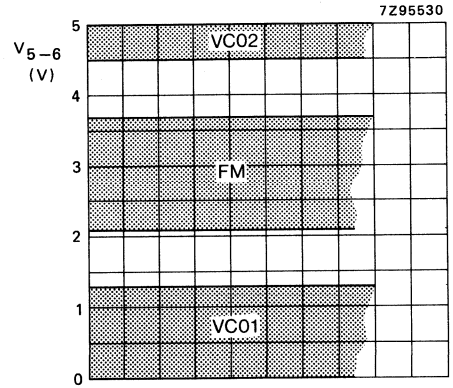


Fig.3 Switching levels of the timing pulse at pin 5.

Divide-by-two stage and synchronous demodulator

The divide-by-two stage halves the frequencies present in the multiplexer output and equalizes the amplitude and pulse shapes of the sequential signals.

Demodulation of the multiplexed signal is performed by filtering the signal via a 2.17 MHz band-pass filter (between pins 8 and 9) and using this filtered signal as a synchronous switch for the main signal. The DC level of the signal from pin 9 is referred externally to the reference voltage from pin 2. An external low-pass filter is required for the output signal from pin 7.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating system IEC 134

parameter	symbol	min.	max.	unit
Supply voltage (pin 3)	V_P	–	13.2	V
Total power dissipation	P_{tot}	see Fig.4		W
Operating ambient temperature range	T_{amb}	−25	+70	°C
Storage temperature range	T_{stg}	−65	+150	°C

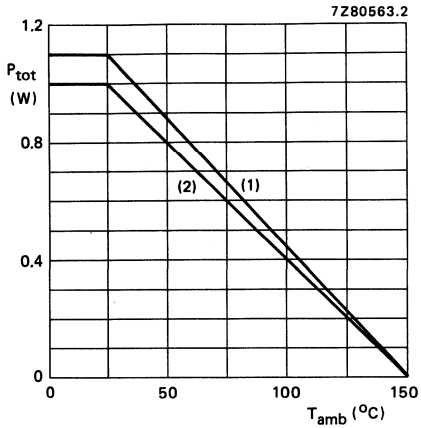
CHARACTERISTICS

$V_P = V_{3-6} = 5$ V; $T_{amb} = 25$ °C; all voltages are with reference to ground; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage (pin 3)		V_P	4.75	5.0	7.0	V
Supply current	$V_{14} = V_{10} = V_2$	I_P	–	35	–	mA
Supply current	$V_{14} = V_2$	I_P	–	20	–	mA
Reference voltage (pin 2)		V_{2-6}	3.38	3.5	3.6	V
Phase-lock loops						
DC voltage output level						
pin 11		V_{11-6}	2.4	2.6	2.8	V
pin 15		V_{15-6}	2.4	2.6	2.8	V
Amplitude of oscillation (peak-to-peak value)						
pin 11		$V_{11(p-p)}$	–	130	–	mV
pin 15		$V_{15(p-p)}$	–	130	–	mV
Input current	see Fig.5					
pin 11	$V_{12-6} = 1.5$ V	I_{11}	–	130	–	μA
pin 15	$V_{16-6} = 1.5$ V	I_{11}	–	130	–	μA
Limiting values for VCO control voltages						
pin 12		V_{12}	0.8	–	1.9	V
pin 16		V_{16}	0.8	–	1.9	V
Output resistance at pin 4	V_4 = HIGH	R_4	5.1	6.8	8.5	kΩ
Input resistance at pin 13		R_{13}	200	–	–	kΩ
Amplitude of f_H pulse required at pin 13	note 1	V_{13}	2	–	–	V
FM input buffer (pin 1)						
Input resistance		R_1	180	–	–	kΩ
Switching level of FM input		V_1	2.2	2.3	2.4	V
Required input amplitude		V_1	0.5	–	2.0	V
Pulse shaper input (pin 5)						
Input resistance		R_5	200	–	–	kΩ
Demodulator						
Sink current at pin 9 into divide-by-two circuit	V_9 = LOW	I_9	0.6	0.9	1.2	mA
Demodulator input bias voltage at pin 8		V_8	1.60	1.68	1.76	V
Demodulator output current from pin 7	see Fig.6					
output current at A		$-I_7$	0.6	0.9	1.2	mA
output current at B		I_7	1.2	0.9	0.6	mA

Note to the characteristics

1. Duty factor and timing not important.



(1) Device mounted on a ceramic substrate
(2) Device mounted on a printed-circuit board

Fig.4 Power derating curve.

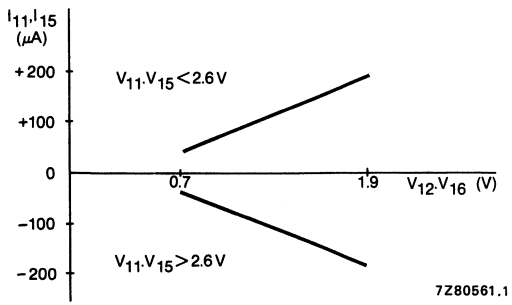


Fig.5 Current input to pins 11 and 15 as a function of voltage at pins 12 and 16 (typical values).

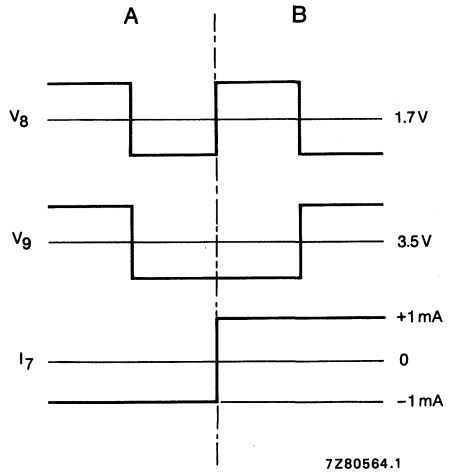


Fig.6 Demodulator output current from pin 7 (typical values).

APPLICATION INFORMATION

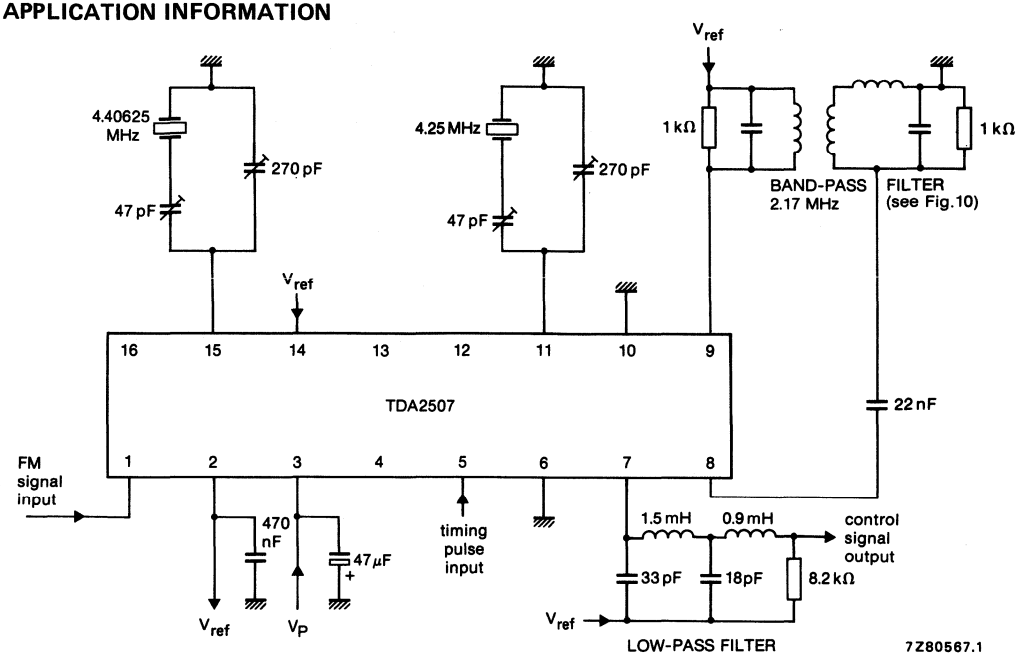


Fig.7 Application diagram using two crystals for tuning; V_P = 5 V.

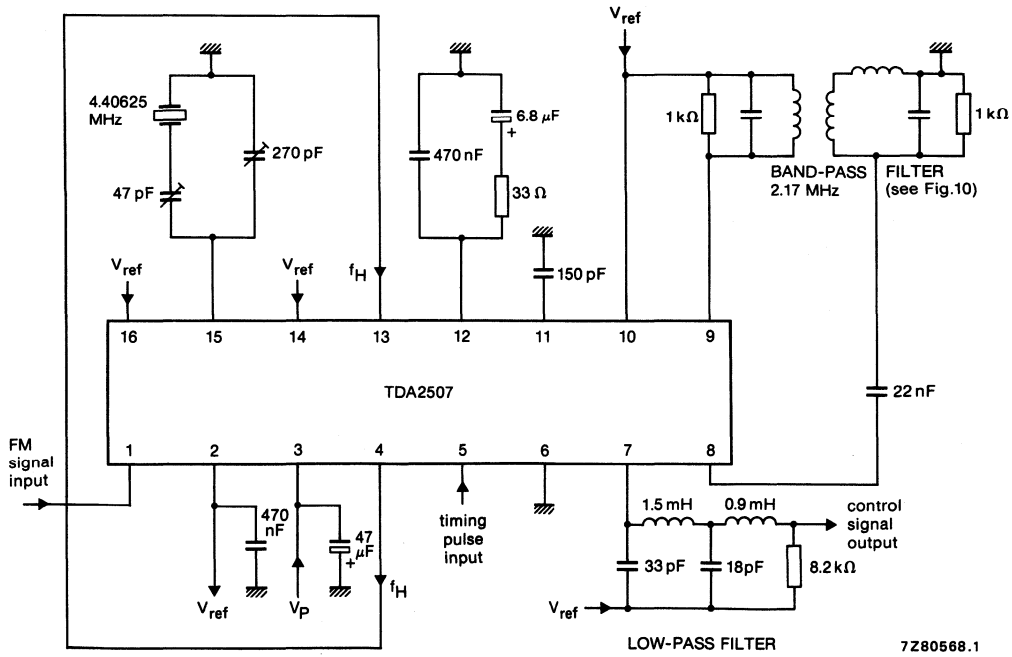


Fig.8 Application diagram using single crystal tuning; V_P = 5 V.

APPLICATION INFORMATION (continued)

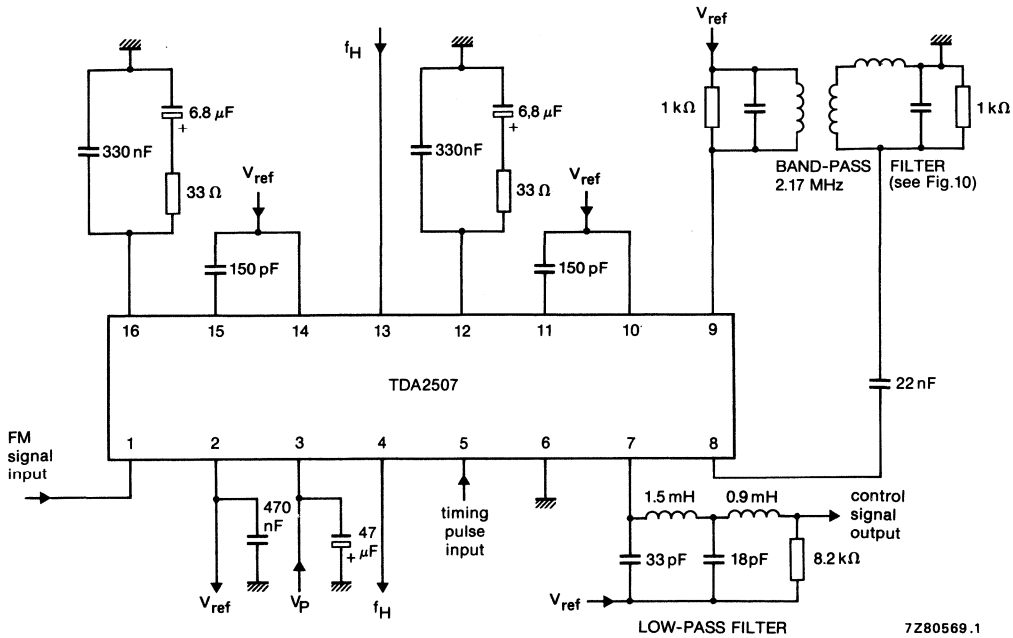


Fig.9 Application diagram using PLL tuning; V_P = 5 V.

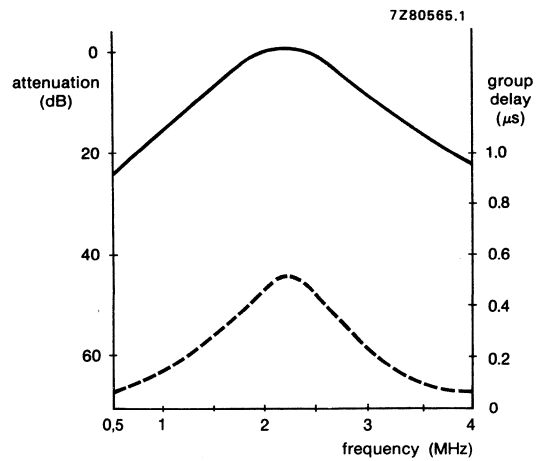


Fig.10 Typical response of 2.17 MHz band-pass filter.

AM SOUND I.F. CIRCUIT FOR FRENCH STANDARD

GENERAL DESCRIPTION

The TDA2543 is a monolithic integrated AM sound i.f. circuit in television receivers for the French standards L and L'.

The circuit incorporates the following functions:

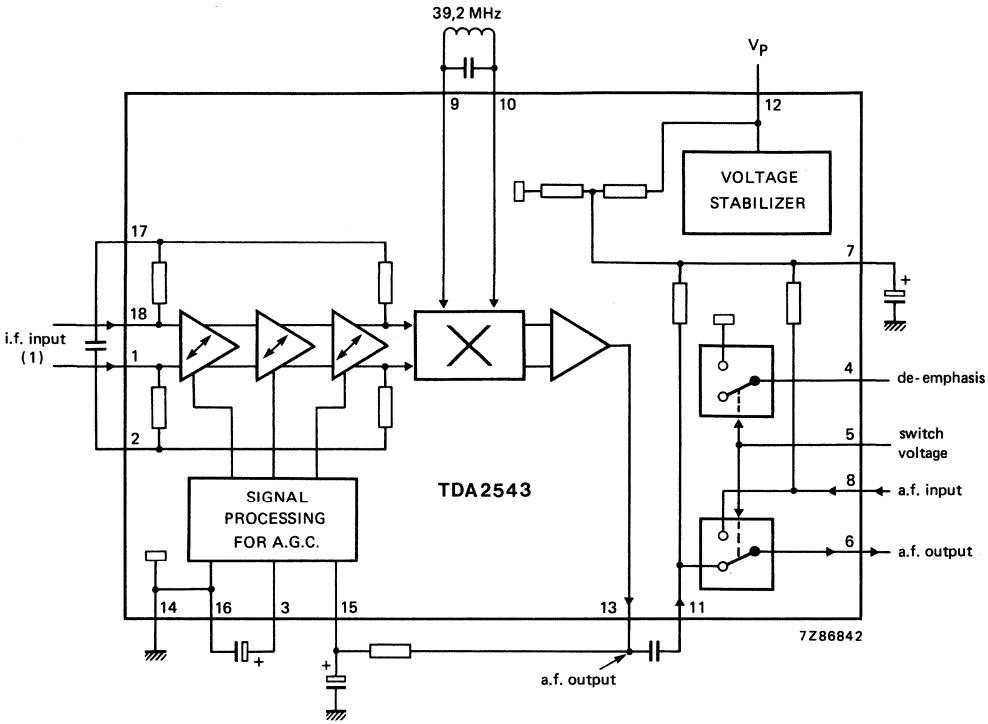
- 3-stage gain controlled i.f. amplifier, providing complete i.f. gain
- Synchronous AM demodulator
- A.G.C. circuit
- Audio input circuit with two external audio inputs and switching facilities to provide for either the demodulated i.f. or an external signal output
- Demodulated i.f. output is available from the input of the switching circuit

QUICK REFERENCE DATA

Supply voltage (pin 12)	$V_{12\text{-}14} = V_P$	typ.	12 V
Minimum i.f. vision carrier input voltage (r.m.s. value) for an output signal $V_{13\text{-}14(rms)}$ = 480 mV	$V_{VC1\text{-}18(rms)}$	max.	30 μV
I.F. control range	ΔG_v	min.	60 dB
A.F. output voltage (r.m.s. value)	$V_{13\text{-}14(rms)}$	typ.	680 mV
Distortion at $V_{VC1\text{-}18(rms)}$ = 5 mV	d_{tot}	max.	1 %
Signal-to-weighted-noise ratio according to CCIR 468	S + N/N	min.	50 dB
Maximum signal amplitude for the a.f. switch (r.m.s. value)	$V_{8;11\text{-}14(rms)}$	min.	2 V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



(1) I.F. signal: vision carrier (V.C.) and sound carrier (S.C.).

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 12)	$V_{12\text{-}14} = V_P$	max.	13,2 V
Switch voltage (pin 5)	$V_{5\text{-}14}$	max.	V_P V
Current at pin 4	I_4	max.	5 mA
	$-I_4$	short-circuit proof	
Storage temperature range	T_{stg}	−25 to +150	°C
Operating ambient temperature range	T_{amb}	0 to +70	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; input signal (vision carrier V.C.) with f_{VC} = 39,2 MHz; sound carrier (S.C.) modulated with f_m = 1 kHz and m = 0,8; measured in Fig. 2; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage range (pin 12)	V_P	10,8	–	13,2	V
Supply current (pin 12)	I_P	–	50	–	mA
I.F. input (pins 1 and 18)					
Minimum i.f. vision carrier input voltage (r.m.s. value) for an output signal $V_{13\text{-}14(rms)}$ = 480 mV	$V_{VC1\text{-}18(rms)}$	–	–	30	μV
Maximum i.f. vision carrier input voltage (r.m.s. value)	$V_{VC1\text{-}18(rms)}$	–	50	–	mV
Input resistance	$R_{1\text{-}18}$	–	2	–	kΩ
Input capacitance	$C_{1\text{-}18}$	–	2	–	pF
I.F. control range (–3 dB)	ΔG_v	60	–	–	dB
A.F. output (pin 13)					
A.F. output voltage (r.m.s. value) at $V_{VC1\text{-}18(rms)}$ = 5 mV	$V_{13\text{-}14(rms)}$	–	680	–	mV
Output resistance	$R_{13\text{-}14}$	–	100	–	Ω
Distortion at $V_{VC1\text{-}18(rms)}$ = 5 mV	d_{tot}	–	–	1	%
Signal-to-weighted-noise ratio at a.f. output (pin 13) according to CCIR 468 at $V_{VC1\text{-}18(rms)}$ = 5 mV	S + N/N	50	–	–	dB
A.F. switch (pins 8, 11 and 6)					
Maximum input voltage (r.m.s. value)	$V_{8\text{-}14(rms)}$ $V_{11\text{-}14(rms)}$	2 2	– –	– –	V V
Voltage gain	G_v	–	0 ± 1	–	dB
Amplitude frequency response (–3 dB)	f	20	–	20 000	Hz
Crosstalk between the non-switched input and the output	α	60	–	–	dB
Input resistance	$R_{8;\ 11\text{-}14}$	10	–	–	kΩ
Output resistance	$R_{6\text{-}14}$	–	400	–	Ω
De-emphasis switch (pin 4)					
Input resistance for: ON ($V_{5\text{-}14} > 3$ V) OFF ($V_{5\text{-}14} < 1$ V)	 $R_{4\text{-}14}$ $R_{4\text{-}14}$	 – 100	 – –	 200 –	 Ω kΩ
Switch voltage (pin 5)					
A.F. switch ON (pin 8 switched)	$V_{5\text{-}14}$	3	–	V_P	V
A.F. switch OFF (pin 11 switched)	$V_{5\text{-}14}$	0	–	1	V

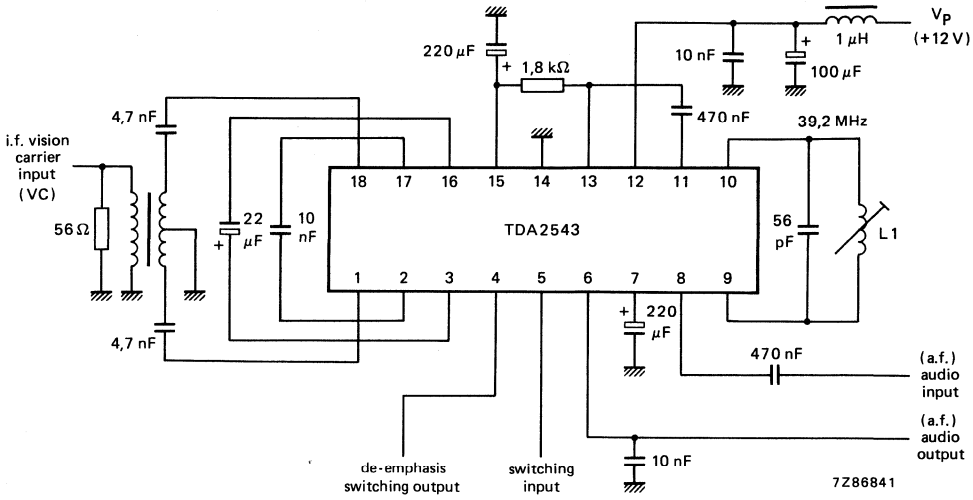


Fig. 2 Measuring circuit; L1 adjusted to minimum distortion at the a.f. output.

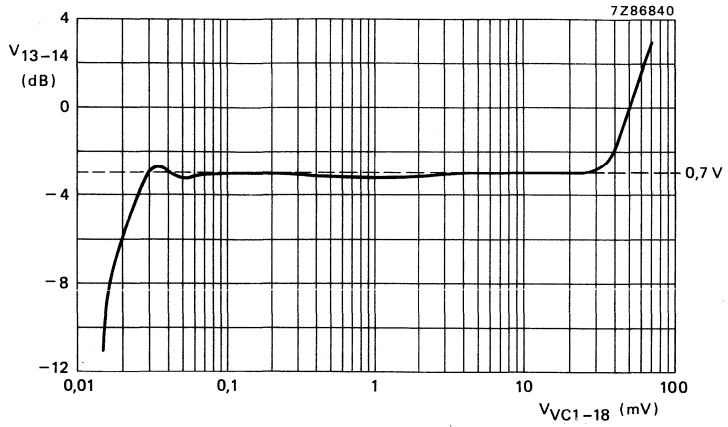


Fig. 3 Control curve of the i.f. amplifier; the r.m.s. a.f. output voltage at pin 13 ($V_{13\text{-}14(rms)}$) as a function of the r.m.s. i.f. vision carrier input voltage ($V_{VC1\text{-}18(rms)}$) at f_m = 1 kHz and m = 0,8.

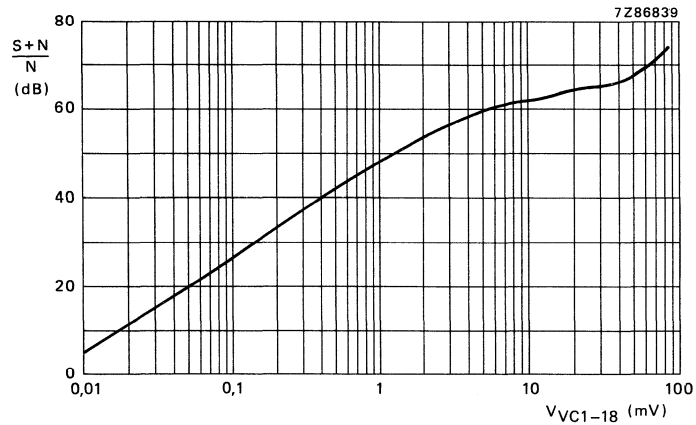


Fig. 4 Signal-to-weighted-noise ratio (S + N/N) at the output (pin 13) as a function of the r.m.s. i.f. vision carrier input voltage ($V_{VC1\text{-}18(rms)}$).

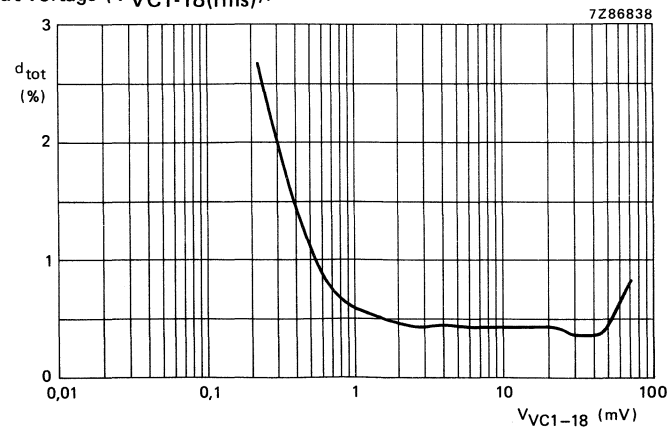


Fig. 5 Distortion (d_{tot}) at the output (pin 13) as a function of the r.m.s. i.f. vision carrier input voltage ($V_{VC1\text{-}18(rms)}$) at f_m = 1 kHz and m = 0,8.

QUASI-SPLIT-SOUND CIRCUIT

GENERAL DESCRIPTION

The TDA2545A is a monolithic integrated circuit for quasi-split-sound processing in television receivers.

Features

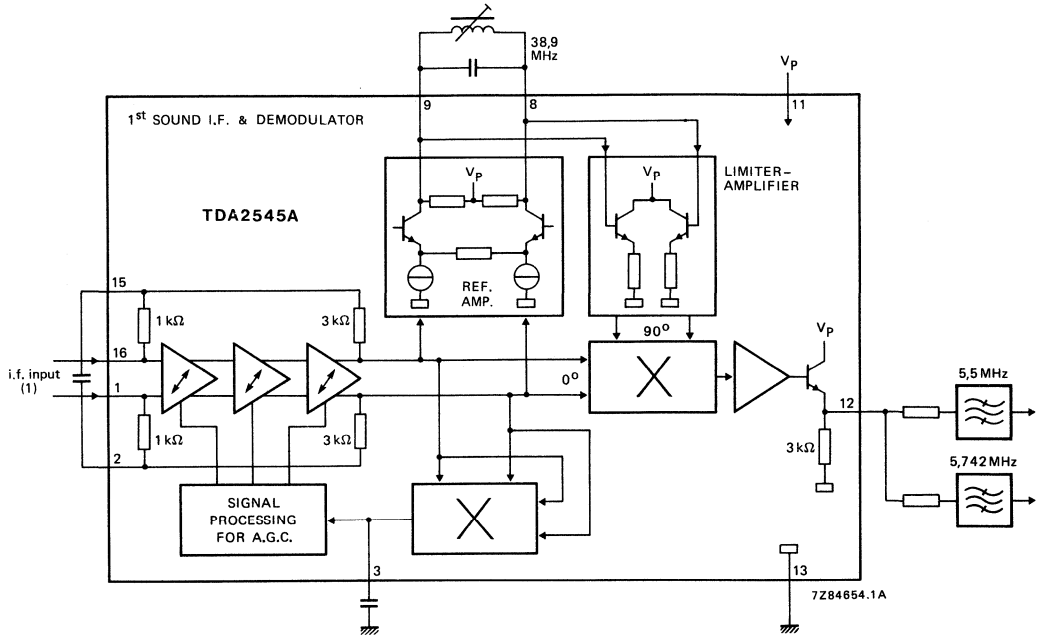
- 3-stage gain controlled i.f. amplifier
- A.G.C. circuit
- Reference amplifier and limiter amplifier for vision carrier (V.C.) processing
- Linear multiplier for quadrature demodulation

QUICK REFERENCE DATA

Supply voltage (pin 11)	$V_P = V_{11\text{-}13}$	typ.	12 V
Supply current (pin 11)	$I_P = I_{11}$	typ.	45 mA
Minimum i.f. vision carrier input voltage (r.m.s. value)	$V_{VC1\text{-}16(rms)}$	typ.	150 μV
Output voltage; 5,5 MHz (r.m.s. value)	$V_{12\text{-}13(rms)}$	typ.	100 mV
Output voltage; 5,742 MHz (r.m.s. value)	$V_{12\text{-}13(rms)}$	typ.	45 mV
I.F. control range	ΔG_V	typ.	64 dB
Signal-to-weighted-noise ratio (rel. to 1 kHz; 30 kHz deviation)			
at 5,5 MHz } for 2T/20T pulses with white bars	S + W/W	typ.	58 dB
at 5,742 MHz } for 2T/20T pulses with white bars	S + W/W	typ.	56 dB

PACKAGE OUTLINES

16-lead DIL; plastic (SOT38).



(1) I.F. signal: vision carrier (V.C.) and sound carrier (S.C.).

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 11)	$V_P = V_{11-13}$	max.	13,2	V
Storage temperature range	T_{stg}	−25 to	+150	°C
Operating ambient temperature range	T_{amb}	0 to	+70	°C

CHARACTERISTICS

$V_P = V_{11-13} = 12$ V; $T_{amb} = 25$ °C; measured at $f_{VC} = 38{,}9$ MHz, $f_{SC1} = 33{,}4$ MHz, $f_{SC2} = 33{,}158$ MHz:

Vision carrier (V.C.) modulated with different video signals (see below); modulation depth 100% (proportional to 10% residual carrier).

Vision carrier amplitude (r.m.s. value) is $V_{VC} = 10$ mV.
Vision-to-sound carrier ratios are VC/SC1 = 13 dB and VC/SC2 = 20 dB.

Sound carriers (SC1, SC2) modulated with f = 1 kHz and deviation $\Delta f = \pm 30$ kHz.
For measuring circuit see Fig. 2; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply (pin 11)					
Supply voltage	$V_P = V_{11-13}$	10,8	12	13,2	V
Supply current	$I_P = I_{11}$	33	45	55	mA
I.F. amplifier					
Input voltage for start of gain control (intercarrier signals −3 dB)	$V_{VC1-16(rms)}$	–	150	200	μV
Input voltage for end of gain control (intercarrier signals + 1 dB)	$V_{VC1-16(rms)}$	100	250	–	mV
I.F. gain control range	ΔG_v	60	64	–	dB
Control voltage range (see Fig. 3)	V_{3-13}	4	–	V_p	V
Input resistance	R_{1-16}	–	2,5	–	kΩ
Input capacitance	C_{1-16}	–	1,5	–	pF
Intercarrier generation					
Output voltage; 5,5 MHz (r.m.s. value)	$V_{12-13(rms)}$	60	100	140	mV
Output voltage; 5,742 MHz (r.m.s. value)	$V_{12-13(rms)}$	27	45	63	mV
D.C. output voltage	V_{12-13}	–	5,9	–	V
Allowable d.c. load resistance at the output	R_{12-13}	7	–	–	kΩ
Allowable output current	$-I_{12}$	–	–	1	mA
Intercarrier signal-to-noise (see note 1) (measured behind the FM demodulators) weighted according to CCIR 468-2, quasi-peak					
a. 2T/20T pulses with white bars (see also Fig. 4)					
at 5,5 MHz	S+W/W	53	58	–	dB
at 5,742 MHz	S+W/W	51	56	–	dB
b. 6 kHz sinewave					
at 5,5 MHz	S+W/W	50	53	–	dB
at 5,742 MHz	S+W/W	50	53	–	dB
c. black level (sync pulses only)					
at 5,5 MHz	S+W/W	60	65	–	dB
at 5,742 MHz	S+W/W	58	63	–	dB

Note 1.
Incidental phase on the vision carrier, caused by TV transmitter, has to be less than 0,5 degrees for black to white transient (equivalent to S+W/W = 56 dB for 6 kHz sinewave).

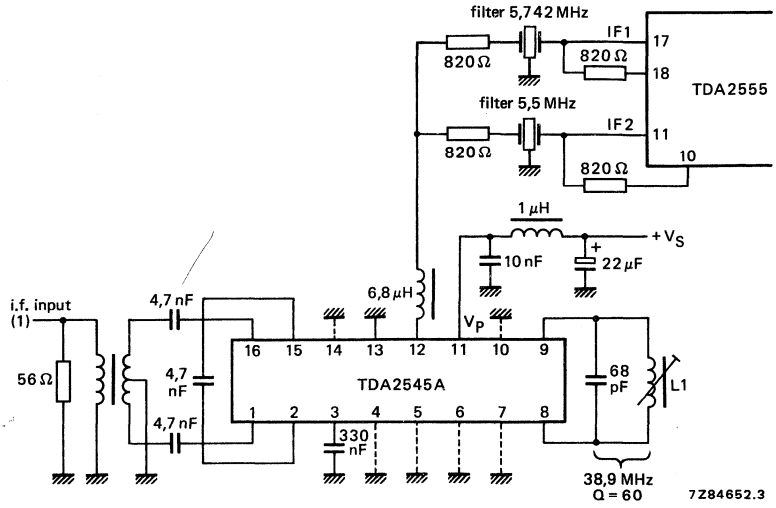


Fig. 2 Measuring circuit for TDA2545A.

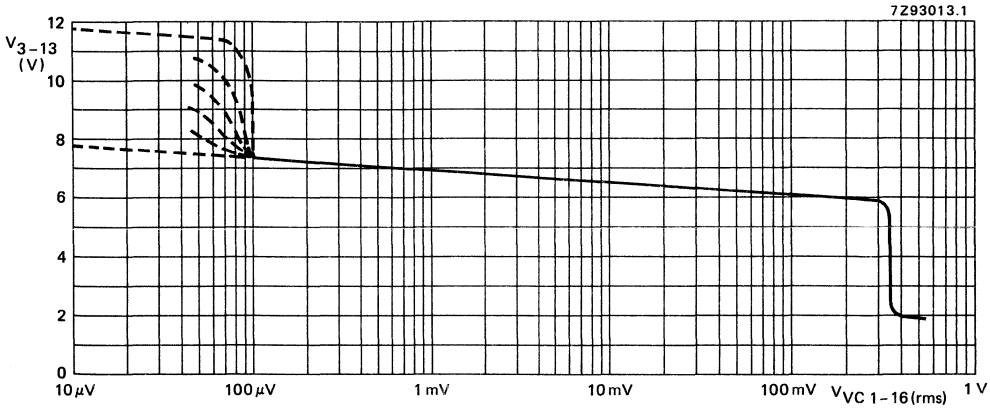


Fig. 3 Control voltage at pin 3 as a function of the input voltage $V_{VC1-16\,(rms)}$.

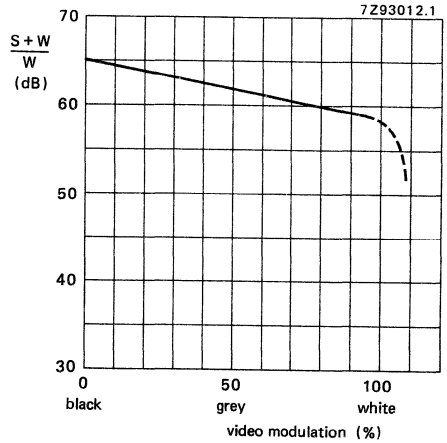


Fig. 4 Signal-to-weighted-noise ratio depending on video modulation.

QUASI-SPLIT-SOUND CIRCUIT WITH 5,5 MHz DEMODULATION

GENERAL DESCRIPTION

The TDA2546A is a monolithic integrated circuit for quasi-split-sound processing, including 5,5 MHz demodulation, in television receivers.

Features

1st i.f. (V.C.: vision carrier plus S.C.: sound carrier)

- 3-stage gain controlled i.f. amplifier
- A.G.C. circuit
- Reference amplifier and limiter amplifier for vision carrier (V.C.) processing
- Linear multiplier for quadrature demodulation

2nd i.f. (5,5 MHz signal)

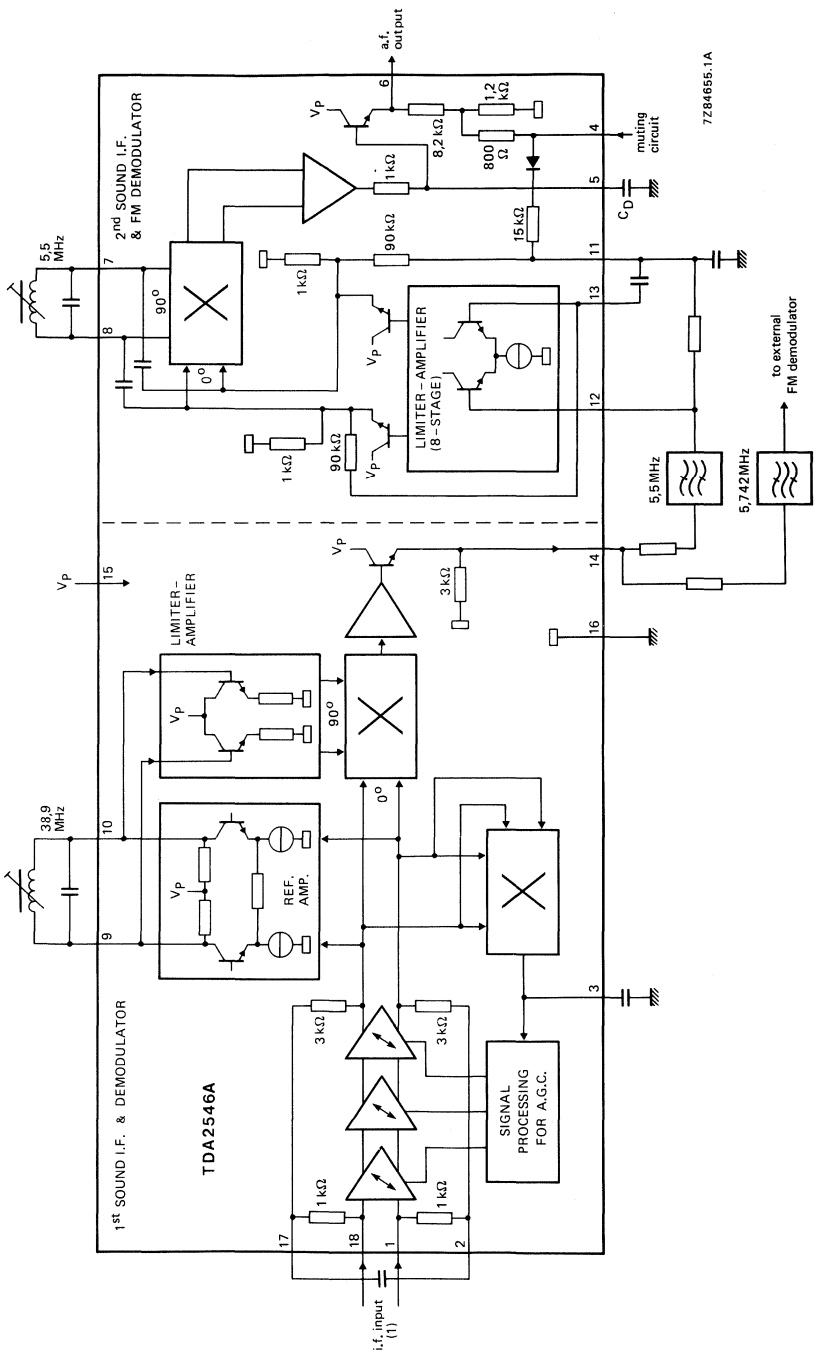
- 8-stage limiter amplifier
- Quadrature demodulator
- A.F. amplifier with de-emphasis
- AV switch

QUICK REFERENCE DATA

Supply voltage (pin 15)	$V_P = V_{15\text{-}16}$	typ.	12 V
Supply current (pin 15)	$I_P = I_{15}$	typ.	57 mA
Minimum i.f. vision carrier input voltage (r.m.s. value)	$V_{VC1\text{-}18(rms)}$	typ.	150 μV
Output voltage; 5,5 MHz (r.m.s. value)	$V_{14\text{-}16(rms)}$	typ.	100 mV
Output voltage; 5,742 MHz (r.m.s. value)	$V_{14\text{-}16(rms)}$	typ.	45 mV
I.F. control range	ΔG_V	typ.	64 dB
Signal-to-weighted-noise ratio (rel. to 1 kHz; 30 kHz deviation)			
at 5,5 MHz for 2T/20T pulses with white bars	S + W/W	typ.	58 dB
at 5,742 MHz	S + W/W	typ.	56 dB
A.F. output voltage (r.m.s. value)	$V_{o6\text{-}16(rms)}$	typ.	0,6 V

PACKAGE OUTLINES

18-lead DIL; plastic (SOT102).



(1) I.F. signal: vision carrier (V.C.) and sound carrier (S.C.)

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 15)	$V_P = V_{15-16}$	max.	13,2	V
Input current (pin 4)	I_4	max.	7	mA
Storage temperature range	T_{stg}	−25 to	+150	°C
Operating ambient temperature range	T_{amb}	0 to	+70	°C

CHARACTERISTICS

$V_P = V_{15-16} = 12$ V; $T_{amb} = 25$ °C; measured at $f_{VC} = 38{,}9$ MHz, $f_{SC1} = 33{,}4$ MHz, $f_{SC2} = 33{,}158$ MHz:

Vision carrier (V.C.) modulated with different video signals (see below); modulation depth 100% (proportional to 10% residual carrier).

Vision carrier amplitude (r.m.s. value) is $V_{VC} = 10$ mV.
Vision-to-sound carrier ratios are VC/SC1 = 13 dB and VC/SC2 = 20 dB.

Sound carriers (SC1, SC2) modulated with f = 1 kHz and deviation $\Delta f = \pm 30$ kHz.
For measuring circuit see Fig. 2; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply (pin 15)					
Supply voltage	$V_P = V_{15-16}$	10,8	12	13,2	V
Supply current	$I_P = I_{15}$	40	57	75	mA
I.F. amplifier					
Input voltage for start of gain control (intercarrier signals −3 dB)	$V_{VC1-18(rms)}$	–	150	200	μV
Input voltage for end of gain control (intercarrier signals + 1 dB)	$V_{VC1-18(rms)}$	100	250	–	mV
I.F. gain control range	ΔG_V	60	64	–	dB
Control voltage range (see Fig. 3)	V_{3-16}	4	–	V_p	V
Input resistance	R_{1-18}	–	2,5	–	kΩ
Input capacitance	C_{1-18}	–	1,5	–	pF
Intercarrier generation					
Output voltage; 5,5 MHz (r.m.s. value)	$V_{14-16(rms)}$	60	100	140	mV
Output voltage; 5,742 MHz (r.m.s. value)	$V_{14-16(rms)}$	27	45	63	mV
D.C. output voltage	V_{14-16}	–	5,9	–	V
Allowable d.c. load resistance at the output	R_{14-16}	7	–	–	V
Allowable output current	$-I_{14}$	–	–	1	mA
Frequency demodulator (measured at f = 5,5 MHz)					
Input voltage vor start of limiting (r.m.s. value)	$V_{12-16(rms)}$	–	–	100	μV
Maximum input voltage (r.m.s. value)	$V_{12-16(rms)}$	–	200	–	mV
D.C. output voltage	$V_{11,12,13-16}$	–	2,2	–	V

parameter	symbol	min.	typ.	max.	unit
A.F. output voltage (r.m.s. value)	$V_{6\text{-}16(rms)}$	450	600	810	mV
D.C. output voltage	$V_{6\text{-}16}$	–	4	–	V
Allowable d.c. load resistance at the output	$R_{6\text{-}16}$	27	–	–	kΩ
Allowable a.c. load impedance at the output	$Z_{6\text{-}16}$	10	–	–	kΩ
Total harmonic distortion	THD	–	–	1	%
Internal de-emphasis resistance	$R_{i5\text{-}16}$	–	1	–	kΩ
Switching voltage (pin 4)					
for mute	$V_{4\text{-}16}$	9	–	–	V
for a.f. on	$V_{4\text{-}16}$	–	–	2,5	V
Intercarrier signal-to-noise (measured behind the FM demodulators)					
Signal-to-weighted-noise ratio according to CCIR 468-2, quasi-peak 2T/20T pulses with white bars (see also Fig. 4)					
at 5,5 MHz	S+W/W	53	58	–	dB
at 5,742 MHz	S+W/W	51	56	–	dB
6 kHz sine wave					
at 5,5 MHz	S+W/W	50	53	–	dB
at 5,742 MHz	S+W/W	50	53	–	dB
with black level (vision carrier modulated with sync pulses only)					
at 5,5 MHz	S+W/W	60	65	–	dB
at 5,742 MHz	S+W/W	58	63	–	dB

NOTES TO THE CHARACTERISTICS

1. Incidential phase on the vision carrier, caused by TV-transmitter, has to be less than 0,5 degrees for black to white transient.
   (Equivalent to S+W/W = 56 dB for 6 kHz sine wave).

(1) I.F. signal: vision carrier (V.C.) and sound carrier (S.C.)

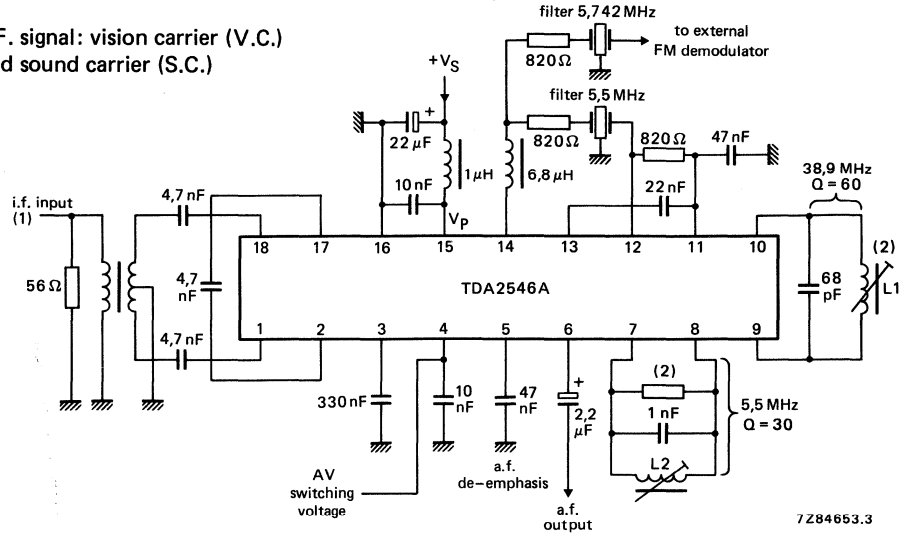


Fig. 2 Measuring circuit for TDA2546A.

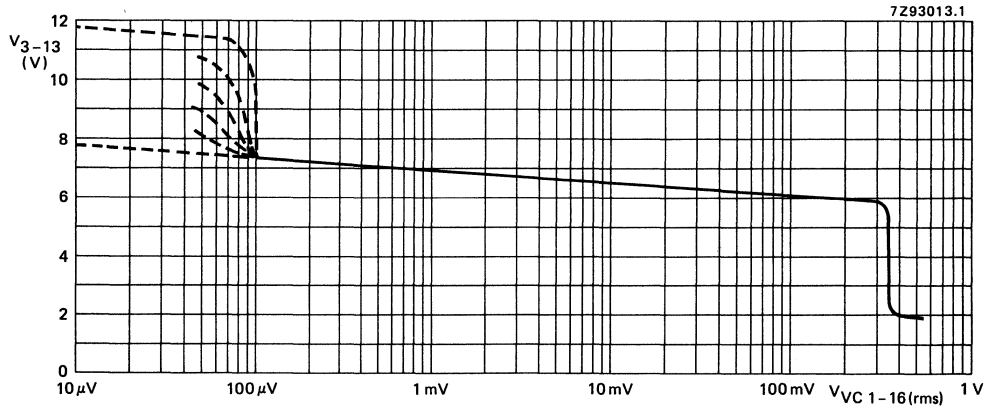


Fig. 3 Control voltage at pin 3 as a function of the input voltage $V_{VC1-18(rms)}$.

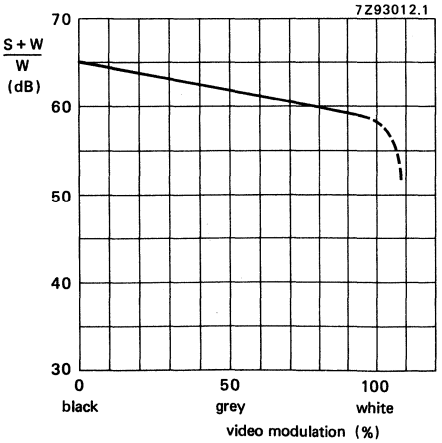


Fig. 4 Signal-to-weighted-noise ratio depending on video modulation.

I.F. AMPLIFIER AND DEMODULATOR FOR MULTISTANDARD TV RECEIVERS

GENERAL DESCRIPTION

The TDA2549 is a complete i.f. circuit with a.f.c., a.g.c., demodulation and video preamplification facilities for multistandard television receivers. It is capable of handling positively and negatively modulated video signals in both colour and black/white receivers.

Features

- Gain-controlled wide-band amplifier providing complete i.f. gain
- Synchronous demodulator for positive and negative modulation
- Video preamplifier with noise protection for negative modulation
- Auxiliary video input and output (75 Ω)
- Video switch to select between auxiliary video input signal and demodulated video signal
- A.F.C. circuit with on/off switch and inverter switch
- A.G.C. circuit for positive modulation (mean level) and negative modulation (noise gate)
- A.G.C. output for controlling MOSFET tuners

QUICK REFERENCE DATA

Supply voltage (pins 13 and 21)	$V_P = V_{13;21-3}$	typ.	12 V
Supply current (pins 13 and 21)	$I_P = I_{13;21-3}$	typ.	82 mA
I.F. input signal at V_o = 2 V (between pins 6 and 7)	$V_i = V_{6-7}$	typ.	50 μV
Video output voltage at V_i = 0 V (between pins 22 and 3)			
positive modulation	$V_o = V_{22-3}$	typ.	2 V
negative modulation	$V_o = V_{22-3}$	typ.	4 V
Gain control range	G_v	typ.	74 dB
Signal-to-noise ratio at V_i = 10 mV	S/N	typ.	57 dB
A.F.C. output voltage swing (pin 15)	V_{15-3}	min.	10 V
Max. tuner a.g.c. output current (pin 10)	I_{10}	min.	0,3 mA
Video bandwidth (3 dB)	B	typ.	5,5 MHz
Auxiliary video input voltage (pin 12) at V_o = 2 V (peak-to-peak value)	$V_{12-3(p-p)}$	typ.	1 V
Auxiliary video output impedance (pin 14)	$\lvert Z_{14-3} \rvert$	typ.	7 Ω
Auxiliary video output voltage (pin 14)	V_{14-3}	typ.	2 V

PACKAGE OUTLINE

24-lead DIL; plastic (SOT101A).

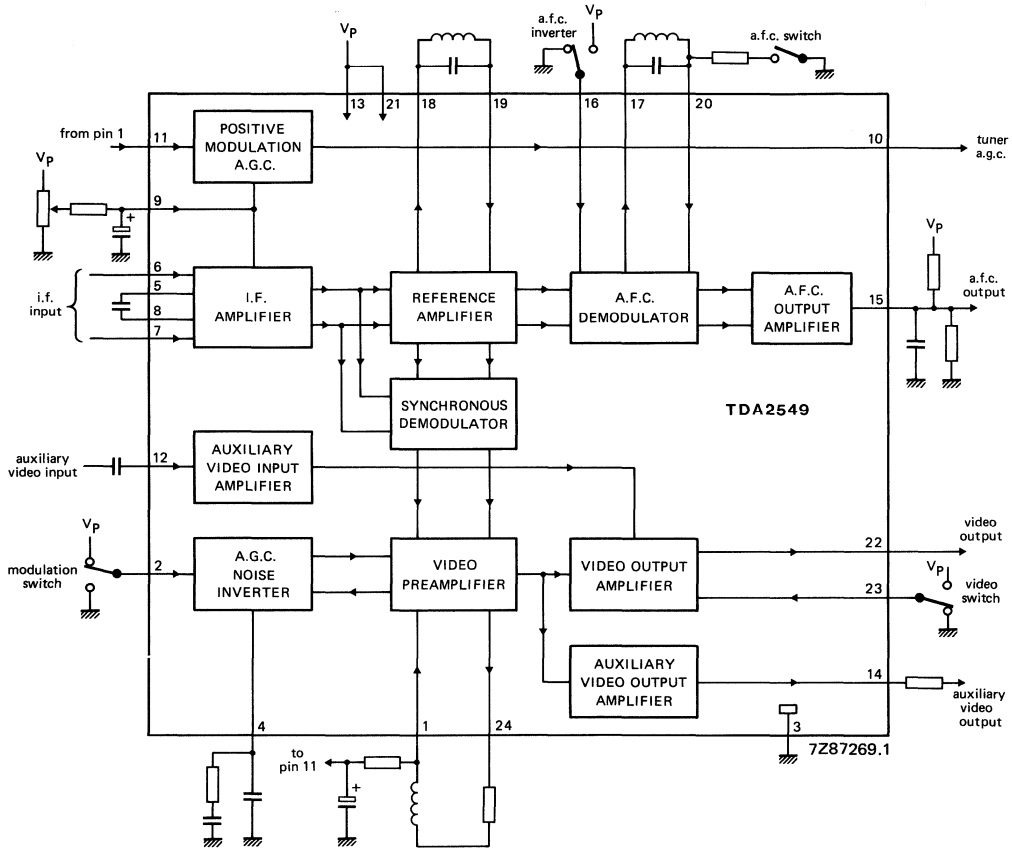


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pins 13 and 21)	V_P	13,8 V
Storage temperature range	T_{stg}	−25 to +125 °C
Operating ambient temperature range	T_{amb}	−25 to +70 °C

CHARACTERISTICS (measured in Fig. 5)

V_P = 12 V; T_{amb} = 25 °C

paramater	symbol	min.	typ.	max.	unit
Supply voltage range	V_P	10,8	12	13,2	V
Supply current (pins 13 and 21)	I_P	–	82	–	mA
I.F. input signal for V_o = 2 V (between pins 6 and 7)	$V_i = V_{6-7}$	–	50	150	μV
Input impedance (differential)	$\lvert Z_{6-7} \rvert$	–	2	–	kΩ
Input capacitance (differential)	C_{6-7}	–	2	–	pF
Zero signal output level positive modulation	V_{22-3}	1,6	2	2,3	V
negative modulation	V_{22-3}	3,7	4	4,3	V
Top sync output level	V_{22-3}	1,7	2	2,3	V
Gain control range	G_v	50	74	–	dB
Signal-to-noise ratio at V_i = 10 mV (note 1)	S/N	50	57	–	dB
Maximum video output amplitude for positive modulation (peak-to-peak value)	$V_{22-3(p-p)}$	4,5	–	–	V
Bandwidth of video amplifier (3 dB)	B	–	5,5	–	MHz
Differential gain at V_o = 2 V	dG	–	4	10	%
Differential phase at V_o = 2 V	$d\varphi$	–	2	10	%
Residual carrier signal (r.m.s. value)	$V_{24-3(rms)}$	–	10	20	mV
Residual second harmonic of carrier signal (r.m.s. value)	$V_{24-3(rms)}$	–	20	60	mV

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
A.F.C. output voltage swing	V_{15-3}	10	–	–	V
Change of frequency required for a.f.c. output voltage swing of 10 V	Δf	–	70	200	kHz
A.F.C. switch off for a voltage lower than:	V_{17-3}	–	–	1,5	V
A.F.C. inverter switch					
positive a.f.c. (Fig. 2)	V_{16-3}	0	–	1,5	V
negative a.f.c. (Fig. 3)	V_{16-3}	4	–	12	V
Tuner A.G.C.					
Leakage current	I_{10}	–	–	15	μA
Saturation voltage					
I_{10} = 0,3 mA	V_{10-3}	–	0,1	0,3	V
take-over point LOW	V_i	–	–	3	mV
take-over point HIGH	V_i	10	–	–	mV
Signal expansion at G_v = 50 dB	ΔV_{22-3}	–	–	0,5	dB
Negative modulation (Fig. 4)					
white spot inverter threshold level	V_{22-3}	–	4,6	–	V
white spot insertion level	V_{22-3}	–	3,2	–	V
noise inverter threshold level	V_{22-3}	–	0,9	–	V
noise insertion level	V_{22-3}	–	2,5	–	V
Positive modulation a.g.c. detector reference level	V_{11-3}	3,0	3,2	3,4	V
Auxiliary video input signal for $V_{o(p-p)}$ = 2 V	V_{12-3}	0,7	1	1,4	V
Auxiliary video output					
output signal (note 2)	V_{14-3}	–	1	–	V
top sync level	V_{14-3}	1	2	3	V
output impedance	$\lvert Z_{14-3} \rvert$	–	7	–	Ω
Levels for video switches					
positive video	V_{2-3}	–	–	1	V
negative video	V_{2-3}	3	–	–	V
internally demodulated signal	V_{23-3}	–	–	1	V
auxiliary video signal	V_{23-3}	3	–	–	V

Notes to the characteristics

1. Signal-to-noise ratio $S/N = \dfrac{V_o \text{ black-to-white}}{V_{n(rms)} \text{ at } B = 5 \text{ MHz}}$.
2. Measured in application of Fig. 5.

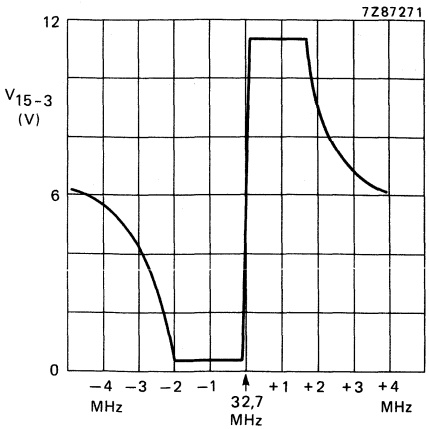


Fig. 2 A.F.C. output voltage V_{15-3} for positive a.f.c.

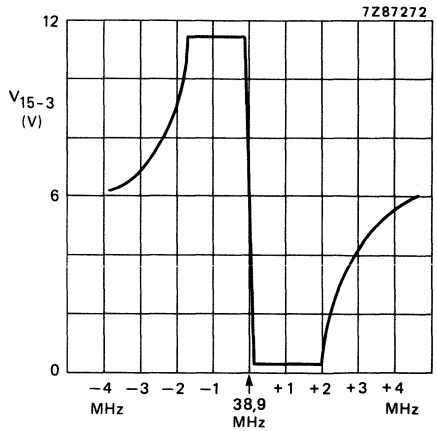


Fig. 3 A.F.C. output voltage V_{15-3} for negative a.f.c.

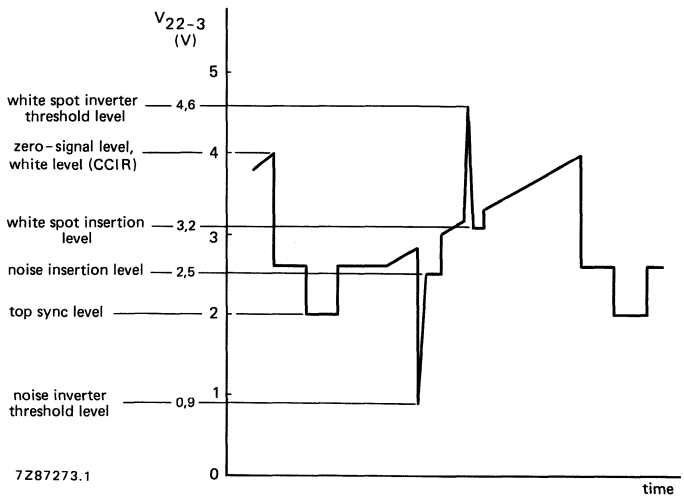


Fig. 4 Video output waveform showing white spot and noise inverter threshold levels.

APPLICATION INFORMATION

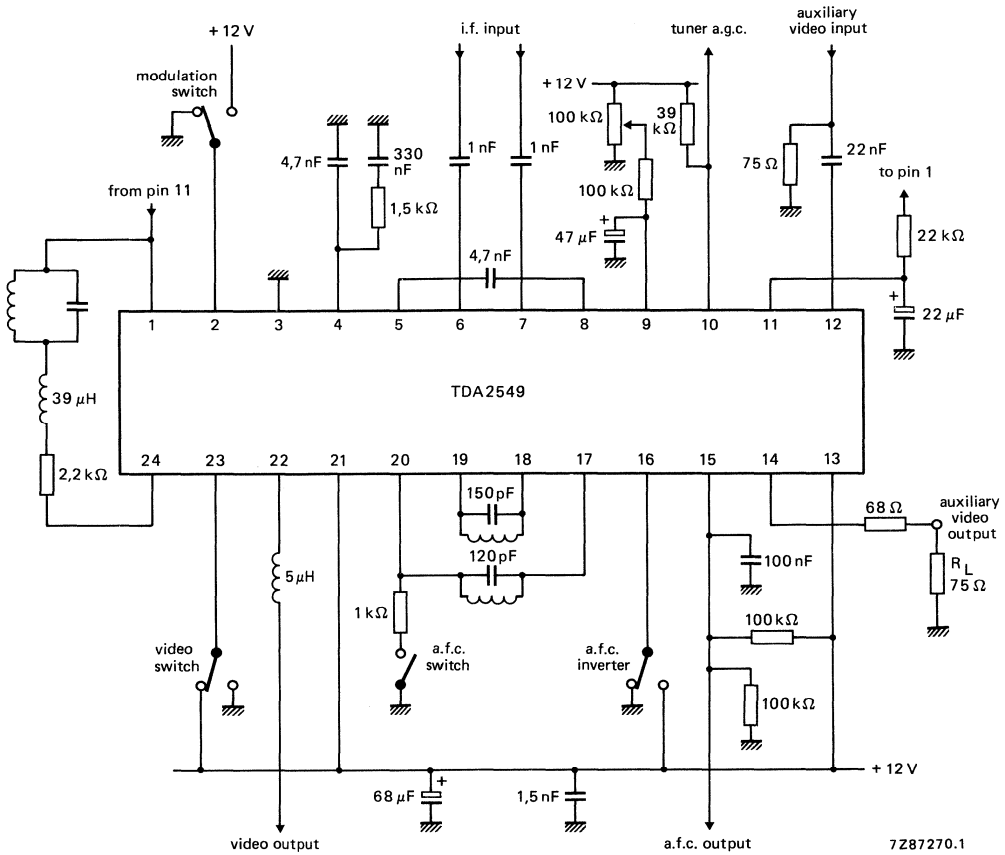


Fig. 5 Application diagram.

DUAL TV SOUND DEMODULATOR CIRCUITS

GENERAL DESCRIPTION

The circuits incorporate two FM demodulator systems to perform the demodulator functions required in a dual sound carrier TV system for demodulating the sound carriers.
The difference between TDA2555 and TDA2557 is the number of stages of the limiting amplifier.

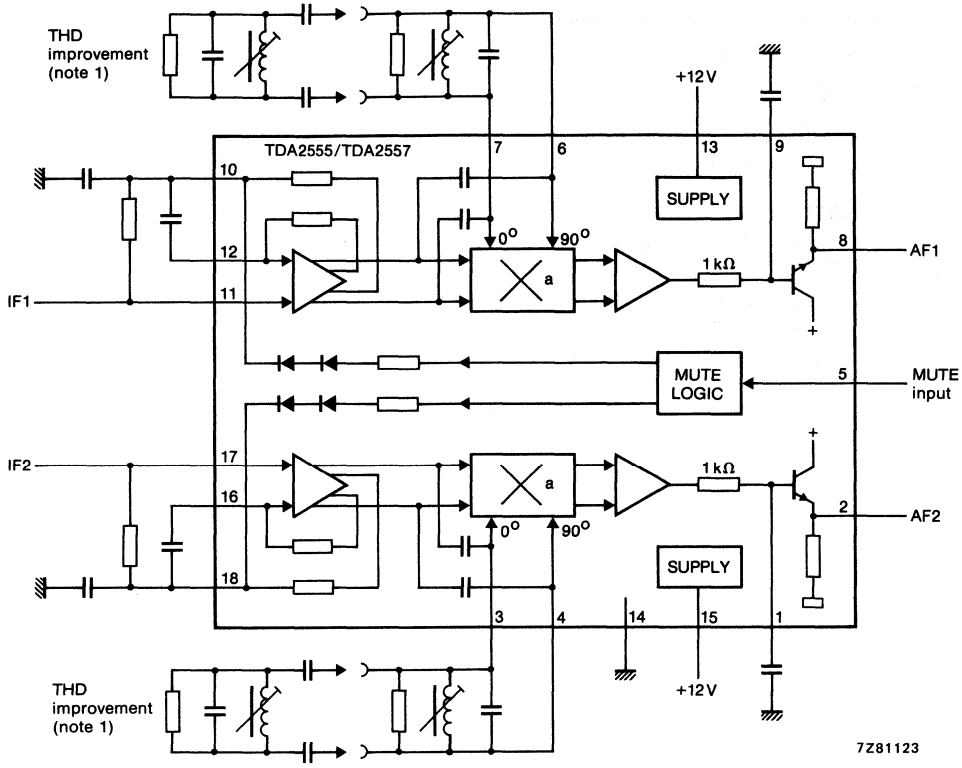
- **Eight** (TDA2555) or **five** (TDA2557) stage limiting amplifier
- Quadrature demodulator for FM detection
- De-emphasis stage
- Output amplifier
- Mute function for each FM demodulator

QUICK REFERENCE DATA

Supply voltage (pins 13 and 15)	V_P	typ.	12	V
Supply current (pins 13 and 15)	I_P	typ.	24,5	mA
AF output voltage (pins 2 and 8)	$V_{o(rms)}$	typ.	600	mV
Total harmonic distortion (note 1)	THD	<	0,1	%
Signal to weighted noise ratio	(S + N)/N	typ.	70	dB

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



a = QUADRATURE DEMODULATOR

Fig. 1 Block diagram.
TDA2555 with 8-stage limiting amplifier;
TDA2557 with 5-stage limiting amplifier.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pins 13 and 15)	V_P	max.	13,2	V
Total power dissipation	P_{tot}	max.	400	mW
Storage temperature range	T_{stg}	−40 to	+ 150	°C
Operating ambient temperature	T_{amb}	0 to	+ 70	°C

CHARACTERISTICS

$V_P = V_{13, 15-14} = 12$ V; $T_{amb} = 25$ °C; $f_{IF1} = 5{,}5$ MHz; $f_{IF2} = 5{,}74$ MHz; $f_{m1} = 1$ kHz;
$\Delta f = \pm 30$ kHz;
$V_{i(rms)} = 5$ mV for TDA2555;
$V_{i(rms)} = 10$ mV for TDA2557;
see test circuit Fig. 3, voltages with respect to ground (pin 14), unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Total current consumption	$I_{13,15}$	18	24,5	30	mA
LIMITING AMPLIFIER					
Maximum input voltage	$V_{11\text{-}12(rms)}$ $V_{16\text{-}17(rms)}$	–	200	–	mV
Input voltage for start of limiting (3 dB AF signal reduction)					
TDA2555	$V_{11\text{-}12(rms)}$ $V_{16\text{-}17(rms)}$	–	50	100	μV
TDA2557	$V_{11\text{-}12(rms)}$ $V_{16\text{-}17(rms)}$	–	250	500	μV
DC voltage (input limiting amplifier) pins 11, 12, 16, 17 to 14	V_i	–	2,0	–	V
DC voltage (feedback loop)	$V_{10,18\text{-}14}$	–	2,0	–	V
FM DEMODULATOR					
IF reference signal voltage	$V_{3\text{-}4(rms)}$ $V_{6\text{-}7(rms)}$	–	200	–	mV
DC voltage	$V_{3,4,6,7\text{-}14}$	–	3,1	–	V
AF output voltage	$V_{2\text{-}14(rms)}$	450	600	750	mV
Difference of output signals	$\frac{V_{2\text{-}14}}{V_{8\text{-}14}}$	–	± 0,1	± 0,5	dB
Total harmonic distortion at outputs AF1 and AF2 (note 1)	THD	–	–	0,5	%
A.M. suppression at outputs AF1 and AF2, $f_{FM} = 70$ Hz; $\Delta f = \pm 50$ kHz; $f_{AM} = 1$ kHz; m = 0,3	AMS	50	–	–	dB

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
FM DEMODULATOR (continued)					
Signal to noise ratio at outputs AF1 and AF2 (CCIR weighted, quasi peak)	$(S+N)/N$	65	70	–	dB
Residual IF-signal without deemphasis	$V_{2,8\text{-}14(rms)}$	–	30	–	mV
Ripple rejection at outputs AF1 and AF2 f = 50 Hz to 20 kHz; $V_{i(rms)}$ = 200 mV	RR	–	40	–	dB
AUDIO OUTPUT STAGE					
emitter follower with 1,0 mA bias current					
DC output voltage	$V_{2,8\text{-}14}$	3,0	4,0	5,0	V
External DC load resistance	$R_{2,8\text{-}14}$	2	–	–	kΩ
AC output current (note 2)	$-I_{2,8\text{-}14(p\text{-}p)}$	–	–	0,5	mA
Deemphasis input resistance (note 3)	$R_{1,9\text{-}14}$	0,8	1,0	1,2	kΩ
DC voltage (deemphasis)	$V_{1,9\text{-}14}$	3,7	4,7	5,7	V
Crosstalk attenuation f = 1 kHz (note 4)	$\alpha_{12,21}$	60	–	–	dB
Crosstalk attenuation f = 10 kHz (note 4)	$\alpha_{12,21}$	60	–	–	dB
Output impedance	$R_{2,8\text{-}14}$	–	25	–	Ω
AF output level (Fig. 2, note 5) MUTE function $V_{i(rms)} < 60$ mV	α	60	–	–	dB
Switching input current					
$V_{5\text{-}14} = 0$ V	$-I_5$	–	–	500	μA
$V_{5\text{-}14} = V_P$	I_5	–	–	500	μA
Internal d.c. voltage no mute (pin 5 not connected)	$V_{5\text{-}14}$	–	6,2	–	V

Notes to the characteristics

1. THD < 0,1% requires a double tuned demodulator circuit (Q_L = 20). With a single tuned circuit a THD of < 0,5% is possible (see Figs 1 and 3).
2. If higher a.c. output current is required an external resistor must be applied from output (pins 2 and 8) to ground (min. 2 kΩ) in order to improve the THD performance ($-I_{2,8} < 4$ mA).
3. The deemphasis time constant is 50 μs.
4. Crosstalk attenuation is defined as:

$$o_{12} = \frac{V_{2\text{-}14} \text{ unmodulated}}{V_{8\text{-}14}} \qquad o_{21} = \frac{V_{8\text{-}14} \text{ unmodulated}}{V_{2\text{-}14}}.$$

5. In the MUTE state the a.f. output level attenuation is more than 60 dB. The MUTE function is only guaranteed for an r.m.s. value of the input voltage lower than 60 mV. See also Fig. 2.

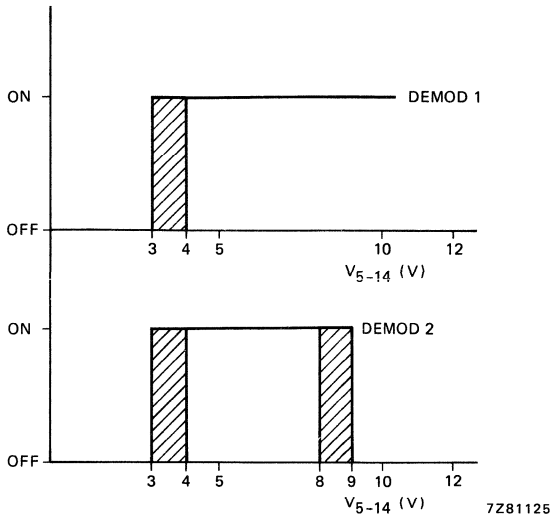


Fig. 2 Mute function.

DEVELOPMENT DATA

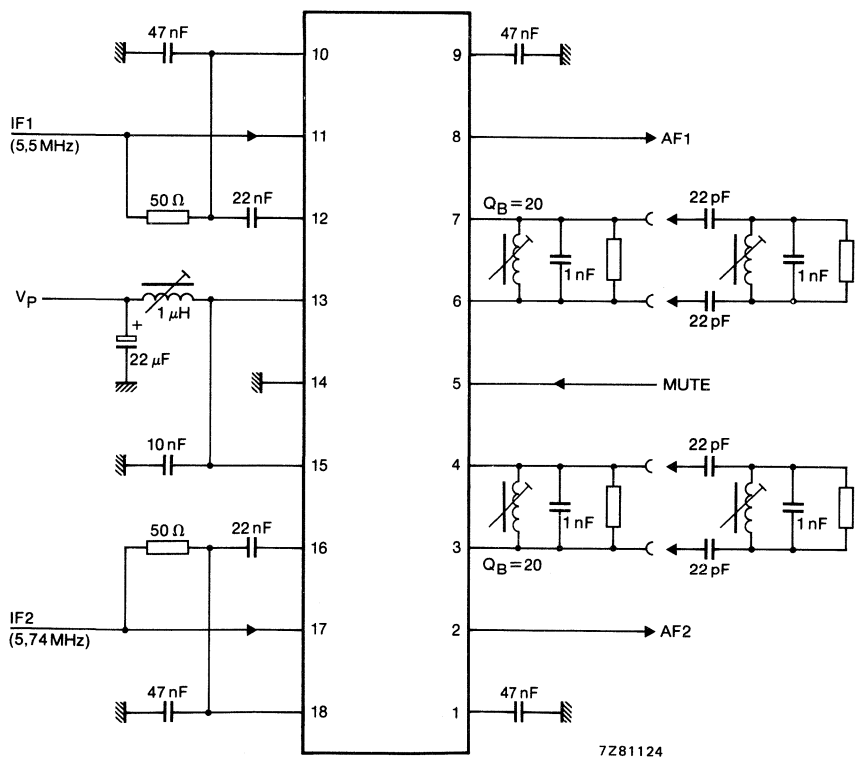


Fig. 3 Test and application circuit.

QUASI-SPLIT-SOUND CIRCUIT WITH DUAL SOUND DEMODULATORS

GENERAL DESCRIPTION

The TDA2556 is a monolithic integrated circuit for quasi-split-sound processing, including two FM demodulators, for two carrier stereo TV receivers and VTR.

Features

First IF (vision carrier plus sound carrier).

- 3 stage gain controlled IF amplifier
- AGC circuit
- Reference amplifier and limiter amplifier for vision carrier (V.C.) processing
- Linear multiplier for quadrature demodulation

Second IF (two separate channels for both FM sound signals).

- 4-stage-limiting amplifier
- Quadrature demodulator
- AF amplifier with de-emphasis
- Output buffer
- Muting for one or both AF outputs

QUICK REFERENCE DATA

Supply voltage, pin 23	$V_P = V_{23-24}$	typ.	12	V
Supply current, pin 23	$I_P = I_{23}$	typ.	73	mA
Minimum IF vision carrier input voltage (rms value)	$V_{VC} = V_{3-4}$	typ.	150	μV
IF control range	ΔG_V	typ.	64	dB
AF output voltage	$V_{O\ 10,\ 15-24(rms)}$	typ.	600	mV
Signal-to-weighted-noise ratio (relative to 1 kHz; 30 kHz deviation)				
at 5,5 MHz } for 2T/20T pulses with white bars	S + W/W	typ.	58	dB
at 5,74 MHz } for 2T/20T pulses with white bars	S + W/W	typ.	56	dB

PACKAGE OUTLINE

24-lead DIL; plastic (SOT101B).

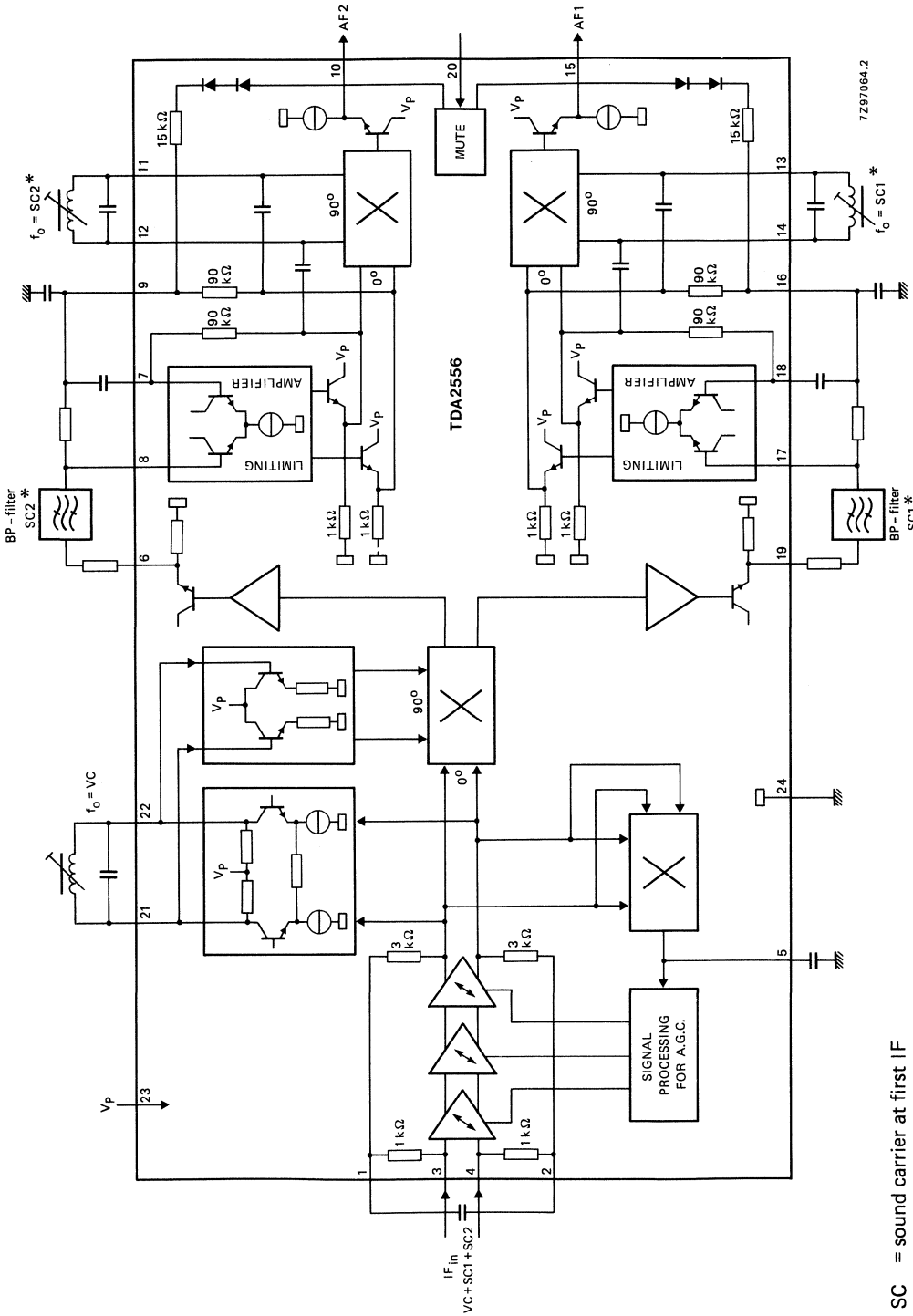


Fig. 1 Block diagram.

SC = sound carrier at first IF
SC* = sound carrier at second IF

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage, pin 23	$V_P = V_{23-24}$	max.	13,2	V
Supply current, pin 23	$I_P = I_{23}$	max.	95	mA
Storage temperature range	T_{stg}	−25 to	+ 150	°C
Operating ambient temperature range	T_{amb}	0 to	+ 70	°C

CHARACTERISTICS

$V_P = V_{23-24}$ = 12 V; T_{amb} = 25 °C; measured at f_{VC} = 38,9 MHz, f_{SC1} = 33,4 MHz, f_{SC2} = 33,158 MHz.
Vision carrier (V.C.) modulated with different video signals (see below); modulation depth 100% (proportional to 10% residual carrier).
Vision carrier amplitude: $V_{VC(rms)}$ = 10 mV.
Vision-to-sound carrier ratios: VC/SC1 = 13 dB, VC/SC2 = 20 dB.
Sound carrier (SC1, SC2) modulated with f = 1 kHz and deviation $\Delta f = \pm 30$ kHz.
For measuring circuit see Fig. 2; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply (pin 23)					
Supply voltage	$V_P = V_{23-24}$	10,8	12	13,2	V
Supply current	$I_P = I_{23}$	–	73	95	mA
First IF amplifier					
Input voltage for start of gain control (intercarrier signals −3 dB)	$V_{VC} = V_{3-4\ (rms)}$	–	150	200	μV
Input voltage for end of gain control (intercarrier signals + 1 dB)	$V_{VC} = V_{3-4\ (rms)}$	100	250	–	mV
Gain control range	ΔG_V	60	64	–	dB
Control voltage range (see Fig. 6)	V_{5-24}	4	–	V_P	V
Input resistance (differential)	R_{3-4}	–	2	–	kΩ
Input capacitance (differential)	C_{3-4}	–	2	–	pF
Intercarrier signal					
Output voltage; 5,5 MHz (SC1*)	$V_{19-24(rms)}$	60	100	140	mV
Output voltage; 5,742 MHz (SC2*)	$V_{6-24(rms)}$	27	45	63	mV
Output voltage d.c. (emitter follower with minimum 1,5 mA bias current)	$V_{6-24/19-24}$	–	5,9	–	V
Allowable d.c. load resistance	$R_{6-24/19-24}$	7	–	–	kΩ
Second IF					
Input voltage for start of limiting	$V_{8-24/17-24(rms)}$	–	700	–	μV
Maximum input voltage	$V_{8-24/17-24(rms)}$	–	200	–	mV
Voltage level d.c.	$V_{7-24/18-24}$	–	2,2	–	V
Voltage level d.c.	$V_{9-24/16-24}$	–	2,2	–	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Second IF (continued)					
AF output voltage	$V_{10\text{-}24/15\text{-}24}$	450	600	810	mV
Output voltage d.c. (emitter follower with 1,0 mA bias current)	$V_{10\text{-}24/15\text{-}24}$	–	4,5	–	V
External d.c. load resistance	$R_{10\text{-}24/15\text{-}24}$	2	–	–	kΩ
External a.c. load current (note 5)	$I_{10/15}$	–	–	0,5	mA
Total harmonic distortion of $V_{10\text{-}24/15\text{-}24}$ (note 3)	THD	–	0,4	1	%
(note 4)	THD	–	–	0,1	%
AM suppression; f_{AM} = 1 kHz, M = 0,3; f_{FM} = 70 Hz; f = ± 50 kHz (note 2)		50	60	–	dB
Crosstalk attenuation (note 2)		60	–	–	dB
S/N ratio (second IF) (note 2) f = 1 kHz; f = ± 50 kHz	$V_{10\text{-}24/15\text{-}24}$	65	70	–	dB
Mute (see Fig. 4)					
Switching voltage for:					
demodulator 1 ON	$V_{20\text{-}24}$	4	–	V_P	V
demodulator 1 OFF	$V_{20\text{-}24}$	0	–	3	V
demodulator 2 ON	$V_{20\text{-}24}$	4	–	8	V
demodulator 2 OFF	$V_{20\text{-}24}$	0 or 9	–	3 or V_P	V
Input current	I_{20}	–500	–	+ 200	μA
Input d.c. potential	$V_{20\text{-}24}$	–	6,3	–	V
AF signal performance, weighted S/N ratio at audio outputs, pins 10, 15; $V_{3\text{-}4}$ = 20 mV rms weighted according to CCIR 468-2, quasi-peak, (see note 1)					
(a) 2T/20T pulse with white bars (see also Fig. 5)					
at 5,5 MHz	(S + W)/W	–	58	–	dB
at 5,74 MHz	(S + W)/W	–	56	–	dB
(b) 6 kHz sine wave					
at 5,5 MHz	(S + W)/W	–	52	–	dB
at 5,74 MHz	(S + W)/W	–	50	–	dB
(c) black level (sync pulses only)					
at 5,5 MHz	(S + W)/W	–	65	–	dB
at 5,74 MHz	(S + W)/W	–	63	–	dB

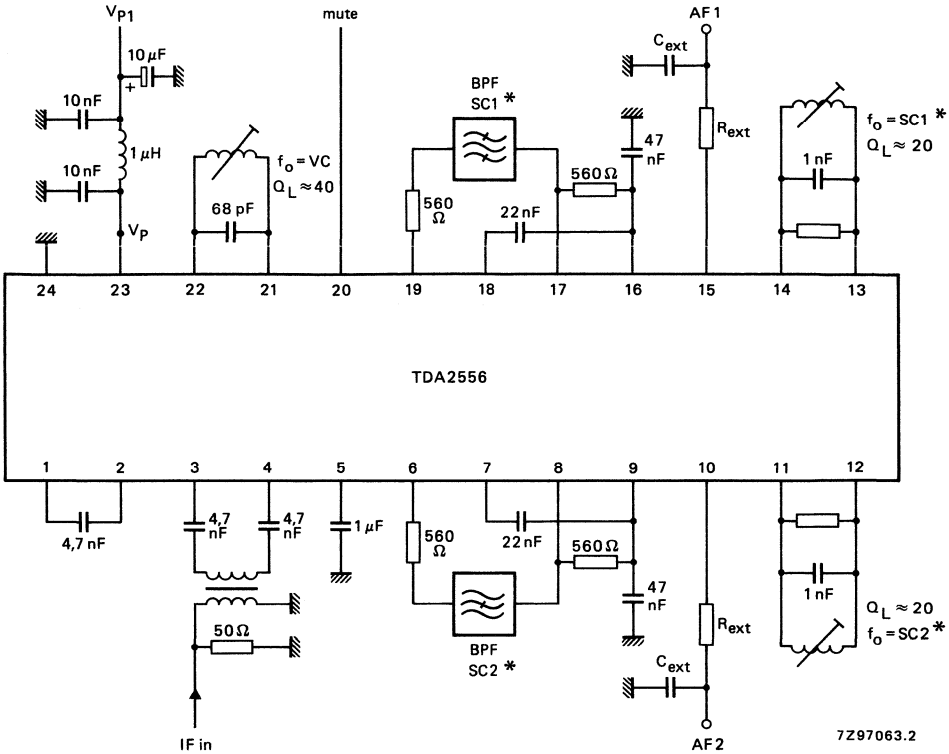


Fig. 2 Application diagram ($\tau_{deemph} = R_{ext} \cdot C_{ext}$)
(Input transformer "IF in" only for testing)

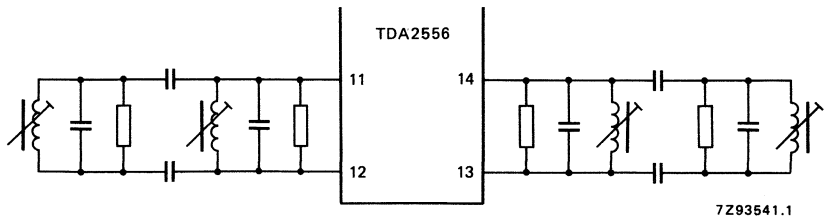


Fig. 3 Distortion improvement (see note 3 and 4).

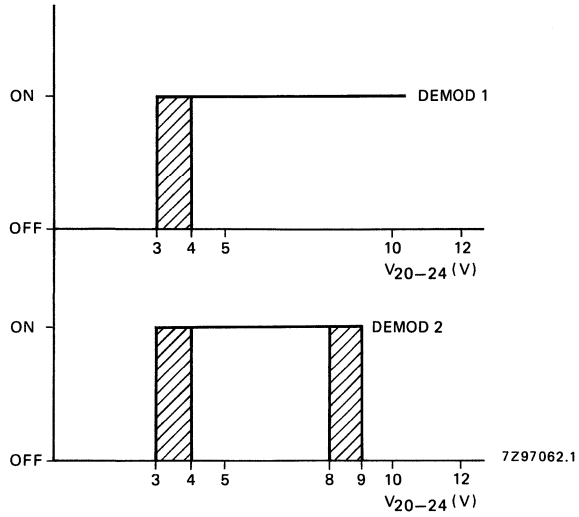


Fig. 4 Mute function.

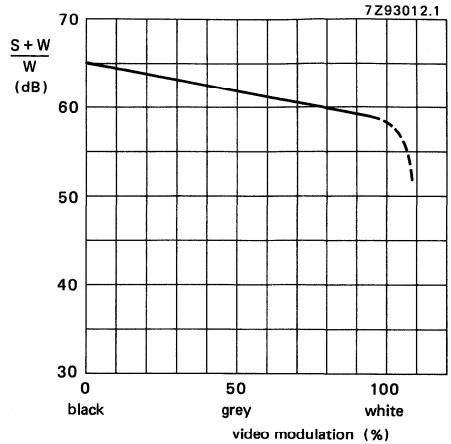


Fig. 5 Signal to weighted noise ratio depending on video modulation.

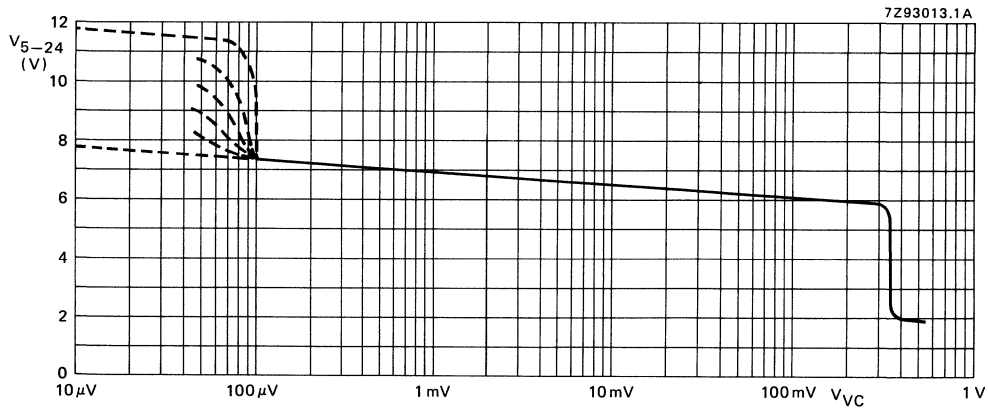


Fig. 6 Control voltage at pin 5 as a function of the input voltage $V_{VC} = V_{3\text{-}4(rms)}$.

Notes to the characteristics

1. Incidential phase on the vision carrier, caused by the TV transmitter, has to be less than 0,5 degrees for black and white transient; this is equivalent to S + W/W = 56 dB for a 6 kHz sine wave.
2. Input signal second IF $V_{8\text{-}24/17\text{-}24}$ = 10 mVrms.
3. THD value is valid for ceramic bandpass filters of SC* and single resonance circuits at pins 11 and 12 and pins 13 and 14.
4. THD value is valid for LC bandpass filters of SC* and double resonance circuits at pins 11 and 12 and pins 13 and 14.
5. If higher a.c. output current is required an external resistor has to be applied from output (pins 10 and 15) to ground (minimum 2 kΩ) in order to improve the THD performance.

SYNCHRONIZATION CIRCUIT WITH VERTICAL OSCILLATOR AND DRIVER STAGES

GENERAL DESCRIPTION

The TDA2577A separates the vertical and horizontal sync pulses from the composite TV video signal and uses them to synchronize horizontal and vertical oscillators.

Features

- Horizontal sync separator and noise inverter
- Horizontal oscillator
- Horizontal output stage
- Horizontal phase detector (sync to oscillator)
- Time constant switch for phase detector (fast time constant during catching)
- Slow time constant for noise only conditions
- Time constant externally switchable (e.g. fast for VCR)
- Inhibit of horizontal phase detector and video transmitter identification circuit during vertical oscillator flyback
- Second phase detector ($\varphi 2$) for storage compensation of horizontal deflection stage
- Sandcastle pulse generator (3-levels)
- Video transmitter identification circuit
- Stabilizer and supply circuit for starting the horizontal oscillator and output stage directly from the mains rectifier
- Duty factor of horizontal output pulse is 50% when flyback pulse is absent
- Vertical sync separator
- Bandgap 6,5 V reference voltage for vertical oscillator and comparator
- Synchronized vertical oscillator/sawtooth generator (synchronization inhibited when no video transmitter is detected)
- Internal circuit for 3% parabolic pre-correction of the oscillator/sawtooth generator. Comparator supplied with pre-corrected sawtooth and external feedback input
- Vertical comparator with internal 3% pre-correction circuit for vertical oscillator/sawtooth generator
- Vertical driver stage
- Vertical blanking pulse generator with external adjustment of pulse duration (50 Hz: 21 lines; 60Hz: 17 lines)
- Vertical guard circuit

QUICK REFERENCE DATA

Supply				
Minimum current required to start horizontal oscillator and output stage (pin 16)	I_{16}	>	4,5	mA
Main supply voltage (pin 10)	$V_P = V_{10-9}$	typ.	12	V
Supply current	$I_P = I_{10}$	typ.	55	mA
Input signals				
Sync pulse input voltage (peak-to-peak value; negative-going)	$V_{5-9(p-p)}$		0,15 to 1	V
Output signals				
Horizontal output pulse (open collector) at I_{11} = 40 mA	V_{11-9}	<	0,5	V
Vertical output pulse (emitter-follower) at I_1 = 10 mA	V_{1-9}	>	4	V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

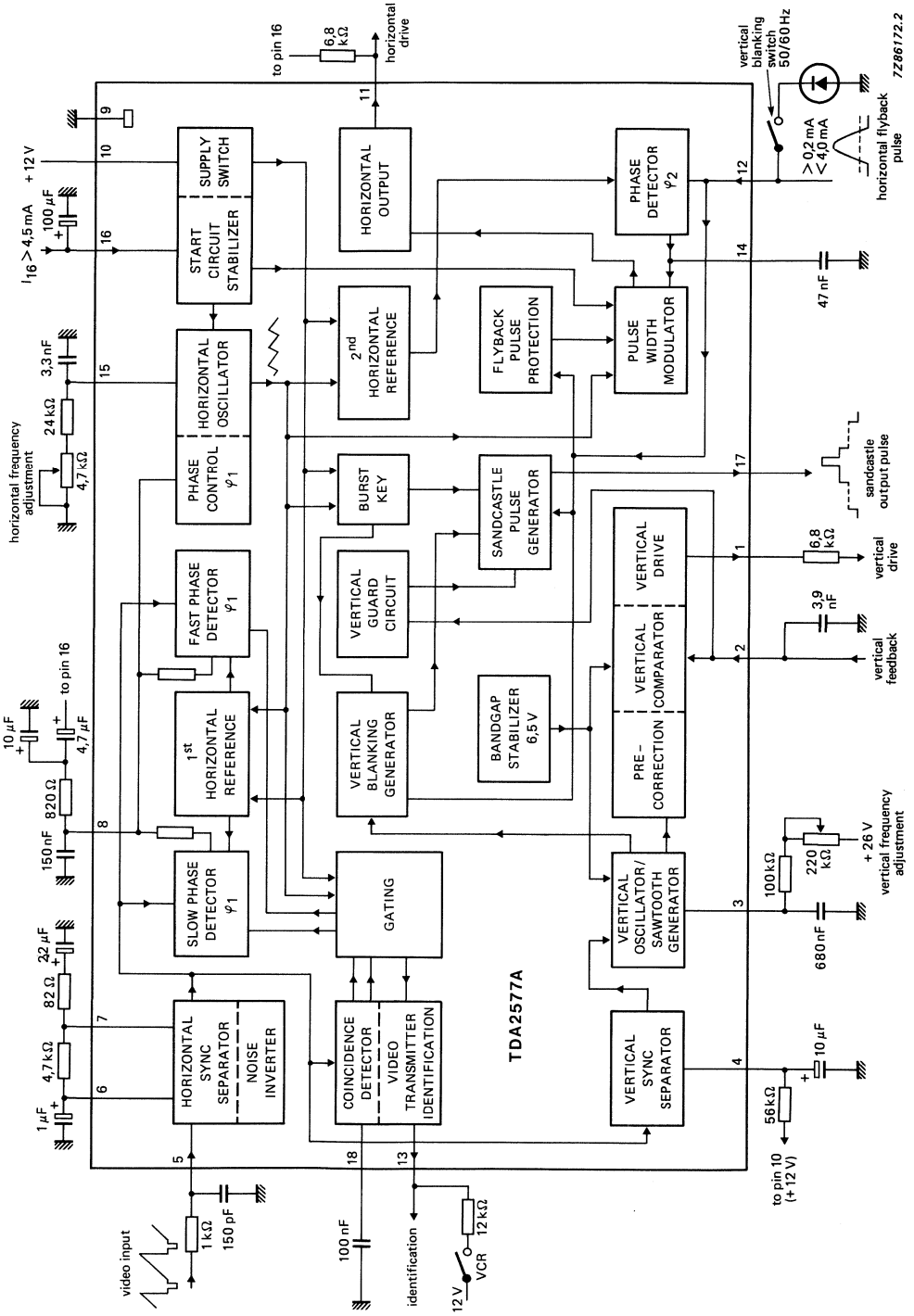


Fig. 1 Block diagram.

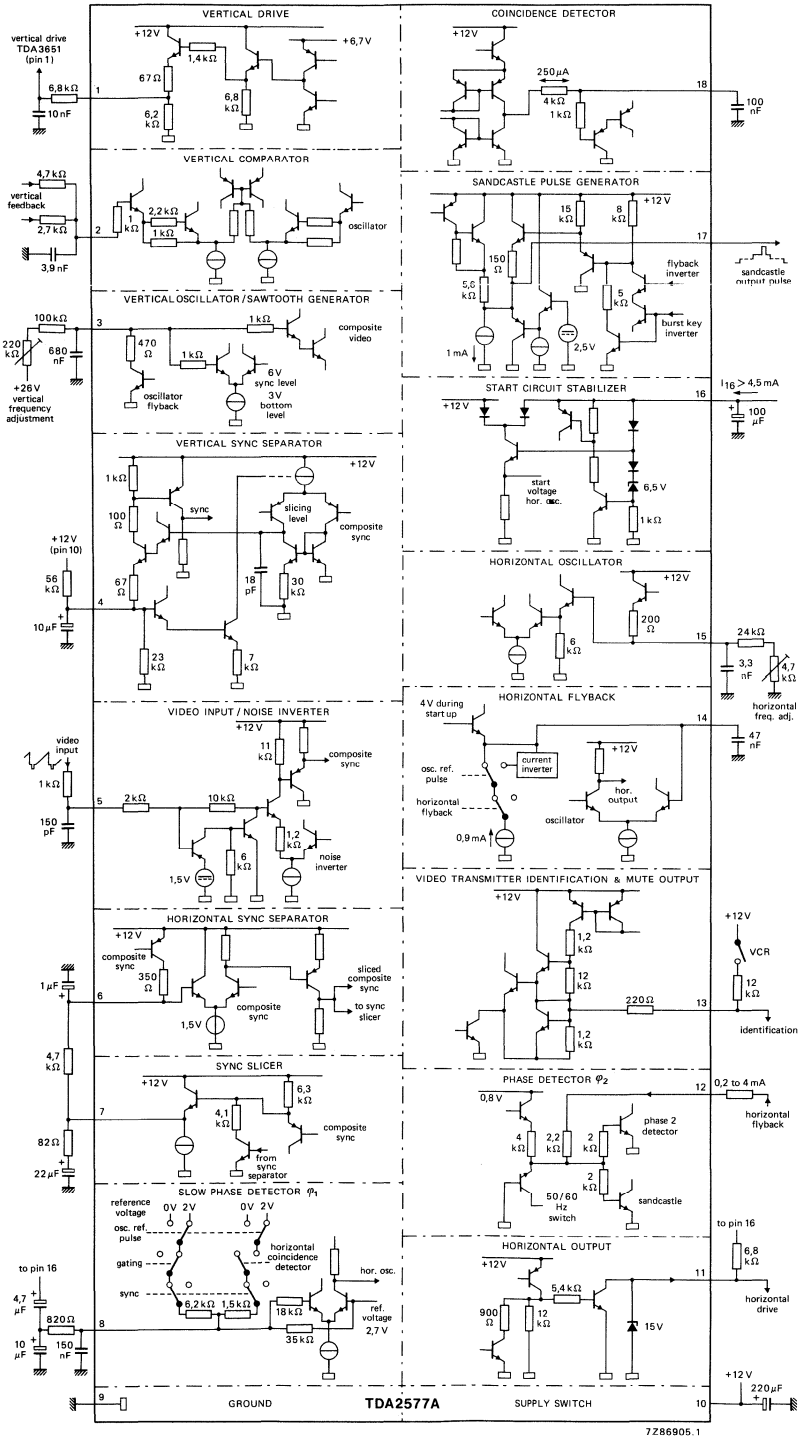


Fig. 2 TDA2577A circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Start current (pin 16)	I_{16}	max.	8	mA
Supply voltage (pin 10)	$V_P = V_{10-9}$	max.	13,2	V
Total power dissipation	P_{tot}	max.	1,1	W
Storage temperature range	T_{stg}		−55 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 65	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	typ.	50	K/W

CHARACTERISTICS

I_{16} = 5 mA; V_P = 12 V; T_{amb} = 25 °C; unless otherwise specified

Supply

Supply current at pin 16	I_{16}		4,5 to 8	mA
Stabilized supply voltage (pin 16)	V_{16-9}	typ.	8,7	V
			8,0 to 9,5	V
Supply current (pin 10)	I_{10}	typ.	55	mA
		<	70	mA
Supply voltage (pin 10)	$V_P = V_{10-9}$	typ.	12	V
			10 to 13,2	V

Video input (pin 5)

Top-sync level	V_{5-9}	typ.	3,1	V
			1,5 to 3,75	V
Sync pulse amplitude (peak-to-peak value) (note 1)	$V_{5-9(p-p)}$	typ.	0,6	V
			0,15 to 1	V
Slicing level		typ.	50	%
			35 to 65	%
Delay between video input and detector output	t_1	typ.	0,35	μs

Noise gate (pin 5)

Switching level	V_{5-9}	typ.	0,7	V
		<	1	V

First control loop (sync to oscillator; pin 8)

Holding range	Δf	typ.	± 800	Hz
Catching range	Δf	typ.	± 800	Hz
			±600 to ±1100	Hz
Control sensitivity video with respect to oscillator, burst key and flyback pulse				
for slow time constant		typ.	1	kHz/μs
for fast time constant		typ.	2,75	kHz/μs

Second control loop (horizontal output to flyback; pin 14)			
Control sensitivity; static (see note 2)	$\Delta t_d/\Delta t_o$	typ.	400 μs/μs
Control range	t_d		1 to 50 μs
Controlled edge	negative		
Phase adjustment (via 2nd control loop; pin 14)			
Control sensitivity		typ.	25 μA/μs
Maximum permissible control current	$\pm I_{14}$	<	60 μA
Horizontal oscillator (pin 15)			
Frequency (no sync)	f_{osc}	typ.	15 625 Hz
Frequency spread (C_{osc} = 3,3 nF; R_{osc} = 24 kΩ)	Δf_{osc}	<	4 %
Frequency deviation between starting point of output signal and stabilized condition	Δf_{osc}	typ. <	6 % 8 %
Temperature coefficient	TC	typ.	$1 \cdot 10^{-4}$ K^{-1}
Horizontal output (pin 11)			
Output voltage; high level	V_{11-9}	<	13,2 V
Voltage at which protection starts	V_{11-9}		13 to 15,8 V
Output voltage; low level start condition at I_{11} = 10 mA	V_{11-9}	typ. <	0,3 V 0,5 V
normal condition at I_{11} = 40 mA	V_{11-9}	typ. <	0,3 V 0,5 V
Duty factor of output signal during starting (no phase shift; voltage at pin 11 low)	δ	typ.	65 %
Duty factor of output signal without flyback pulse	δ	typ.	50 % 47 to 57 %
Controlled edge	negative		
Duration of output pulse (see Fig. 3)			$t_d + t_o + 2,5$ μs
Sandcastle output pulse (pin 17)			
Output voltage during: burst key	V_{17-9}	>	10 V
horizontal blanking	V_{17-9}	typ.	4,6 V 4,2 to 5 V
vertical blanking	V_{17-9}	typ.	2,5 V 2 to 3 V
Pulse duration burst key	t_p	typ.	3,7 μs 3,3 to 4,1 μs
horizontal blanking	flyback pulse (see note 3)		
vertical blanking for 50 Hz application ($-I_{12}$: 0 to 0,1 mA) for 60 Hz application ($-I_{12}$: typ. 0,2 mA)			21 lines 17 lines

CHARACTERISTICS (continued)

Delay between the start of the sync at the video input and the rising edge of the burst key pulse	t_2	typ. 4,8 to 5,6	5,2 µs µs
Delay between the start of the sync and the trailing edge of the burst key	t_2	typ. 8,1 to 9,3	8,8 µs µs
Coincidence detector; video transmitter identification circuit; time constant switches (pin 18); see also Fig. 2			
Detector output current	$\pm I_{18}$	typ.	300 µA
Voltage during noise (note 4)	V_{18-9}	typ.	0,3 V
Voltage level for in-sync condition	V_{18-9}	typ.	7,5 V
Switching level slow to fast	V_{18-9}	typ. 3,2 to 3,8	3,5 V V
Switching level mute function active; φ_1 fast to slow	V_{18-9}	typ. 1,0 to 1,4	1,2 V V
vertical period counter 3 periods fast	V_{18-9}	typ. 0,08 to 0,16	0,12 V V
Switching level slow to fast (locking) mute function inactive	V_{18-9}	typ. 1,5 to 1,9	1,7 V V
Switching level fast to slow (locking)	V_{18-9}	typ. 4,7 to 5,3	5,0 V V
Switching level for VCR (fast time constant) without mute function	V_{18-9}	typ. 8,2 to 9,0	8,6 V V
Video transmitter identification output (pin 13)			
Output voltage active (no sync) at I_{13} = 1 mA	V_{13-9}	$>$ typ.	10 V 11 V
Output voltage active (no sync) at I_{13} = 5 mA	V_{13-9}	$>$ typ.	7 V 10 V
Output voltage inactive	V_{13-9}	$<$ typ.	0,5 V 0,1 V
VCR switching (pin 13)			
Input current for fast time constant phase detector φ_1, with mute function active	I_{13}	typ. 0,4 to 0,8	0,6 mA mA
Flyback input pulse (pin 12)			
Switching level	V_{12-9}	typ.	1 V
Input current	I_{12}		0,2 to 4 mA
Input pulse amplitude (peak-to-peak value)	$V_{12-9(p-p)}$	$<$	12 V
Input resistance	R_{12-9}	typ.	2,7 kΩ
Delay time of sync pulse (measured in φ_1) to flyback at switching level; t_{fl} = 12 µs (see also note 2 and Fig. 4)	t_o	typ.	1,3 µs

Duration of vertical blanking pulse (pin 12)

Required input current (negative)			
for 50 Hz application; 21 lines blanking	$-I_{12}$	typ.	0,2 mA
		$>0,15$ to $<0,3$	mA
for 60 Hz application; 17 lines blanking	$-I_{12}$	$<$	0,1 mA
Maximum allowed input current	$-I_{12}$	$<$	0,4 mA

Vertical sawtooth generator (pin 3)

Vertical frequency (no sync)	f_s	typ.	46 Hz
Frequency spread (C_{osc} = 680 nF; R_{osc} = 187 kΩ; at + 26 V)	Δf_s	$<$	4 %
Synchronization range		typ.	22 %
Input current at V_{3-9} = 6 V	I_3	$<$	2 μA
Frequency shift for V_P = 10 to 13 V	Δf_s	$<$	0,2 %
Temperature coefficient	TC	typ.	$1 \cdot 10^{-4}$ K^{-1}

Comparator (pin 2)

Input voltage; d.c. level	V_{2-9}	typ.	4,4 V
			4,0 to 4,8 V
a.c. level (peak-to-peak value)	$V_{2-9(p-p)}$	typ.	1,5 V
Input current at V_{2-9} = 6 V	I_2	$<$	2 μA
Sawtooth internal pre-correction (parabolic convex)		typ.	3 %

Vertical output stage; emitter follower (pin 1)

Output voltage at I_1 = 10 mA	V_{1-9}	typ.	3,6 V
			3,2 to 5 V
Output current	I_1	$<$	20 mA

Vertical guard circuit

Activating voltage levels (vertical blanking level is 2,5 V)

switching level low	V_{2-9}	typ.	3 V
			2,7 to 3,3 V
switching level high	V_{2-9}	typ.	5,8 V
			5,4 to 6,3 V

Notes to characteristics

1. Up to 1 V peak-to-peak the slicing level is constant; at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.
2. t_d = delay between negative transient of horizontal output pulse and the rising edge of the flyback pulse.
   t_o = delay between the rising edge of the flyback pulse and the start of the current in φ_1 (pin 8).
3. The duration of the flyback pulse is measured at the input switching level, which is about 1 V (t_{fl}).
4. Depends on d.c. level at pin 5; value given applicable for $V_{5-9} \approx 5$ V.

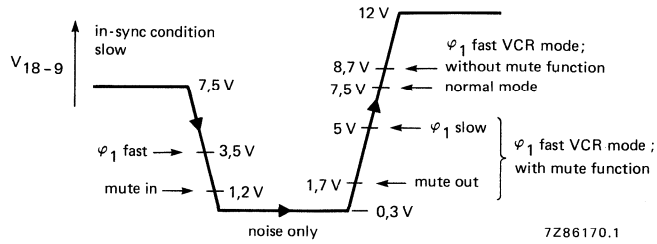


Fig. 3 Voltage levels at pin 18 (V_{18-9}).

APPLICATION INFORMATION

The TDA2577A generates the signal for driving the horizontal deflection output circuit. It also contains a synchronized vertical sawtooth generator for direct drive of the vertical deflection output stage.

The horizontal oscillator and output stage can start operating on a very low supply current ($I_{16} \geqslant 4{,}5$ mA), which can be taken directly from the mains rectifier. Therefore, it is possible to derive the main supply (pin 10) from the horizontal deflection output stage. The duty factor of the horizontal output signal is about 65% during the starting-up procedure. After starting-up, the second phase detector (φ_2) is activated to control the timing of the negative-going edge of the horizontal output signal.

A bandgap reference voltage (6,5 V) is provided for supply and reference of the vertical oscillator and comparator stage.

The slicing level of the horizontal sync separator is independent of the amplitude of the sync pulse at the input. The resistor between pins 6 and 7 determines its value. A 4,7 kΩ resistor gives a slicing level at the middle of the sync pulse. The nominal top sync level at the input is 3,1 V. The amplitude selective noise inverter is activated at a level of 0,7 V.

Good stability is obtained by means of the two control loops. In the first loop, the phase of the horizontal sync signal is compared with a waveform of which the rising edge refers to the top of the horizontal oscillator signal. In the second loop, the phase of the flyback pulse is compared with another reference waveform, the timing of which is such that the top of the flyback pulse is situated symmetrically on the horizontal blanking interval of the video signal. Therefore the first loop can be designed for a good noise immunity, whereas the second loop can be as fast as desired for compensation of switch-off delays in the horizontal output stage.

The first phase detector is gated with a pulse derived from the horizontal oscillator signal. This gating (slow time constant) is switched off during catching. Also, the output current of the phase detector is increased fivefold, during the catching time and VCR conditions (fast time constant). The first phase detector is inhibited during the retrace time of the vertical oscillator.

The in-sync, out-of-sync or no video condition is detected by the video transmitter identification/coincidence detector circuit (pin 18). The voltage on pin 18 defines the time constant and gating of the first phase detector. The relationship between this voltage and the various switching levels is shown in Fig. 3. The complete survey of the switching actions is given in Table 1.

APPLICATION INFORMATION (continued)

Table 1 Switching levels at pin 18.

voltage at pin 18	first phase detector $\varphi 1$				mute output at pin 13		receiving conditions
	time constant		gating				
	slow	fast	on	off	on	off	
7,5 V	X		X			X	video signal detected
7,5 to 3,5 V	X		X			X	video signal detected
3,5 to 1,2 V		X		X		X	video signal detected
1,2 to 0,1 V	X		X		X		noise only
0,1 to 1,7 V	X	*	X	*	X		new video signal detected
1,7 to 5,0 V		X		X		X	horizontal oscillator locked
							VCR playback with mute function
5,0 to 7,5 V	X		X			X	horizontal oscillator locked
8,7 V		X		X		X	VCR playback without mute function

Where: * = 3 vertical periods.

The stability of displayed video information (e.g. channel number), during noise only conditions, is improved by the first phase detector time constant being set to slow.

The average voltage level of the video input on pin 5 during noise only conditions should not exceed 5,5 V otherwise the time constant switch may be set to fast due to the average voltage level on pin 18 dropping below 0,1 V. When the voltage on pin 18 drops below 100 mV a counter is activated which sets the time constant switch to fast, and not gated for 3 vertical periods. This condition occurs when a new video signal is present at pin 5. When the horizontal oscillator is locked the voltage on pin 18 increases. Nominally a level of 5 V is reached within 15 ms (1 vertical period). The mute switching level of 1,2 V is reached within 5 ms (C_{18} = 47 nF). If the video transmitter identification circuit is required to operate under VCR playback conditions the first phase detector can be set to fast by connecting a resistor of 180 kΩ between pin 18 and ground. Also a current of 0,6 mA into pin 13 sets the first phase detector to fast without affecting the mute output function (active HIGH with no video signal detected). For VCR playback without mute function, the first phase detector can be set to fast by connecting a resistor of 1 kΩ to the supply (pin 10).

The supply for the horizontal oscillator (pin 15) and horizontal output stage (pin 11) is derived from the voltage at pin 16 during the start condition. The horizontal output signal starts at a nominal supply current into pin 16 of 3,8 mA, which will result in a supply voltage of about 5,5 V (for guaranteed operation of all devices $I_{16} > 4{,}5$ mA). It is possible that the main supply voltage at pin 10 is 0 V during starting, so the main supply of the IC can be taken from the horizontal deflection output stage. The start of the other IC functions depends on the value of the main supply voltage at pin 10. At 5,5 V all IC functions start operating except the second phase detector (oscillator to flyback pulse). The output voltage of the second phase detector at pin 14 is clamped by means of an internally loaded n-p-n emitter follower. This ensures that the duty factor of the horizontal output signal (pin 11) remains at about 65%. The second phase detector will close if the supply voltage at pin 10 reaches 8,8 V. At this value the supply current for the horizontal oscillator and output stage is delivered by pin 10, which also causes the voltage at pin 16 to change to a stabilized 8,7 V. This change switches off the n-p-n emitter follower at pin 14 and activates the second phase detector. The supply voltage for the horizontal oscillator will, however, still be referred to the stabilized voltage at pin 16, and the duty factor of the output signal at pin 12 is at the value required by the delay at the horizontal deflection stage. Thus switch-off delays

in the horizontal output stage are compensated. When no horizontal flyback signal is detected the duty factor of the horizontal output signal is 50%.

Horizontal picture shift is possible by externally charging or discharging the 47 nF capacitor connected to pin 14.

The IC also contains a synchronized vertical oscillator/sawtooth generator. The oscillator signal is connected to the internal comparator (the other side of which is connected to pin 2), via an inverter and amplitude divider stage. The output of the comparator drives an emitter-follower output stage at pin 1. For a linear sawtooth in the oscillator, the load resistor at pin 3 should be connected to a voltage source of 26 V or higher. The sawtooth amplitude is not influenced by the main supply at pin 10. The feedback signal is applied to pin 2 and compared to the sawtooth signal at pin 3. For an economical feedback circuit with less picture bounce the sawtooth signal is internally precorrected by 3% (convex) referred to pin 2. The linearity of the vertical deflection current depends upon the oscillator signal at pin 3 and the feedback signal at pin 2.

Synchronization of the vertical oscillator is inhibited when the mute output is present at pin 13.

To minimize the influence of the horizontal part on the vertical part a 6,5 V bandgap reference source is provided for supply and reference of the vertical oscillator and comparator.

The sandcastle pulse, generated at pin 17, has three different voltage levels. The highest level (11 V) can be used for burst gating and black level clamping. The second level (4,6 V) is obtained from the horizontal flyback pulse at pin 12 and used for horizontal blanking. The third level (2,5 V) is used for vertical blanking and is derived by counting the horizontal frequency pulses. For 50 Hz the blanking pulse duration is 21 lines and for 60 Hz it is 17 lines. The blanking pulse duration is set by the negative voltage value of the horizontal flyback pulse at pin 12.

The IC also incorporates a vertical guard circuit, which monitors the vertical feedback signal at pin 2. If this level is below 3 V or higher than 5,8 V, the guard circuit will insert a continuous level of 2,5 V into the sandcastle output signal. This will result in complete blanking of the screen if the sandcastle pulse is used for blanking in the TV set.

APPLICATION INFORMATION (continued)

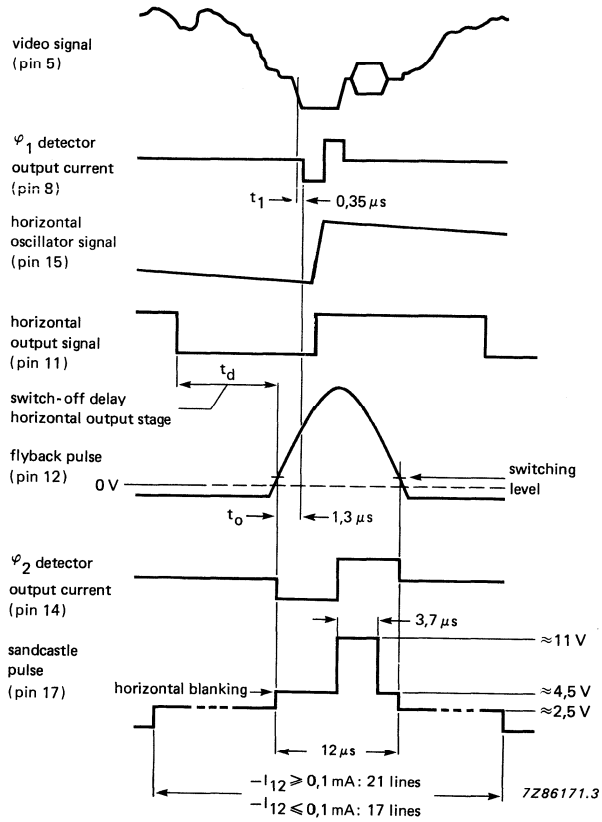


Fig. 4 Timing diagram of the TDA2577A.

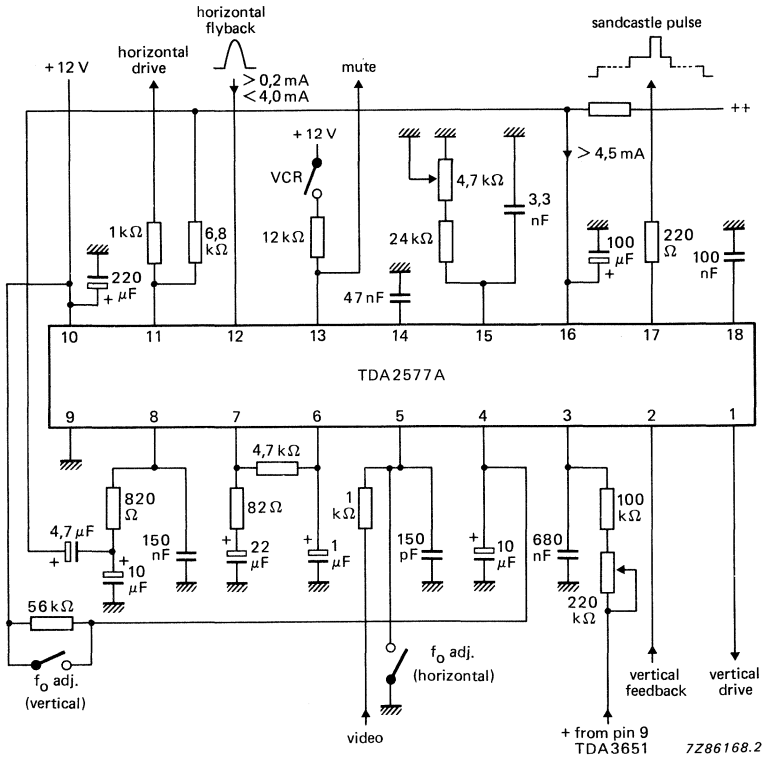


Fig. 5 Typical application circuit diagram; for combination of the TDA2577A with the TDA3651 see Fig. 7.

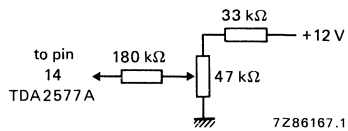


Fig. 6 Circuit configuration at pin 14 for phase adjustment.

APPLICATION INFORMATION (continued)

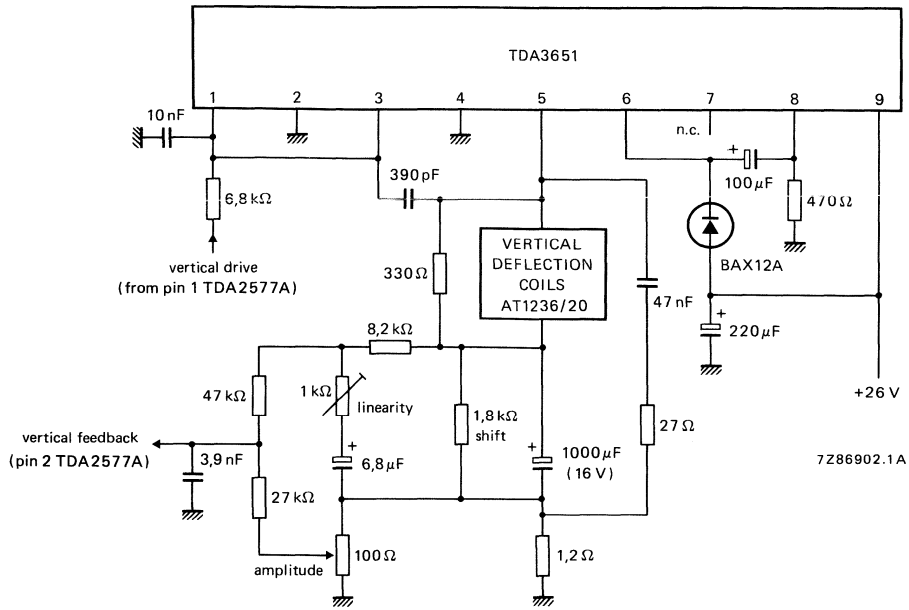


Fig. 7 Typical application circuit diagram of the TDA3651 (vertical output), when used in combination with the TDA2577A (90° application).

SYNCHRONIZATION CIRCUIT WITH VERTICAL OSCILLATOR AND DRIVER STAGES

GENERAL DESCRIPTION

The TDA2578A separates the vertical and horizontal sync pulses from the composite TV video signal and uses them to synchronize horizontal and vertical oscillators.

Features

- Horizontal sync separator and noise inverter
- Horizontal oscillator
- Horizontal output stage
- Horizontal phase detector (sync to oscillator)
- Time constant switch for phase detector (fast time constant during catching)
- Slow time constant for noise only conditions
- Time constant externally switchable (e.g. fast for VCR)
- Inhibit of horizontal phase detector and video transmitter identification circuit during vertical oscillator flyback
- Second phase detector (φ_2) for storage compensation of horizontal deflection stage
- Sandcastle pulse generator (3-levels)
- Video transmitter identification circuit
- Stabilizer and supply circuit for starting the horizontal oscillator and output stage directly from the mains rectifier
- Duty factor of horizontal output pulse is 50% when flyback pulse is absent
- Vertical sync separator
- Bandgap 6,5 V reference voltage for vertical oscillator and comparator
- Synchronized vertical oscillator/sawtooth generator (synchronization inhibited when no video transmitter is detected)
- Internal circuit for 6% parabolic pre-correction of the oscillator/sawtooth generator. Comparator supplied with pre-corrected sawtooth and external feedback input
- Vertical driver stage
- Vertical blanking pulse generator
- 50/60 Hz detector
- 50/60 Hz identification output
- Automatic amplitude adjustment for 60 Hz
- Automatic adjustment of blanking pulse duration (50 Hz: 21 lines; 60 Hz: 17 lines)
- Vertical guard curcuit

QUICK REFERENCE DATA

Supply			
Minimum current required to start horizontal oscillator and output stage (pin 16)	I_{16}	>	4,5 mA
Main supply voltage (pin 10)	$V_P = V_{10-9}$	typ.	12 V
Supply current	$I_P = I_{10}$	typ.	55 mA
Input signals			
Sync pulse input voltage (peak-to-peak value; negative-going)	$V_{5-9(p-p)}$		0,15 to 1 V
Output signals			
Horizontal output pulse (open collector) at I_{11} = 40 mA	V_{11-9}	<	0,5 V
Vertical output pulse (emitter-follower) at I_1 = 10 mA	V_{1-9}	>	4 V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

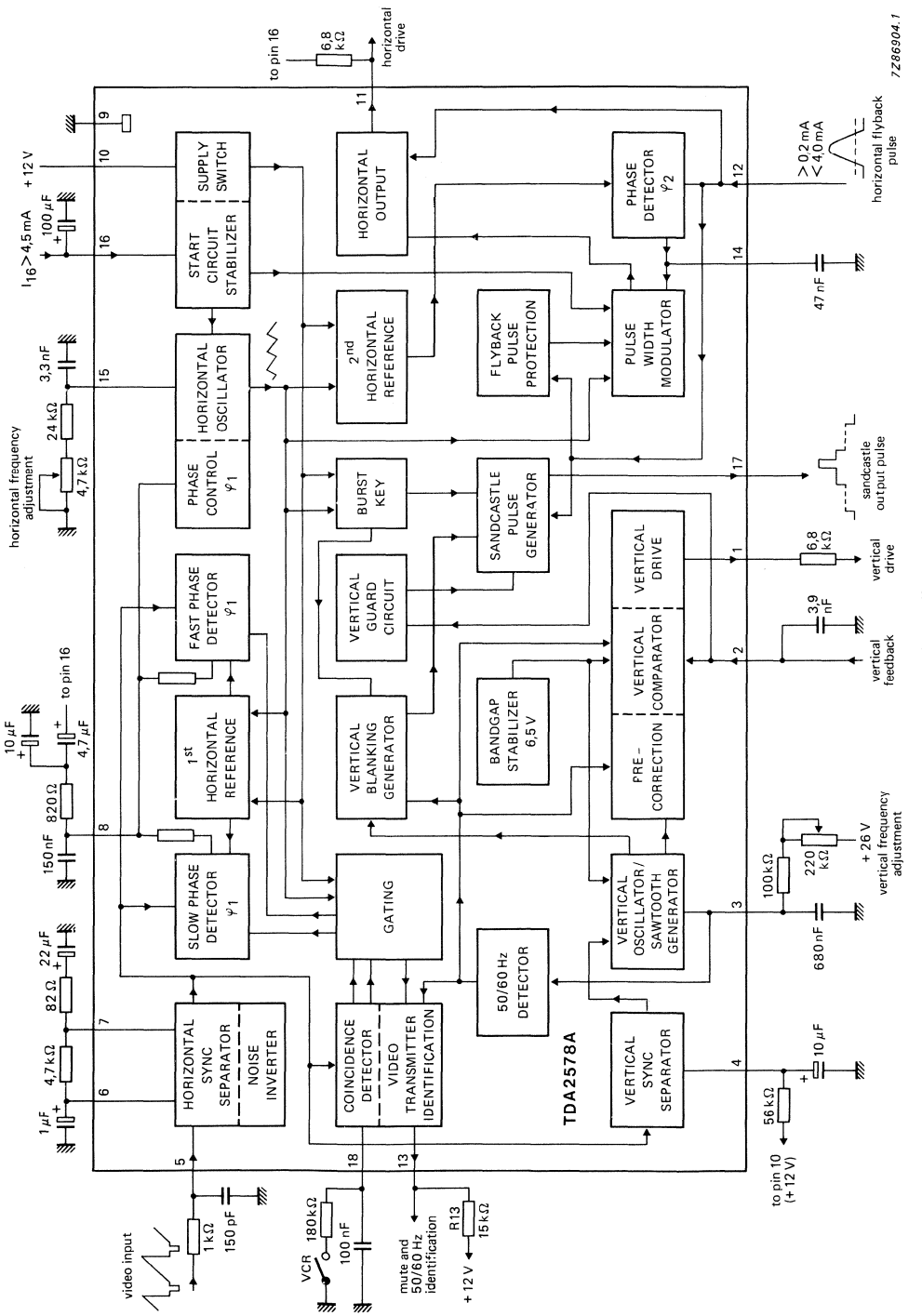


Fig. 1 Block diagram.

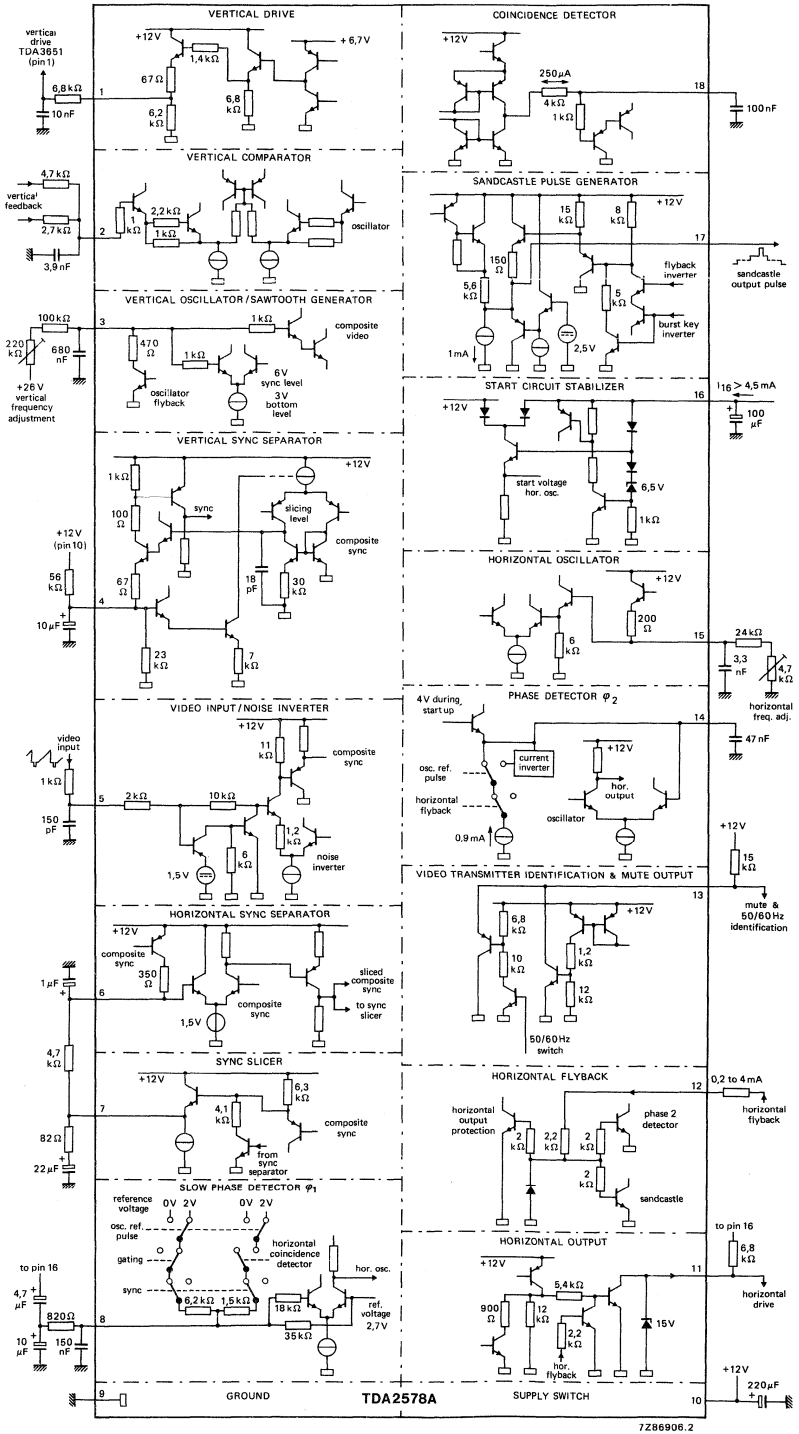


Fig. 2 TDA2578A circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Start current (pin 16)	I_{16}	max.	8	mA
Supply voltage (pin 10)	$V_P = V_{10-9}$	max.	13,2	V
Total power dissipation	P_{tot}	max.	1,1	W
Storage temperature range	T_{stg}	−55 to +	150	°C
Operating ambient temperature range	T_{amb}	−25 to +	65	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	typ.	50	K/W

CHARACTERISTICS

I_{16} = 5 mA; V_P = 12 V; T_{amb} = 25 °C; unless otherwise specified

Supply

Supply current at pin 16	I_{16}		4,5 to 8	mA
Stabilized supply voltage (pin 16)	V_{16-9}	typ.	8,7	V
			8,0 to 9,5	V
Supply current (pin 10)	I_{10}	typ.	55	mA
		<	70	mA
Supply voltage (pin 10)	$V_P = V_{10-9}$	typ.	12	V
			10 to 13,2	V

Video input (pin 5)

Top-sync level	V_{5-9}	typ.	3,1	V
			1,5 to 3,75	V
Sync pulse amplitude (peak-to-peak value) (note 1)	$V_{5-9(p-p)}$	typ.	0,6	V
			0,15 to 1	V
Slicing level		typ.	50	%
			35 to 65	%
Delay between video input and detector output	t_1	typ.	0,35	μs

Noise gate (pin 5)

Switching level	V_{5-9}	typ.	0,7	V
		<	1	V

First control loop (sync to oscillator; pin 8)

Holding range	Δf	typ.	± 800	Hz
Catching range	Δf	typ.	± 800	Hz
			±600 to ±1100	Hz
Control sensitivity video with respect to oscillator, burst key and flyback pulse				
for slow time constant		typ.	1	kHz/μs
for fast time constant		typ.	2,75	kHz/μs

Second control loop (horizontal output to flyback; pin 14)				
Control sensitivity; static (see note 2)	$\Delta t_d/\Delta t_o$	typ.	400	$\mu s/\mu s$
Control range	t_d		1 to 45	μs
Controlled edge	positive			
Phase adjustment (via 2nd control loop; pin 14)				
Control sensitivity		typ.	25	$\mu A/\mu s$
Maximum permissible control current	$\pm I_{14}$	<	60	μA
Horizontal oscillator (pin 15)				
Frequency (no sync)	f_{osc}	typ.	15 625	Hz
Frequency spread (C_{osc} = 3,3 nF; R_{osc} = 24 kΩ; no sync)	Δf_{osc}	<	4	%
Frequency deviation between starting point of output signal and stabilized condition	Δf_{osc}	typ. <	6 8	% %
Temperature coefficient	TC	typ.	$1 \cdot 10^{-4}$	K^{-1}
Horizontal output (pin 11)				
Output voltage; high level	V_{11-9}	<	13,2	V
Voltage at which protection starts	V_{11-9}		13 to 15,8	V
Output voltage; low level start condition at I_{11} = 10 mA	V_{11-9}	typ. <	0,3 0,5	V V
normal condition at I_{11} = 40 mA	V_{11-9}	typ. <	0,3 0,5	V V
Duty factor of output signal during starting (no phase shift) I_{16} = 4 mA (voltage at pin 11 low)	δ	typ.	65	%
Duty factor of output signal without flyback pulse	δ	typ.	50 45 to 55	% %
Controlled edge	positive			
Duration of output pulse (see Fig. 4)	t_d + horizontal flyback pulse			
Sandcastle output pulse (pin 17)				
Output voltage during: burst key	V_{17-9}	>	10	V
horizontal blanking	V_{17-9}	typ. 	4,6 4,2 to 5	V V
vertical blanking	V_{17-9}	typ. 	2,5 2 to 3	V V
Pulse duration burst key	t_p	typ. 	3,7 3,3 to 4,1	μs μs
horizontal blanking	flyback pulse (see note 3)			
vertical blanking at 50 Hz at 60 Hz	21 lines 17 lines			

CHARACTERISTICS (continued)

Delay between the start of the sync at the video input and the rising edge of the burst key pulse	t_2	typ.	5,2	μs
			4,8 to 5,6	μs
Delay between start of sync and trailing edge of burst key	t_2	typ.	8,8	μs
			8,1 to 9,3	μs
Coincidence detector; video transmitter identification circuit; time constant switches (pin 18); see also Fig. 3				
Detector output current	$\pm I_{18}$	typ.	300	μA
Voltage during noise (note 4)	V_{18-9}	typ.	0,3	V
Voltage level for in-sync condition	V_{18-9}	typ.	7,5	V
Switching level slow to fast	V_{18-9}	typ.	3,5	V
			3,2 to 3,8	V
Switching level mute function active; φ_1 fast to slow	V_{18-9}	typ.	1,2	V
			1,0 to 1,4	V
vertical period counter 3 periods fast	V_{18-9}	typ.	0,12	V
			0,08 to 0,16	V
Switching level slow to fast (locking) mute function inactive	V_{18-9}	typ.	1,7	V
			1,5 to 1,9	V
Switching level fast to slow (locking)	V_{18-9}	typ.	5,0	V
			4,7 to 5,3	V
Switching level for VCR (fast time constant) without mute function	V_{18-9}	typ.	8,6	V
			8,2 to 9,0	V
Video transmitter identification output (pin 13)				
Output voltage active (no sync) at I_{13} = 1 mA	V_{13-9}	<	0,5	V
		typ.	0,3	V
Sink current active (no sync)	I_{13}	$\leqslant$	5	mA
Output current inactive (sync: 50 Hz)	I_{13}	<	1	μA
50/60 Hz identification (pin 13)				
R13 = 15 kΩ to + 12 V (note 5) at f = 50 Hz (in sync condition)	V_{13-9}	typ.	V_{10-9}	V
at f = 60 Hz (in sync condition)	V_{13-9}	typ.	7,6	V
			7,2 to 8	V
Flyback input pulse (pin 12)				
Switching level	V_{12-9}	typ.	1	V
Input current	I_{12}		0,2 to 4	mA
Input pulse amplitude (peak-to-peak value)	$V_{12-9(p-p)}$	<	12	V
Input resistance	R_{12-9}	typ.	2,7	kΩ
Delay time of sync pulse (measured in φ_1) to flyback at switching level; t_{fl} = 12 μs (see also note 2 and Fig. 4)	t_o	typ.	1,3	μs

Vertical sawtooth generator (pin 3)			
Vertical frequency (no sync)	f_s	typ.	46 Hz
Frequency spread (C_{osc} = 680 nF; R_{osc} = 187 kΩ; at + 26 V)	Δf_s	<	4 %
Synchronization range (note 6)		typ.	33 %
Input current at V_{3-9} = 6 V	I_3	<	3 μA
Frequency shift for V_P = 10 to 13 V	Δf_s	<	0,2 %
Temperature coefficient	TC	typ.	$1 \cdot 10^{-4}$ K^{-1}
Comparator (pin 2)			
Input voltage; d.c. level	V_{2-9}	typ. 4,0 to 4,8	4,4 V V
a.c. level (peak-to-peak value)	$V_{2-9(p-p)}$	typ.	0,8 V
Input current at V_{2-9} = 6 V	I_2	<	2 μA
Sawtooth internal pre-correction (parabolic convex)		typ.	6 %
Vertical output stage; emitter follower (pin 1)			
Output voltage at I_1 = 10 mA	V_{1-9}	typ. 3,2 to 5	3,6 V V
Output current	I_1	<	20 mA
Vertical guard circuit			
Activating voltage levels (vertical blanking level is 2,5 V) switching level low	V_{2-9}	typ. 3,0 to 3,7	3,35 V V
switching level high	V_{2-9}	typ. 4,75 to 5,55	5,15 V V

Notes to characteristics

1. Up to 1 V peak-to-peak the slicing level is constant; at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.
2. t_d = delay between positive transient of horizontal output pulse and the rising edge of the flyback pulse.
   t_o = delay between the rising edge of the flyback pulse and the start of the current in φ_1 (pin 8).
3. The duration of the flyback pulse is measured at the input switching level, which is about 1 V (t_{fl}).
4. Depends on d.c. level at pin 5; value given applicable for $V_{5-9} \approx 5$ V.
5. For 60 Hz a p-n-p emitter clamp is activated.
6. When f_o = 46 Hz the 50/60 Hz detector switches over to 60 Hz; video input signal at pin 5 ≈ 55 Hz.

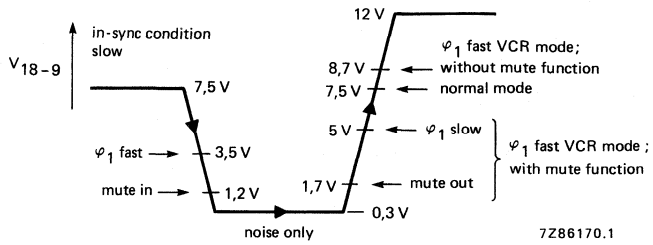


Fig. 3 Voltage levels at pin 18 (V_{18-9}).

APPLICATION INFORMATION

The TDA2578A generates the signal for driving the horizontal deflection output circuit. It also contains a synchronized vertical sawtooth generator for direct drive of the vertical deflection output stage.

The horizontal oscillator and output stage can start operating on a very low supply current ($I_{16} \geqslant 4{,}5$ mA), which can be taken directly from the mains rectifier. Therefore, it is possible to derive the main supply (pin 10) from the horizontal deflection output stage. The duty factor of the horizontal output signal is about 65% during the starting-up procedure. After starting-up, the second phase detector (φ_2) is activated to control the timing of the positive-going edge of the horizontal output signal.

A bandgap reference voltage (6,5 V) is provided for supply and reference of the vertical oscillator and comparator stage.

The slicing level of the horizontal sync separator is independent of the amplitude of the sync pulse at the input. The resistor between pins 6 and 7 determines its value. A 4,7 kΩ resistor gives a slicing level at the middle of the sync pulse. The nominal top sync level at the input is 3,1 V. The amplitude selective noise inverter is activated at a level of 0,7 V.

Good stability is obtained by means of the two control loops. In the first loop, the phase of the horizontal sync signal is compared with a waveform of which the rising edge refers to the top of the horizontal oscillator signal. In the second loop, the phase of the flyback pulse is compared with another reference waveform, the timing of which is such that the top of the flyback pulse is situated symmetrically on the horizontal blanking internal of the video signal. Therefore the first loop can be designed for a good noise immunity, whereas the second loop can be as fast as desired for compensation of switch-off delays in the horizontal output stage.

The first phase detector is gated with a pulse derived from the horizontal oscillator signal. This gating (slow time constant) is switched off during catching. Also, the output current of the phase detector is increased fivefold, during the catching time and VCR conditions (fast time constant). The first phase detector is inhibited during the retrace time of the vertical oscillator.

The in-sync, out-of-sync or no video condition is detected by the video transmitter identification/coincidence detector circuit (pin 18). The voltage on pin 18 defines the time constant and gating of the first phase detector. The relationship between this voltage and the various switching levels is shown in Fig. 3. The complete survey of the switching actions is given in Table 1.

Table 1 Switching levels at pin 18.

voltage at pin 18	first phase detector φ_1				mute output at pin 13		receiving conditions
	time constant		gating				
	slow	fast	on	off	on	off	
7,5 V	X		X			X	video signal detected
7,5 to 3,5 V	X		X			X	video signal detected
3,5 to 1,2 V		X		X		X	video signal detected
1,2 to 0,1 V	X		X		X		noise only
0,1 to 1,7 V	X	*	X	*	X		new video signal detected
1,7 to 5,0 V		X		X		X	horizontal oscillator locked VCR playback with mute function
5,0 to 7,5 V	X		X			X	horizontal oscillator locked
8,7 V		X		X		X	VCR playback without mute function

Where: * = 3 vertical periods.

APPLICATION INFORMATION (continued)

The stability of displayed video information (e.g. channel number), during noise only conditions, is improved by the first phase detector time constant being set to slow.

The average voltage level of the video input on pin 5 during noise only conditions should not exceed 5,5 V otherwise the time constant switch may be set to fast due to the average voltage level on pin 18 dropping below 0,1 V. When the voltage on pin 18 drops below 100 mV a counter is activated which sets the time constant switch to fast, and not gated for 3 vertical periods. This condition occurs when a new video signal is present at pin 5. When the horizontal oscillator is locked the voltage on pin 18 increases. Nominally a level of 5 V is reached within 15 ms (1 vertical period). The mute switching level of 1,2 V is reached within 5 ms (C_{18} = 47 nF). If the video transmitter identification circuit is required to operate under VCR playback conditions the first phase detector can be set to fast by connecting a resistor of 180 kΩ between pin 18 and ground (see Fig. 7).

The supply for the horizontal oscillator (pin 15) and horizontal output stage (pin 11) is derived from the voltage at pin 16 during the start condition. The horizontal output signal starts at a nominal supply current into pin 16 of 4,2 mA, which will result in a supply voltage of about 5,5 V (for guaranteed operation of all devices $I_{16} > 4{,}5$ mA). It is possible that the main supply voltage at pin 10 is 0 V during starting, so the main supply of the IC can be taken from the horizontal deflection output stage. The start of the other IC functions depends on the value of the main supply voltage at pin 10. At 5,5 V all IC functions start operating except the second phase detector (oscillator to flyback pulse). The output voltage of the second phase detector at pin 14 is clamped by means of an internally loaded n-p-n emitter follower. This ensures that the duty factor of the horizontal output signal (pin 11) remains at about 65%. The second phase detector will close if the supply voltage at pin 10 reaches 8,8 V. At this value the supply current for the horizontal oscillator and output stage is delivered by pin 10, which also causes the voltage at pin 16 to change to a stabilized 8,7 V. This change switches off the n-p-n emitter follower at pin 14 and activates the second phase detector. The supply voltage for the horizontal oscillator will, however, still be referred to the stabilized voltage at pin 16, and the duty factor of the output signal at pin 12 is at the value required by the delay at the horizontal deflection stage. Thus switch-off delays in the horizontal output stage are compensated. When no horizontal flyback signal is detected the duty factor of the horizontal output signal is 50%.

Horizontal picture shift is possible by externally charging or discharging the 47 nF capacitor connected to pin 14.

The IC also contains a synchronized vertical oscillator/sawtooth generator. The oscillator signal is connected to the internal comparator (the other side of which is connected to pin 2), via an inverter and amplitude divider stage. The output of the comparator drives an emitter-follower output stage at pin 1. For a linear sawtooth in the oscillator, the load resistor at pin 3 should be connected to a voltage source of 26 V or higher. The sawtooth amplitude is not influenced by the main supply at pin 10. The feedback signal is applied to pin 2 and compared to the sawtooth signal at pin 3. For an economical feedback circuit with less picture bounce the sawtooth signal is internally pre-corrected by 6% (convex) referred to pin 2. The linearity of the vertical deflection current depends upon the oscillator signal at pin 3 and the feedback signal at pin 2.

Synchronization of the vertical oscillator is inhibited when the mute output is present at pin 13.

To minimize the influence of the horizontal part on the vertical part a 6,7 V bandgap reference source is provided for supply and reference of the vertical oscillator and comparator.

The sandcastle pulse, generated at pin 17, has three different voltage levels. The highest level (11 V) can be used for burst gating and black level clamping. The second level (4,6 V) is obtained from the horizontal flyback pulse at pin 12 and used for horizontal blanking. The third level (2,5 V) is used for vertical blanking and is derived by counting the horizontal frequency pulses. For 50 Hz the blanking pulse duration is 21 lines and for 60 Hz it is 17 lines. The blanking pulse duration and sawtooth amplitude is automatically adjusted via the 50/60 Hz detector.

The IC also incorporates a vertical guard circuit, which monitors the vertical feedback signal at pin 2. If this level is below 3,35 V or higher than 5,15 V, the guard circuit will insert a continuous level of 2,5 V into the sandcastle output signal. This will result in complete blanking of the screen if the sandcastle pulse is used for blanking in the TV set.

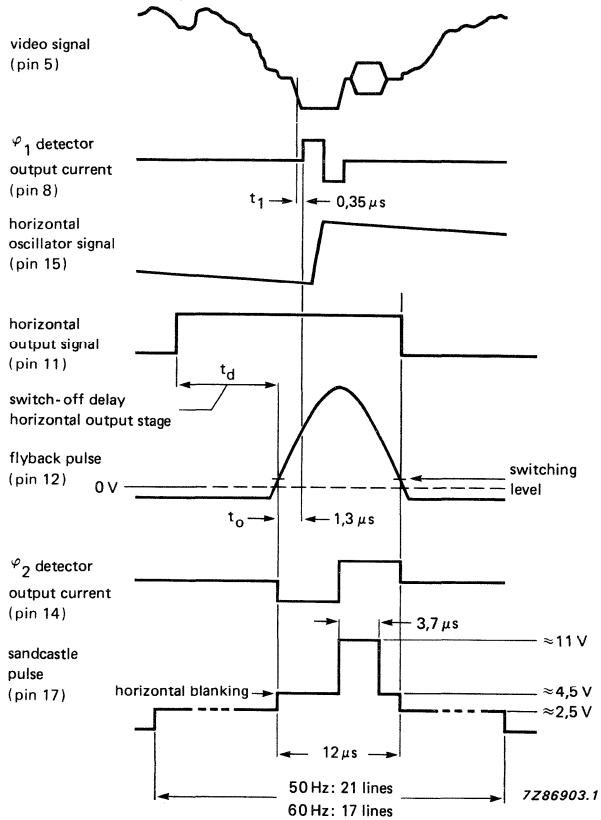
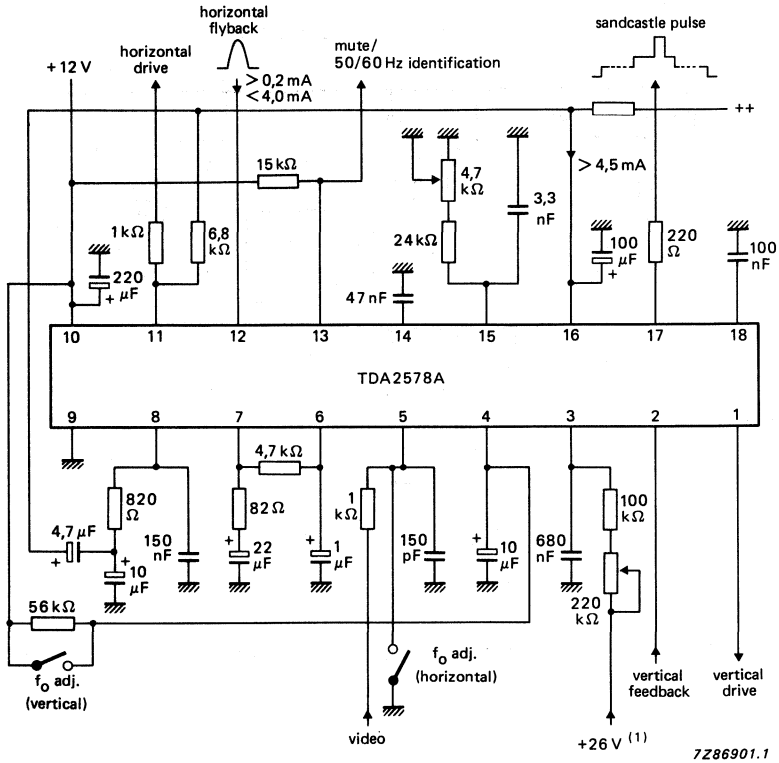


Fig. 4 Timing diagram of the TDA2578A.

APPLICATION INFORMATION (continued)



(1) ⩾ 26 V for linear scan.

Fig. 5 Typical application circuit diagram; for application of the TDA2578A with the TDA3651 see Fig. 8.

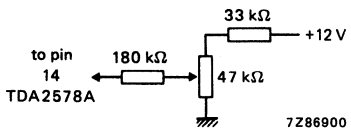


Fig. 6 Circuit configuration at pin 14 for phase adjustment.

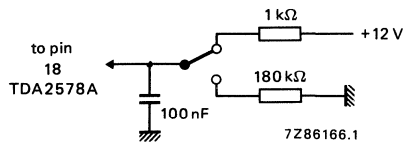


Fig. 7 Circuit configuration at pin 18 for VCR mode.
1 kΩ resistor between pin 18 and + 12 V: without mute function.
180 kΩ between pin 18 and ground: with mute function.

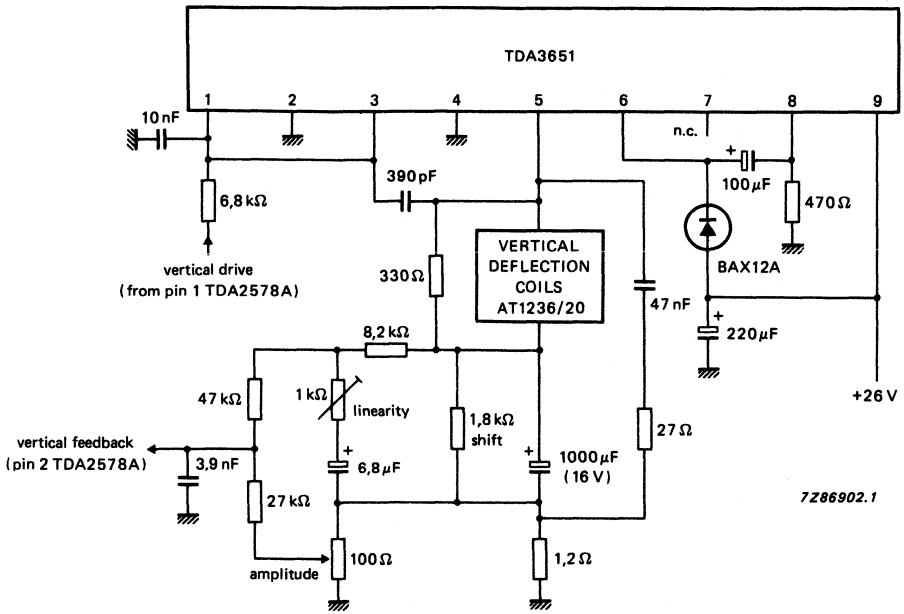


Fig. 8 Typical application circuit diagram of the TDA3651 (vertical output), when used in combination with the TDA2578A, (90° application).

HORIZONTAL/VERTICAL SYNCHRONIZATION CIRCUIT

GENERAL DESCRIPTION

The TDA2579A generates and synchronizes horizontal and vertical signals. The device has a 3 level sandcastle output; a transmitter identification signal and also 50/60 Hz identification.

Features

- Horizontal phase detector, (sync to oscillator), sync separator and noise inverter
- Triple current source in the phase detector with automatic selection
- Second phase detector for storage compensation of the horizontal output
- Stabilized direct starting of the horizontal oscillator and output stage from mains supply
- Horizontal output pulse with constant duty cycle value of 29 μs
- Internal vertical sync separator, and two integration selection times
- Divider system with three different reset enable windows
- Synchronization is set to 628 divider ratio when no vertical sync pulses and no video transmitter is identified
- Vertical comparator with a low DC feedback signal
- 50/60 Hz identification output combined with mute function
- Automatic amplitude adjustment for 50 and 60 Hz and blanking pulse duration
- Automatic adaption of the burst-key pulsewidth

QUICK REFERENCE DATA

parameter	condition	symbol	min.	typ.	max.	unit
Supply						
Minimum required current for starting horizontal oscillator and output stage		I_{16}	6.2	–	–	mA
Main supply voltage		V_{10}	–	12	–	V
Supply current		I_{10}	–	70	–	mA
Input signals						
Sync pulse input amplitude		$V_{5(p-p)}$	0.05	–	1.0	V
Horizontal flyback pulse input current		I_{12}	–	1	–	mA
Vertical comparator input signal						
Voltage AC		V_2	–	0.8	–	V
Voltage DC		V_2	–	1	–	V
Output signals						
Horizontal output (open collector) I_{11} = 25 mA		V_{11}	–	–	0.5	V
Vertical output stage driver (emitter follower) I_1 = 1.5 mA		V_1	5	–	–	V
Sandcastle output levels						
V_{17} burst-key		V_{17}	9.8	–	–	V
horizontal blanking		V_{17}	–	4.5	–	V
vertical blanking		V_{17}	–	2.5	–	V
Video transmitter identification output stage (open collector loaded with external resistor to positive supply). No sync. pulse present		V_{13}	–	–	0.5	V
		I_{13}	–	–	5	mA
Sync pulse present						
divider ratio > 576		V_{13}	–	V_{10}	–	V
divider ratio < 576		V_{13}	–	7.65	–	V

PACKAGE OUTLINE

18-lead dual in line; plastic (SOT102).

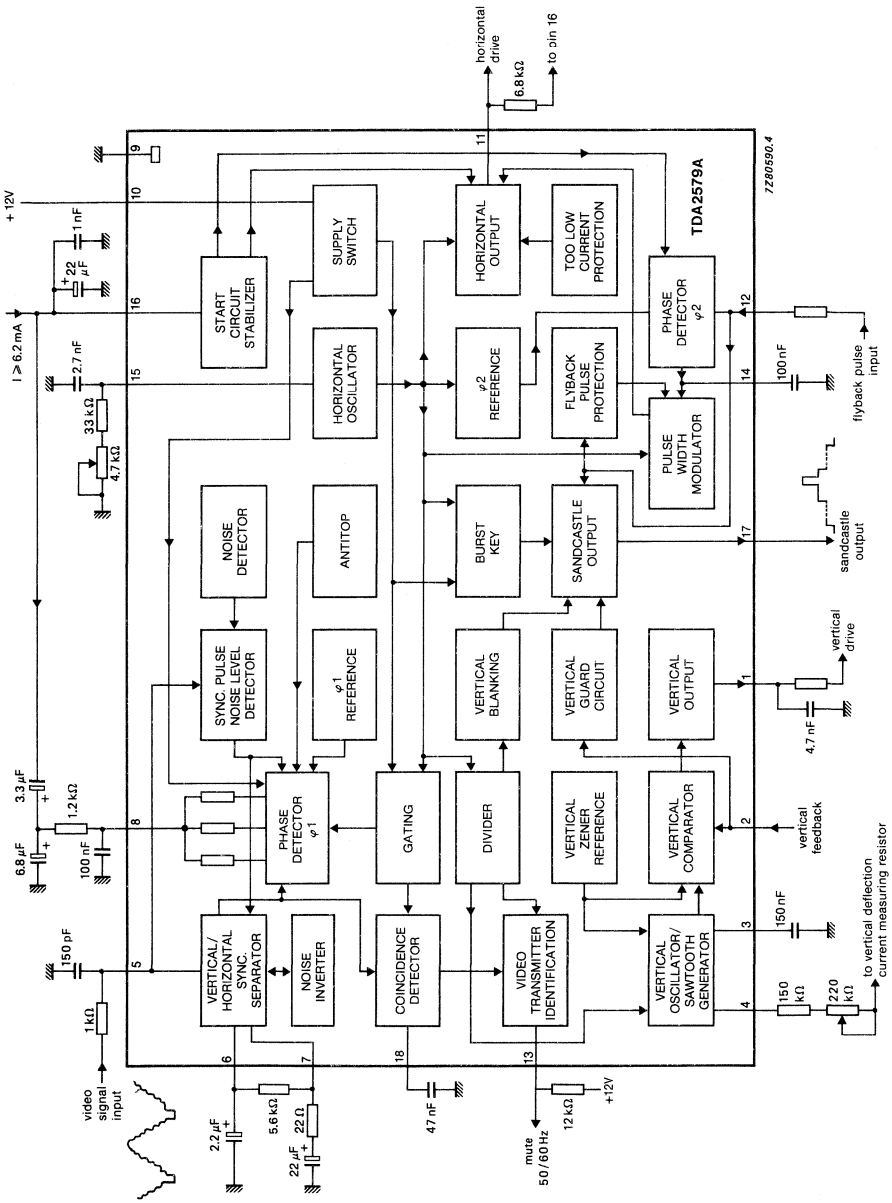


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

Vertical part (pins 1,2,3,4)

The IC embodies a synchronized divider system for generating the vertical sawtooth at pin 3. The divider system has an internal frequency doubling circuit, so the horizontal oscillator is working at its normal line frequency and one line period equals 2 clock pulses. Due to the divider system no vertical frequency adjustment is needed. The divider has a discriminator window for automatically switching over from the 60 Hz to 50 Hz system. The divider system operates with 3 different divider reset windows for maximum interference/disturbance protection.

The windows are activated via an up/down counter. The counter increases its counter value by 1 for each time the separated vertical sync pulse is within the searched window. The count is decreased by 1 when the vertical sync pulse is not present.

Large (search) window: divider ratio between 488 and 722

This mode is valid for the following conditions:

1. Divider is looking for a new transmitter.
2. Divider ratio found, not within the narrow window limits.
3. Non standard TV-signal condition detected while a double or enlarged vertical sync. pulse is still found after the internally generated anti-top-flutter pulse has ended. This means a vertical sync pulse width larger than 8 clock pulses (50 Hz), that is, 10 clock pulses (60 Hz). In general this mode is activated for video tape recorders operating in the feature/trick mode.
4. Up/down counter value of the divider system operating in the narrow window mode decreases below count 1.
5. Externally setting. This can be reached by loading pin 18 with a resistor of 220 kΩ to earth or connecting a 3.6 V diode stabistor between pin 18 and ground.

Narrow window: divider ratio between 522-528 (60 Hz) or 622-628 (50 Hz).

The divider system switches over to this mode when the up/down counter has reached its maximum value of 12 approved vertical sync pulses. When the divider operates in this mode and a vertical sync pulse is missing within the window the divider is reset at the end of the window and the counter value is decreased by 1. At a counter value below count 1 the divider system switches over to the large window mode.

Standard TV-norm

When the up/down counter has reached its maximum value of 12 in the narrow window mode, the information applied to the up/down counter is changed such that the standard divider ratio value is tested. When the counter has reached a value of 14 the divider system is changed over to the standard divider ratio mode. In this mode the divider is always reset at the standard value even if the vertical sync pulse is missing. A missed vertical sync pulse decreases the counter value by 1. When the counter reaches the value of 10 the divider system is switched over to the large window mode. The standard TV-norm condition gives maximum protection for video recorders playing tapes with anti-copy guards.

No-TV-transmitter found: (pin 18 $<$ 1.2 V)

In this condition, only noise is present, the divider is rest to count 628. In this way a stable picture display at normal height is achieved.

Video tape recorders in feature mode

It should be noted that some VTRs operating in the feature modes, such as picture search, generate such distorted pictures that the no-TV-transmitter detection circuit can be activated as pin V_{18} drops below 1.2 V. This would imply a rolling picture (see Phase detector, sub paragraph d). In general VTR-machines use a re-inserted vertical sync pulse in the feature mode. Therefore the divider system has been made such that the automatic reset of the divider at count 628 when V_{18} is below 1.2 V is inhibited when a vertical sync pulse is detected.

The divider system also generates the anti-top-flutter pulse which inhibits the Phase 1 detector during the vertical sync. pulse. The width of this pulse depends on the divider mode. For the divider mode a the start is generated at the reset of the divider. In mode b and c the anti-top-flutter pulse starts at the beginning of the first equalizing pulse. The anti-top-flutter pulse ends at count 8 for 50 Hz and count 10 for 60 Hz. The vertical blanking pulse is also generated via the divider system. The start is at the reset of the divider while the blanking pulse ends at count 34 (17 lines) for 60 Hz, and at count 42 (21 lines) for 50 Hz systems. The vertical blanking pulse generated at the sandcastle output pin 17 is made by adding the anti-top-flutter pulse and the blanking pulse. In this way the vertical blanking pulse starts at the beginning of the first equalizing pulse when the divider operates in the b or c mode. For generating a vertical linear sawtooth voltage a capacitor should be connected to pin 3. The recommended value is 150 nF to 330 nF (see Fig. 1).

The capacitor is charged via an internal current source starting at the reset of the divider system. The voltage on the capacitor is monitored by a comparator which is activated also at reset. When the capacitor has reached a voltage value of 5.85 V for the 50 Hz system or 5.0 V for the 60 Hz system the voltage is kept constant until the charging period ends. The charge period width is 26 clock pulses. At clock pulse 26 the comparator is switched off and the capacitor is discharged by an npn transistor current source, the value of which can be set by an external resistor between pin 4 and ground (pin 9). Pin 4 is connected to a pnp transistor current source which determines the current of the npn current source at pin 3. The pnp current source on pin 4 is connected to an internal zener diode reference voltage which has a typical voltage of ≈ 7.7 volts. The recommended operating current range is 10 to 75 μA. The resistance at pin R_4 should be 100 to 770 kΩ. By using a double current mirror concept the vertical sawtooth pre-correction can be set on the desired value by means of external components between pin 4 and pin 3, or by connecting the pin 4 resistor to the vertical current measuring resistor of the vertical output stage. The vertical amplitude is set by the current of pin 4. The vertical feedback voltage of the output stage has to be applied to pin 2. For the normal amplitude adjustment the values are DC = 1 V and AC = 0.8 V. Due to the automatic system adaption both values are valid for 50 Hz and 60 Hz.

The low DC voltage value improves the picture bounce behaviour as less parabola compensation is necessary. Even a fully DC coupled feedback circuit is possible.

Vertical guard

The IC also contains a vertical guard circuit. This circuit monitors the vertical feedback signal on pin 2. When the level on pin 2 is below 0.35 V or higher than 1.85 V the guard circuit inserts a continuous level of 2.5 V in the sandcastle output signal of pin 17. This results in the blanking of the picture displayed, thus preventing a burnt-in horizontal line. The guard levels specified refer to the zener diode reference voltage source level.

Driver output

The driver output is at pin 1, it can deliver a drive current of 1.5 mA at 5 V output. The internal impedance is approximately 150 Ω. The output pin is also connected to an internal current source with a sink current of 0.35 mA.

Sync separator, phase detector and TV-station identification (pins 5,6,7,8 and 18)

The video input signal is connected to pin 5. The sync separator is designed such that the slicing level is independent of the amplitude of the sync pulse. The black level is measured and stored in the capacitor at pin 7. The slicing level value is stored in the capacitor at pin 6. The slicing level value can be chosen by the value of the external resistor between pins 6 and 7. The value is given by the formula:

$$P = \frac{R_S}{5.3 + R_S} \times 100 \quad (R_S \text{ value in } k\Omega)$$

Where R_S is the resistor between pins 6 and 7 and top sync level equals 100%. The recommended resistor value is 5.6 kΩ.

Black level detector

A gating signal is used for the black level detector. This signal is composed of an internal horizontal reference pulse with a duty factor of 50% and the flyback pulse at pin 12. In this way the TV-transmitter identification operates also for all DC conditions at input pin 5 (no video modulation, plain carrier only).
During the frame interval the slicing level detector is inhibited by a signal which starts with the anti-top flutter pulse and ends with the reset vertical divider circuit. In this way shift of the slicing level due to the vertical sync signal is reduced and separation of the vertical sync pulse is improved.

DEVELOPMENT DATA

Noise inverter

An internal noise inverter is activated when the video level at pin 5 decreases below 0.7 V. The IC also embodies a built-in sync pulse noise level detection circuit. This circuit is directly connected to pin 5 and measures the noise level at the middle of the horizontal sync pulse. When a signal-to-noise level of 19 dB is detected a counter circuit is activated. A video input signal is processed as "acceptable noise free" when 12 out of 16 sync pulses have a noise level below 19 dB for two successive frame periods. The sync pulses are processed during a 16 line width gating period generated by the divider system. The measuring circuit has a built-in noise level hysteresis of approximately 3 dB.
When the "acceptable noise free" condition is found the phase detector of pin 8 is switched to not gated and normal time constant. When a higher sync pulse noise level is found the phase detector is switched over to slow time constant and gated sync pulse phase detection. At the same time the integration time of the vertical sync pulse separator is adapted.

$$S/N = 20 \text{ Log} \frac{\text{Video voltage (black to white}_{p\text{-}p})}{\text{Noise}_{rms}}$$

Phase detector

The phase detector circuit is connected to pin 8. This circuit consists of 3 separate phase detectors which are activated depending on the voltage of pin 18 and the state of the sync pulse noise detection circuit. For normal and fast time constants all three phase detectors are activated during the vertical blanking period, this with the exception of the anti-top-flutter pulse period, and the separated vertical sync-pulse time. As a result, phase jumps in the video signal related to the video head, take over of video recorders are quickly restored within the vertical blanking period. At the end of the blanking period the phase detector time constant is increased by 1.5 times. In this way there is no requirement for external VTR time constant switching, and so all station numbers are suitable for signals from VTR, video games or home computers.
For quick locking of a new TV station starting from a noise only signal condition (normal time constant) a special circuit is incorporated. A new TV station which is not locked to the horizontal oscillator will result in a voltage decrease below 0.1 V at pin 18. This will activate a frame period counter which switches the phase detector to fast for 3 frame periods during the vertical scan period.

The horizontal oscillator will now lock to the new TV-station and as a result, the voltage on pin 18 will increase to approximately 6.5 V. When pin 18 reaches a level of 1.8 V the mute output transistor of pin 13 is switched OFF and the divider is set to the large window. In general the mute signal is switched OFF within 5 ms (pin C_{18} = 47 nF) after reception of a new TV-signal. When the voltage on pin 18 reaches a level of 5 V, usually within 15 ms, the frame counter is switched OFF and the time constant is switched from fast to normal during the vertical scan period.

If the new TV station is weak, the sync-noise detector is activated. This will result in a change over of pin 18 voltage from 6.5 V to ≈ 10 V. When pin 18 exceeds the level of 7.8 V the phase detector is switched to slow time constant and gated sync pulse condition. The current is also reduced during the vertical blanking period by 1 mA. When desired, most conditions of the phase detector can also be set by external means in the following way:

a. Fast time constant TV transmitter identification circuit not active, connect pin 18 to earth (pin 9).
b. Fast time constant TV transmitter identification circuit active, connect a resistor of 220 kΩ between pin 18 and ground.
   This condition can also be set by using a 3.6 V stabistor diode instead of a resistor.
c. Slow time constant, (with exception of frame blanking period), connect pin 18 via a resistor of 10 kΩ to + 12 V, pin 10. In this condition the transmitter identification circuit is not active.
d. No switching to slow time constant desired (transmitter identification circuit active), connect a 6.8 V zener diode between pin 18 and ground.

Fig. 2 illustrates the operation of the 3 phase detector circuits.

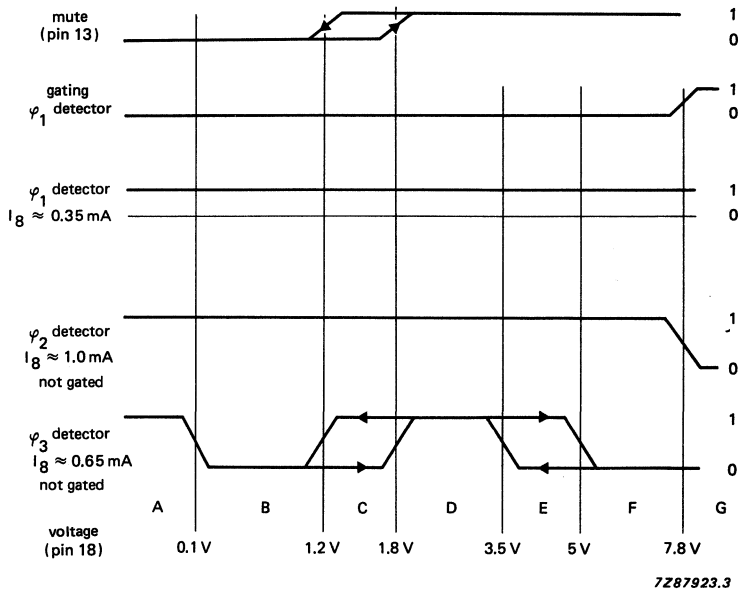


Fig. 2 Timing diagram, phase detectors.

Supply (pins 9, 10 and 16)

The IC has been designed such that the horizontal oscillator and output stage can start operating by application of a very low supply current into pin 16.

The horizontal oscillator starts at a supply current of approximately 4 mA. The horizontal output stage is forced into the non-conducting stage until the supply current has a typical value of 5 mA. The circuit has been designed so that after starting the horizontal output function a current drop of $\approx$ 1 mA is allowed. The starting circuit has the ability to derive the main supply (pin 10) from the horizontal output stage. The horizontal output signal can also be used as the oscillator signal for synchronized switched mode power supplies. The maximum allowed starting current is 9.7 mA (T_{amb} = 25 °C). The main supply should be connected to pin 10, and pin 9 should be used as ground. When the voltage on pin 10 increases from zero to its final value (typically 12 V) a part of the supply current of the starting circuit is taken from pin 10 via internal diodes, and the voltage on pin 16 will stabilize to a typical value of 9.4 V.

In a stabilized condition (pin $V_{10} > 10$ V) the minimum required supply current to pin 16 is $\approx$ 2.5 mA. All other IC functions are switched on via the main supply voltage on pin 10. When the voltage on pin 10 reaches a value of $\approx$ 7 V the horizontal phase detector circuit is activated and the vertical ramp on pin 3 is started. The second phase detector circuit and burst pulse circuit are started when the voltage on pin 10 reaches the stabilized voltage value of pin 16 which is typically 9.4 V.

To close the second phase detector loop, a flyback pulse must be applied to pin 12. When no flyback pulse is detected the duty factor of the horizontal output stage is 50%.

For remote switch-off pin 16 can be connected to ground (via a npn transistor with a series resistor of $\approx$ 500 Ω) which switches off the horizontal output.

Horizontal oscillator, horizontal output transistor, and second phase detector (pins 11, 12, 14 and 15)

The horizontal oscillator is connected to pin 15. The frequency is set by an external RC combination between pin 15 and ground, pin 9. The open collector horizontal output stage is connected to pin 11. An internal zener diode configuration limits the open voltage of pin 11 to $\approx$ 14.5 V.
The horizontal output transistor at pin 11 is blocked until the current into pin 16 reaches a value of $\approx$ 5 mA.
A higher current results in a horizontal output signal at pin 11, which starts with a duty factor of $\approx$ 40% HIGH.

The duty factor is set by an internal current-source-loaded npn emitter follower stage connected to pin 14 during starting. When pin 16 changes over to voltage stabilization the npn emitter follower and current source load at pin 14 are switched OFF and the second phase detector circuit is activated, provided a horizontal flyback pulse is present at pin 12. When no flyback pulse is detected at pin 12 the duty factor of the horizontal output stage is set to 50%.

The phase detector circuit at pin 14 compensates for storage time in the horizontal deflection output stage. The horizontal output pulse duration is 29 μs HIGH for storage times between 1 μs and 17 μs (29 μs flyback pulse of 12 μs). A higher storage time increases the HIGH time. Horizontal picture shift is possible by forcing an external charge or discharge current into the capacitor at pin 14.

Mute output and 50/60 Hz identification (pin 13)

The collector of an npn transistor is connected to pin 13. When the voltage on pin 18 drops below 1.2 V (no TV-transmitter) the npn transistor is switched ON.
When the voltage on pin 18 increases to a level of $\approx$ 1.8 V (new TV-transmitter found) the npn transistor is switched OFF.

Pin 13 has also the possibility for 50/60 Hz identification. This function is available when pin 13 is connected to pin 10 (+ 12 V) via an external pull-up resistor of 10 to 20 kΩ. When no TV-transmitter is identified the voltage on pin 13 will be LOW ($<$ 0.5 V). When a TV-transmitter with a divider ratio $>$ 576 (50 Hz) is detected the output voltage of pin 13 is HIGH (+ 12 V).
When a TV-transmitter with a divider ratio $<$ 576 (60 Hz) is found an internal pnp transistor with its emitter connected to pin 13 will force this pin output voltage down to $\approx$ 7.6 V.

Sandcastle output (pin 17)

The sandcastle output pulse generated at pin 17, has three different voltage levels. The highest level, (10.4 V), can be used for burst gating and black level clamping. The second level (4.5 V) is obtained from the horizontal flyback pulse at pin 12, and is used for horizontal blanking. The third level (2.5 V) is used for vertical blanking and is derived via the vertical divider system. For 50 Hz the blanking pulse duration is 42 clock pulses and for 60 Hz it is 34 clock pulses started from the vertical divider reset. For TV-signals which have a divider ratio between 622 and 628 or between 522 and 528 the pulse is started at the first equalizing pulse. With the 50/60 Hz information the burst-key pulse width is switched to improve the behaviour in multi-norm concepts.

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Start current	I_{16}	–	9.7	mA
Supply voltage	V_{10}	–	13.2	V
Total power dissipation	P_{tot}	–	1.2	W
Storage temperature range	T_{stg}	−55	+ 150	°C
Operating ambient temperature range	T_{amb}	−25	+ 70	°C

Thermal resistance

From junction to ambient in free air $R_{th\ j\text{-}a}$ 50 K/W

DEVELOPMENT DATA

CHARACTERISTICS

T_{amb} = 25 °C; I_{16} = 6.2 mA; V_{10} = 12 V; unless otherwise specified
Voltage measurements are taken with respect to pin 9 (ground)

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply current (pin 16)						
V_{10} = 0 V		I_{16}	6.2	–	9.7	mA
V_{10} = 10 V		I_{16}	2.5	–	9.7	mA
Stabilized voltage (pin 16)		V_{16}	8.9	9.4	9.8	V
Current consumption (pin 10)		I_{10}	–	70	85	mA
Supply voltage range (pin 10)		V_P	10	12	13.2	V
Video input (pin 5)						
Top sync level		V_5	1.5	3.1	3.75	V
Sync pulse amplitude (peak-to-peak value)	note 1	$V5_{(p-p)}$	0.05	0.6	1.0	V
Slicing level	note 2		35	50	65	%
Delay between video input and detector output (see also Fig. 3)			0.2	0.3	0.55	μs
Sync pulse noise level detector circuit active	note 3	S/N	–	19	–	dB
Sync pulse						
Noise level detector circuit hysteresis			–	3	–	dB
Noise gate (pin 5)						
Switching level		V_5	–	+ 0.7	+ 1	V
First control loop (pin 8) (horizontal oscillator to sync)						
Holding range		Δf	–	± 800		Hz
Catching range		Δf	± 700	± 800	± 1100	
Control sensitivity video with respect to burst-key and flyback-pulse						
Slow time constant			–	2.1	–	kHz/μs
Normal time constant			–	5.2	–	kHz/μs
Fast time constant			–	3.2	–	kHz/μs
Phase modulation due to hum on the supply line (pin 10)	note 4		–	0.2	–	μs/Vtt
Phase modulation due to hum on input current (pin 16)	note 4		–	0.08	–	μs/Vtt

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Second control loop (pin 14) (horizontal flyback to horizontal oscillator)						
Control sensitivity	t_d = 10 µs	$\Delta t_d/\Delta t_o$	200	300	600	µs
Control range		t_d	1	–	>45	µs
Control range for constant duty factor horizontal output		t_d		29 (–t flyback pulse)		µs
Controlled edge of horizontal output signal (pin 11)				positive		
Phase adjustment (pin 14) (via second control loop)						
Control sensitivity	t_d = 10 µs		–	25	–	µA/µs
Maximum allowed control current		I_{14}	–	–	± 60	µA
Horizontal oscillator (pin 15)	C = 2.7 nF; R_{osc} = 34.8 kΩ					
Frequency (no sync)		f	–	15625	–	Hz
Spread (fixed external component, no sync)		Δf	–	–	± 4	%
Frequency deviation between starting point output signal and stabilized condition		Δf	–	+ 6	+ 8	%
Temperature coefficient		T_C	–	-1.10^{-4}	–	/K
Horizontal output (pin 11) (Open collector)						
Output voltage high		V_{11}	–	–	13.2	V
Start voltage protection (internal zener diode)		V_{11}	13	–	15.8	V
Low input current (pin 16) protection output enabled		I_{16}	–	5.5	6.2	mA
Output voltage low start condition	I_{11} = 10 mA	V_{11}	–	0.1	0.5	V
Duty factor output current during starting	I_{16} = 6.2 mA		50	60	70	%
Output voltage low normal condition	I_{11} = 25 mA	V_{11}	–	0.3	0.5	V
Duty factor output current without flyback pulse (pin 12)			45	50	55	%
Duration of the output pulse HIGH	T_d = 8 µs		27	29	31	µs
Controlled edge				positive		
Temperature coefficient horizontal output pulse			–	-5.10^{-2}	–	µs/°C

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Sandcastle output signal (pin 17)	I_L = 1 mA					
Output voltage during:						
burst-key		V_{17}	9.8	10.4	–	V
horizontal blanking		V_{17}	4.1	4.5	4.9	V
vertical blanking		V_{17}	2.1	2.5	2.9	V
Zero level output voltage	I_{sink} = 0.5 mA	V_{17}	–	–	0.7	V
Pulse width:						
burst-key (50 Hz)		t_p	3.95	4.25	4.7	µs
burst-key (60 Hz)		t_p	3.45	3.75	4.1	µs
Horizontal blanking		V_{12}	–	1.0	–	V
Vertical blanking	note 5					
Phase position burstkey time between middle sync pulse at pin 5 and start of burst pulse at pin 17			2.3	2.7	3.1	µs
Time between start sync pulse and end of burst pulse at pin 17						
(50 Hz)			–	9.3	9.7	µs
(60 Hz)			–	8.8	9.2	µs
Coincidence detector, video transmitter identification circuit and time constant switching levels (see also Fig. 1)						
Detector output current		I_{18}	–	0.25	–	mA
Voltage level for in sync condition (φ_1 normal)		V_{18}	5.8	6.5	7.0	V
Voltage for noisy sync pulse (φ_1 slow and gated)		V_{18}	9	10	–	V
Voltage level for noise only	note 6	V_{18}	–	0.3	–	V
Switching level normal to fast		V_{18}	<3.2	3.5	3.8	V
Switching level mute output active and fast to normal		V_{18}	<1.0	1.2	1.4	V
Switching level frame period counter (3 periods fast)		V_{18}	<0.08	0.12	0.16	V
Switching level: normal to fast (locking) mute output inactive		V_{18}	>1.5	1.75	1.9	V
Switching level fast to normal (locking)		V_{18}	>4.7	5.0	5.3	V
Switching level normal to slow (gated sync pulse)		V_{18}	7.4	7.8	8.2	V

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Video transmitter identification output (pin 13)						
Output voltage active (no sync)	I_{13} = 1 mA	V_{13}	–	0.15	0.32	V
Sink current active (no sync)	$V_{13} < 1$ V	I_{13}	–	–	5	mA
Output current inactive (sync 50 Hz)		I_{13}	–	–	1	μA
50/60 Hz identification (pin 13) (R_{13} positive supply 12 kΩ)						
Emitter follower, pnp:						
60 Hz: $\frac{2 \times f_H}{f_V} < 576$ voltage		V_{13}	7.2	7.65	8.1	V
50 Hz: $\frac{2 \times f_H}{f_V} > 576$ voltage		V_{13}	–	V_{10}	–	V
Flyback input pulse (pin 12)						
Switching level		V_{12}	–	+1	–	V
Input current		I_{12}	+0.2	–	+3	mA
Input pulse		V_{12}	–	–	12	V_P
Input resistance			–	3.5	–	kΩ
Phase position without shift time between the middle of the sync pulse at pin 5 and the middle of the horizontal blanking pulse at pin 17		t_d	2.1	2.5	2.9	μs
Vertical ramp generator (pin 3)						
Pulse width charge current		–	–	26	–	clock pulses
Charge current		I_3	–	3	–	mA
Top level ramp signal voltage						
Divider in 50 Hz mode	note 7	V_3	5.5	5.85	6.3	V
Divider in 60 Hz mode	note 7	V_3	4.7	5.0	5.4	V
Ramp amplitude	C_3 = 150 nF,					
R_4 = 330 kΩ 50 Hz	note 7		–	3.1	–	V_P
R_4 = 330 kΩ 60 Hz	note 7		–	2.5	–	V_P
Temperature coefficient	I_4 = 30 μA	I_3	–	+ 100	–	10^{-6}/K

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Current source (pin 4)						
Output voltage	$I_4 = 30\ \mu A$	V_4	7.2	7.7	8.1	V
Allowed current range		I_4	10	–	75	μA
Temperature coefficient output voltage	$I_4 = 30\ \mu A$	TC	–	+ 50	–	$10^{-6}/K$
Comparator (pin 2)	$C_3 = 150$ nF; $R_4 = 330\ k\Omega$					
Input voltage						
DC level	note 7	V_2	0.9	1.0	1.1	V
AC level		V_2	–	0.8	–	V_P
Deviation amplitude 50/60 Hz			–	1.75	2.5	%
Vertical output stage (pin 1) (npn emitter follower)						
Output voltage	I_O pin 1 = +1.5 mA					
	note 7	V_1	5.2	5.7	6.5	V
R_S, sync separator resistor			–	150	–	Ω
Continuous sink current			–	0.35	–	mA
Vertical guard circuit (pin 2)						
Active ($V_{17} = 2.5$ V)						
Switching level LOW	note 7	V_2	> 1.7	1.85	2.0	V
Switching level HIGH	note 7	V_2	< 0.25	0.35	0.45	V

Notes to the characteristics

1. Up to 1 V peak-to-peak the slicing level is constant, at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.
2. The slicing level is fixed by the formula:

$$P = \frac{R_S}{5.3 + R_S} \times 100\% \quad (R_S \text{ value in } k\Omega)$$

3. $$S/N = 20 \log \frac{\text{video voltage black to white (p-p)}}{\text{noise (rms)}}$$

   measured with 1 $V_{p\text{-}p}$ video input
4. Measured between pin 5 and sandcastle output pin 17.
5. Divider in search (large) mode:
   start: reset divider = start vertical sync plus 1 clock pulse
   stop:

$$n = \frac{2 \times f_H}{f_V} > 576 \text{ clock pulse } 42$$

$$n = \frac{2 \times f_H}{f_V} < 576 \text{ clock pulse } 34$$

   Divider in small window mode:
   start: clock pulse 517 (60 Hz) clock pulse 619 (50 Hz)
   stop: clock pulse 34 (60 Hz) clock pulse 42 (50 Hz)
6. Depends on DC level of pin 5, given value is valid for $V_5 \approx 5$ V.
7. Value related to internal zener diode reference voltage source spread includes the complete spread of reference voltage.

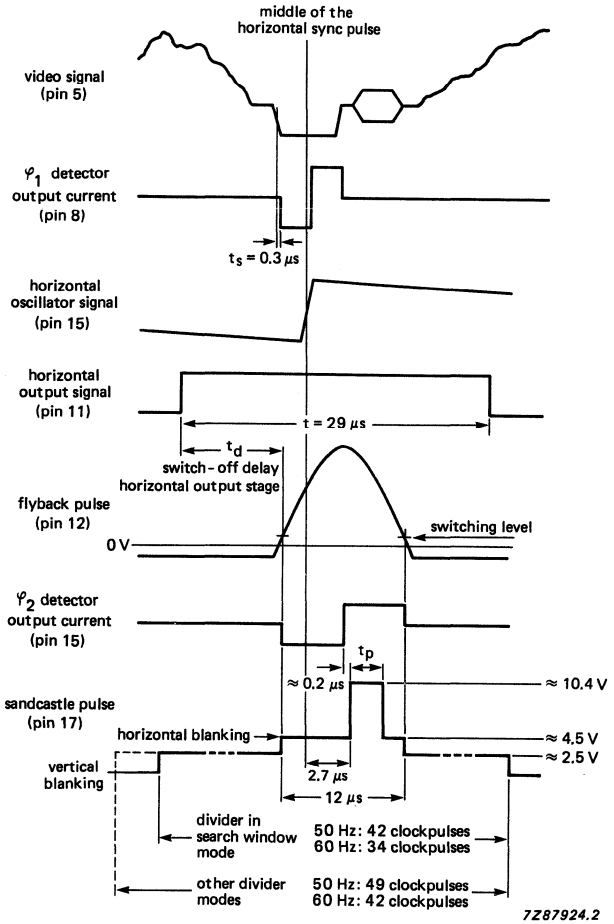


Fig. 3 Timing diagram of the TDA2579A.

APPLICATION INFORMATION

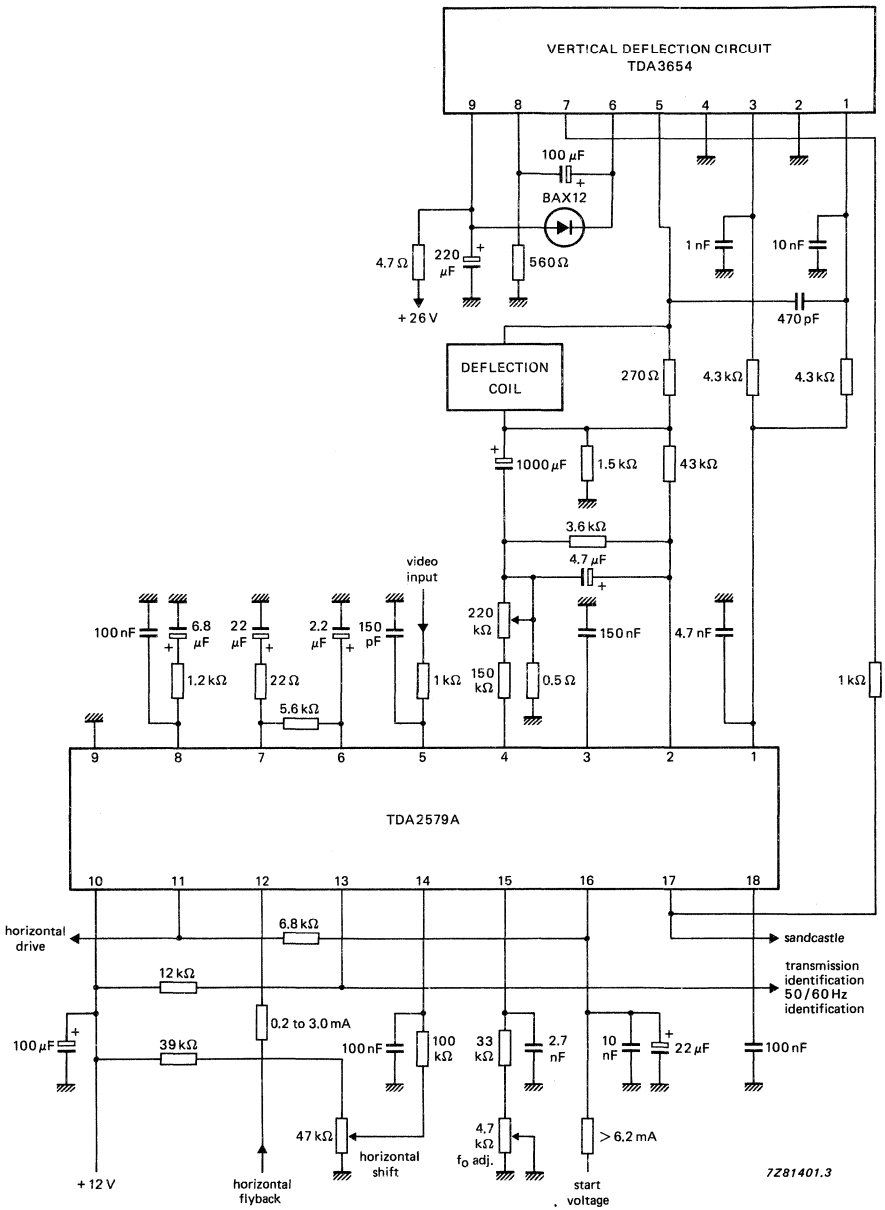


Fig. 4 TDA2579A 110° application circuit (45AX).

CONTROL CIRCUIT FOR POWER SUPPLIES

The TDA2582 is a monolithic integrated circuit for controlling power supplies which are provided with the drive for the horizontal deflection stage.
The circuit features the following:

- Voltage controlled horizontal oscillator.
- Phase detector.
- Duty factor control for the negative-going transient of the output signal.
- Duty factor increases from zero to its normal operation value.
- Adjustable maximum duty factor.
- Over-voltage and over-current protection with automatic re-start after switch-off.
- Counting circuit for permanent switch-off when n-times over-current or over-voltage is sensed.
- Protection for open-reference voltage.
- Protection for too low supply voltage.
- Protection against loop faults.
- Positive tracking of duty factor and feedback voltage when the feedback voltage is smaller than the reference voltage minus 1,5 V.
- Normal and 'smooth' remote ON/OFF possibility.

QUICK REFERENCE DATA

Supply voltage	$V_{9\text{-}16}$	typ.	12 V
Supply current	I_9	typ.	14 mA
Input signals			
Horizontal drive pulse (peak-to-peak value)	$V_{3\text{-}16(p\text{-}p)}$		5 to 11 V
Flyback pulse (differentiated deflection current); peak-to-peak value	$V_{2\text{-}16(p\text{-}p)}$		1 to 5 V
External reference voltage	$V_{10\text{-}16}$	typ.	6,1 V
Output signals			
Duty factor of output pulse	δ	$>$ $<$	0 % 98 ± 0,8 %
Output voltage at $I_O < 20$ mA (peak value)	$V_{11\text{-}16M}$	typ.	11,8 V
Output current (peak value)	I_{11M}	$<$	40 mA

PACKAGE OUTLINES

TDA2582 : 16-lead DIL; plastic (SOT38).
TDA2582Q: 16-lead QIL; plastic (SOT58).

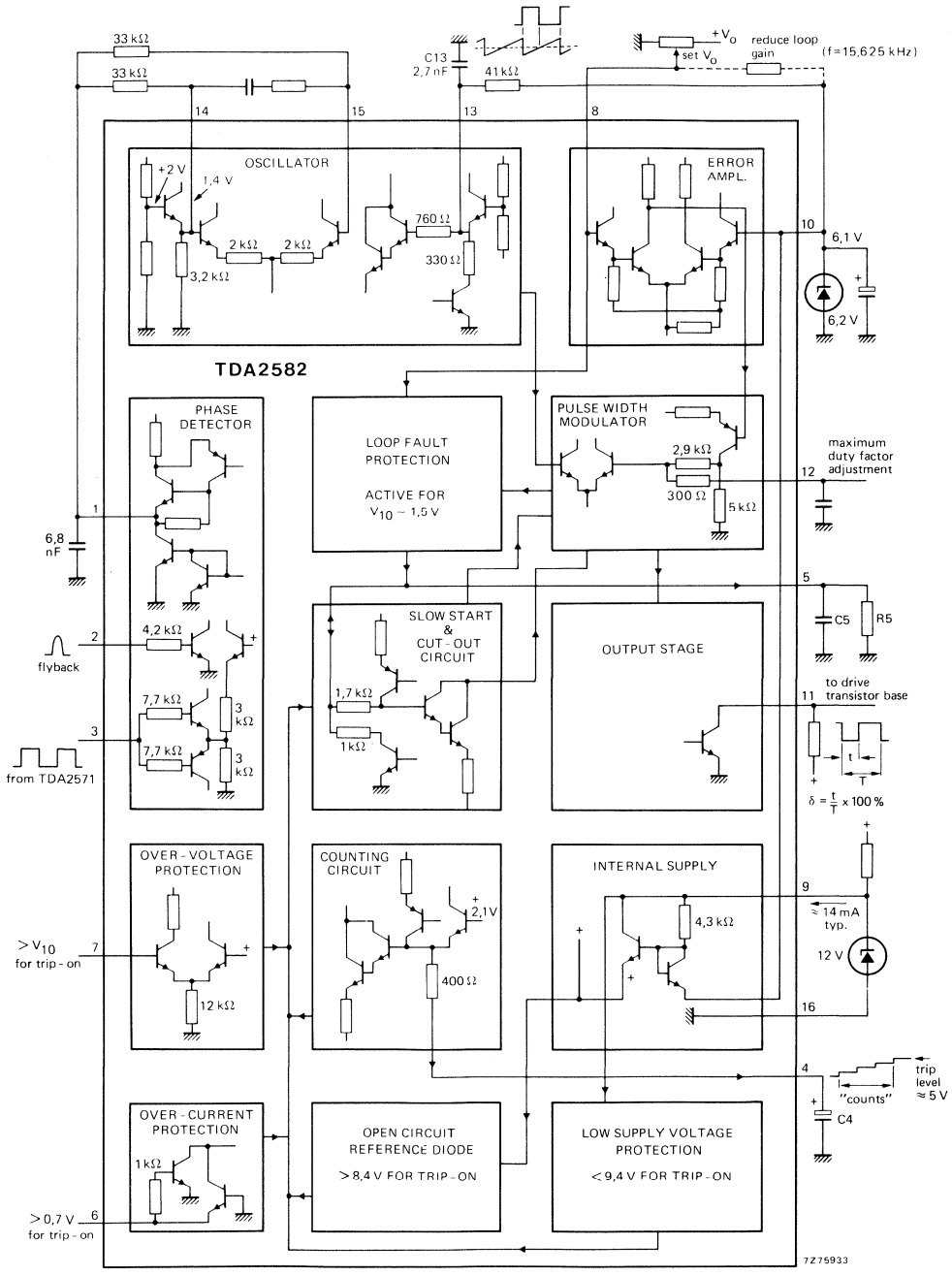


Fig. 1 Block diagram.

Note: trip levels are nominal values.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage at pin 9	V_{9-16}	max. 14	V
Voltage at pin 11	V_{11-16}	0 to 14	V
Output current (peak value)	I_{11M}	max. 40	mA
Total power dissipation	P_{tot}	max. 280	mW
Storage temperature	T_{stg}	−25 to + 125	°C
Operating ambient temperature	T_{amb}	−25 to + 80	°C

CHARACTERISTICS

V_{9-16} = 12 V; V_{10-16} = 6,1 V; T_{amb} = 25 °C; measured in Fig. 4

Supply voltage range	V_{9-16}	typ. 12 10 to 14	V V
Protection voltage too low supply voltage	V_{9-16}	typ. 9,4 8,6 to 9,9	V V
Supply current at δ = 50%	I_9	typ. 14	mA
Supply current during protection	I_9	typ. 14	mA
Minimum required supply current (note 1)	I_9	< 17	mA
Power consumption	P	typ. 170	mW
Required input signals			
Reference voltage (note 2)	V_{10-16}	typ. 6,1 5,6 to 6,6	V V
Feedback input impedance	$\lvert Z_{8-16} \rvert$	typ. 200	kΩ
High reference voltage protection: threshold voltage	V_{10-16}	typ. 8,4 7,9 to 8,9	V V
Horizontal reference signal (square-wave or differentiated; negative transient is reference)			
Voltage driven (peak-to-peak value)	$V_{3-16(p-p)}$	5 to 12	V
Current driven (peak value)	I_{3M}	−1 to + 1,5	mA
Switching level current	$\pm I_3$	< 100	μA
Flyback pulse or differential deflection current	V_{2-16}	1 to 5	V
Flyback pulse current (peak value)	I_{2M}	< 1,5	mA
Over-current protection: (note 3) threshold voltage	$-V_{6-16}$	typ. 640 600 to 695	mV mV
	$+V_{6-16}$	typ. 680 640 to 735	mV mV

Notes

1. This value refers to the minimum required supply current that will start all devices under the following conditions: V_{9-16} = 10 V; V_{10-16} = 6,2 V; δ = 50%.
2. Voltage obtained via an external reference diode. Specified voltages do not refer to the nominal voltages of reference diodes.
3. This spread is inclusive temperature rise of the IC due to warming up. For other ambient temperatures the values must be corrected by using a temperature coefficient of typical −1,85 mV/°C.

CHARACTERISTICS (continued)

Over-voltage protection: ($V_{ref} = V_{10-16}$) threshold voltage	V_{7-16}	typ.	$V_{ref}-60$ mV
			$V_{ref}-130$ to $V_{ref}-0$ mV
Remote control voltage; switch-off (note 1)	V_{4-16}	>	5,6 V
Remote control voltage; switch-on	V_{4-16}	<	4,5 V
'Smooth' remote control; switch-off (note 2)	V_{5-16}	>	4,5 V
'Smooth' remote control; switch-on	V_{5-16}	<	3 V
Remote control switch-off current	I_4	<	1 mA
Delivered output signals			
Horizontal drive pulse (loaded with a resistor of 560 Ω to + 12 V peak-to-peak value	$V_{11-16(p-p)}$	>	11,6 V
Output current; peak value	I_{11M}	<	40 mA
Saturation voltage of output transistor at I_{11} = 20 mA	V_{CEsat}	typ.	200 mV
		<	400 mV
at I_{11} = 40 mA	V_{CEsat}	<	525 mV
Duty factor of output pulse (note 3)	δ	>	0 %
		<	98 ± 0,8 %
Charge current for capacitor on pin 4	I_4	typ.	110 μA
Charge current for capacitor on pin 5	I_5	typ.	120 μA
Supply current for reference	I_{10}	typ.	1 mA
			0,6 to 1,45 mA
Oscillator			
Temperature coefficient		typ.	0,0003 $^oC^{-1}$
		<	0,0004 $^oC^{-1}$
Relative frequency deviation for V_{10-16} changing from 5,6 to 6,6 V		typ.	−1,4 %
		<	−2 %
Oscillator frequency spread (with fixed external components)		<	3 %
Frequency control sensitivity at pin 15 f_{nom} = 15,625 kHz		typ.	5 kHz/V

Notes

1. See application information pin 4.
2. See application information pin 5.
3. The duty factor is specified as follows: $\delta = \frac{t_p}{T} \times 100\%$

   (see Fig. 2). After switch-on the duty factor rises gradually from 0% to the steady value. The relationship between V_{8-16} and the duty factor is given in Fig. 7 and the relationship between V_{12-16} and the duty factor is shown in Fig. 9.

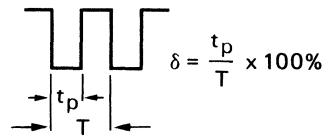


Fig. 2.

Phase control loop

Loop gain of APC-system (automatic phase control) *		typ.	5	kHz/μs
Catching range (f_{nom} = 15,625 kHz)	Δf	>	1300	Hz
		<	2100	Hz
Phase relation between negative transient of sync pulse and middle of flyback	t	typ.	1	μs
Tolerance of phase relation	Δt	⩽	± 0,4	μs

PINNING

1. Phase detector output
2. Flyback pulse position input
3. Reference frequency input
4. Re-start count capacitor/remote control input
5. Slow start and transfer characteristic for low feedback voltages
6. Over-current protection input
7. Over-voltage protection input
8. Feedback voltage input
9. Positive supply
10. Reference input
11. Output
12. Maximum duty factor adjustment/smoothing
13. Oscillator timing network
14. Reactance stage reference voltage
15. Reactance stage input
16. Negative supply (ground)

* For component values see Fig. 1.

APPLICATION INFORMATION

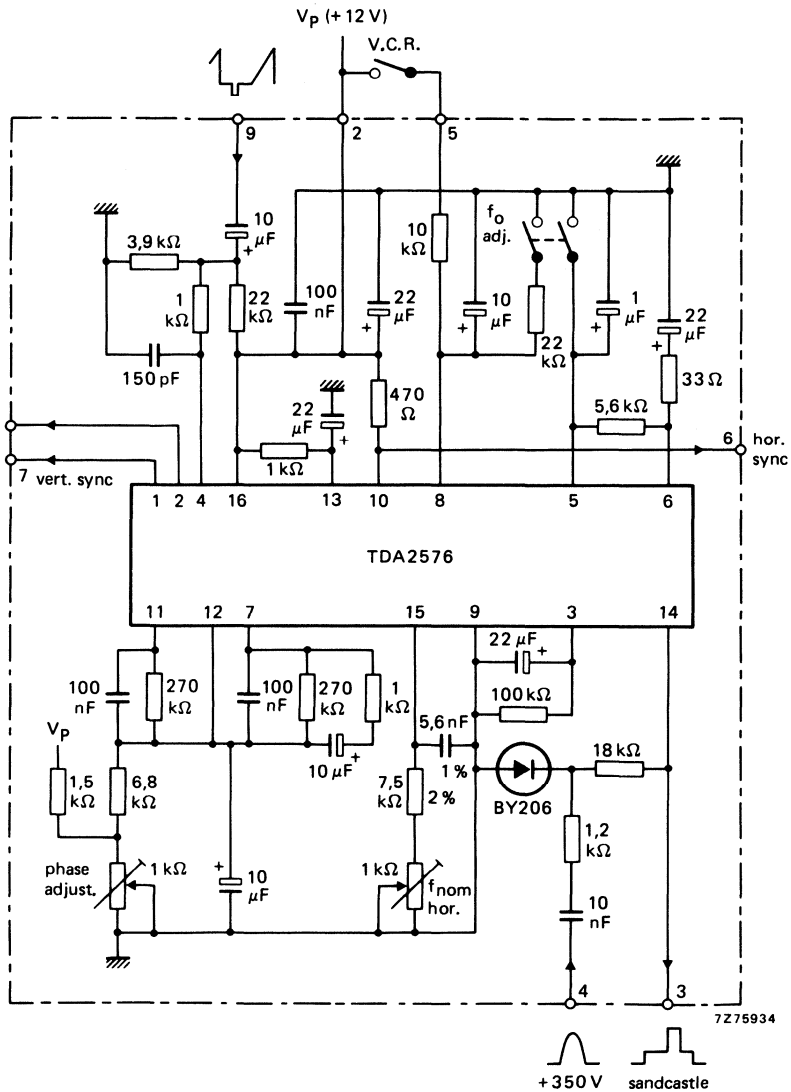


Fig. 3a.

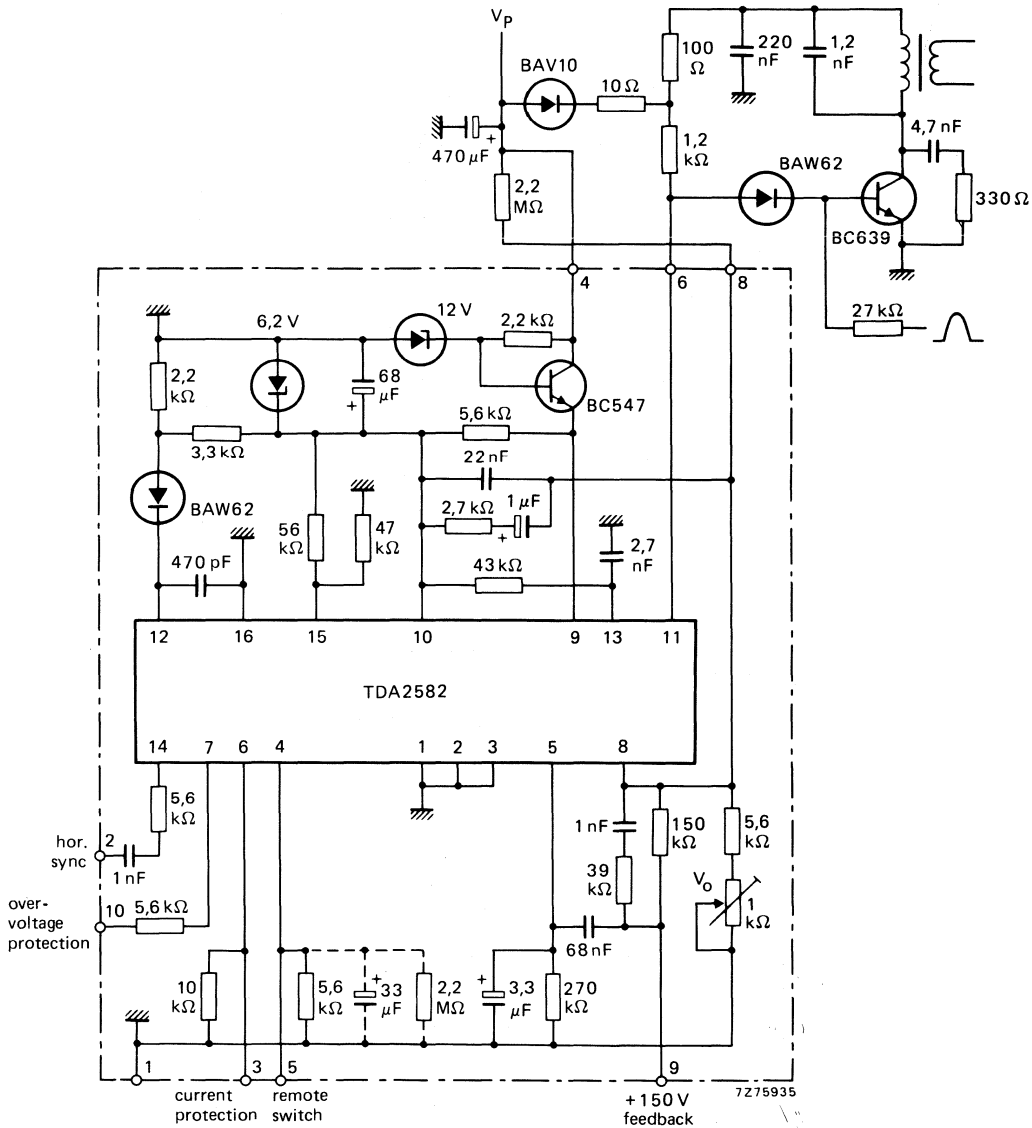


Fig. 3b.

Lead 6 (pin 10) of circuit TDA2576 connected to lead 2 (pin 14) of circuit TDA2582.

APPLICATION INFORMATION

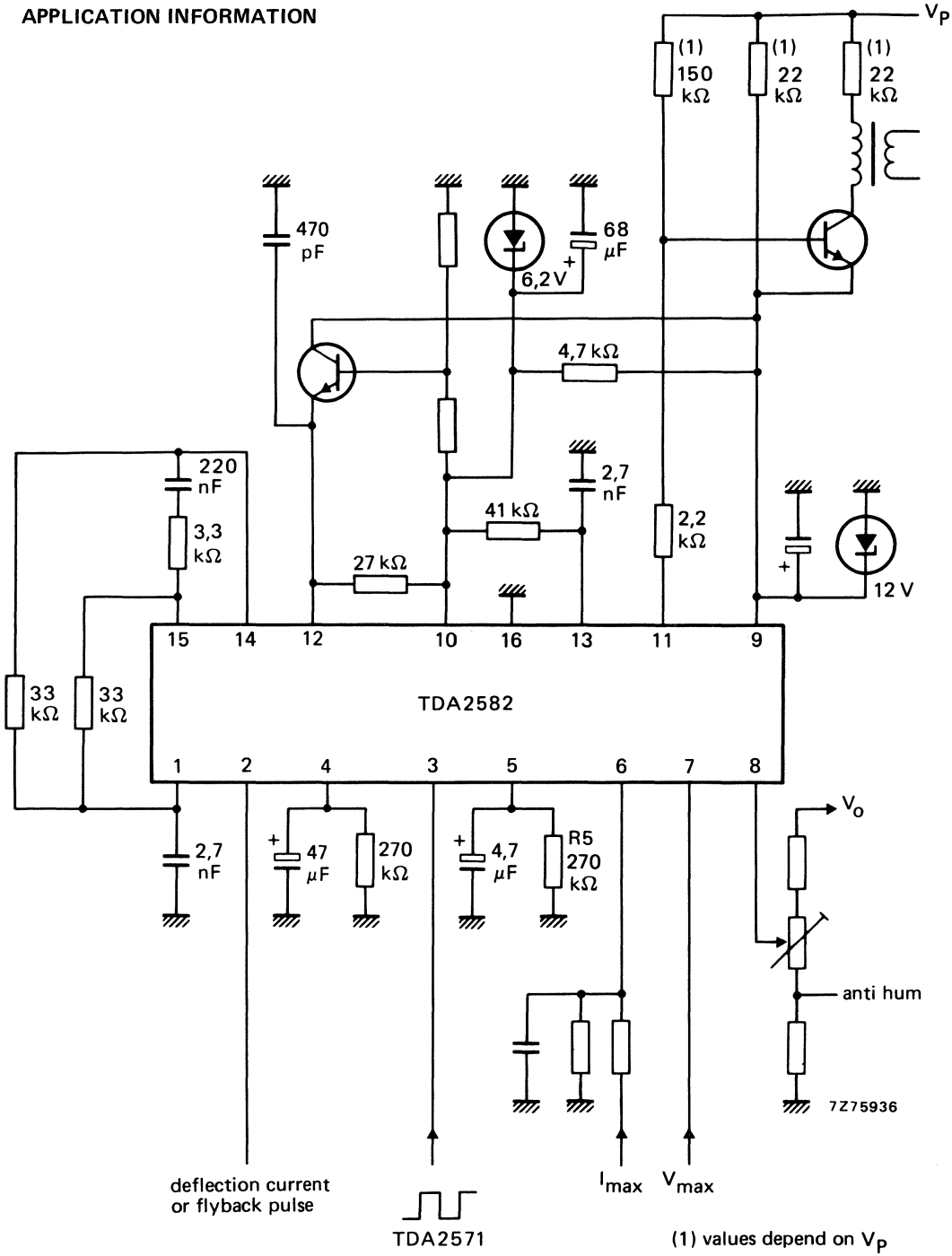


Fig. 4 Circuit diagram.

The function is described against the corresponding pin number

1. Phase detector output

The output circuit consists of a bidirectional current source which is active for the time that the signal on pin 2 exceeds 1 V.
The current values are chosen such that the correct phase relation is obtained when the output signal of the TDA2571 is applied to pin 3.
With a resistor of 2 x 33 kΩ and a capacitor of 2,7 nF the control steepness is 0,55 V/μs (Fig. 4).

2. Flyback pulse input

The signal applied to pin 2 is normally a flyback pulse with a duration of about 12 μs. However, the phase detector system also accepts a signal derived by differentiating the deflection current by means of a small toroidal core (pulse duration > 3 μs).

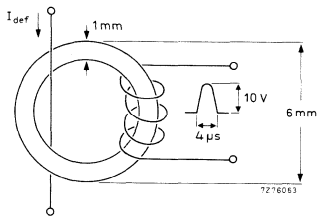


Fig. 5a.

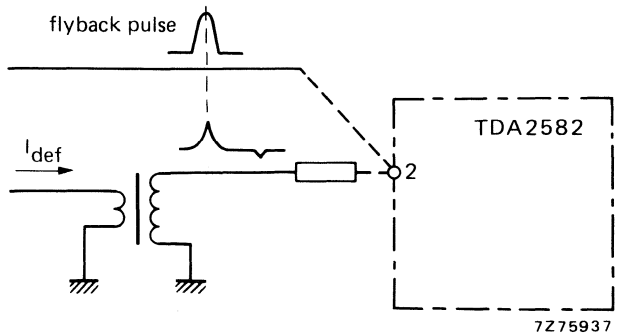


Fig. 5b.

The toroidal transformer in Fig. 5a is for obtaining a pulse representing the mid-flyback from the deflection current. The connection of the picture phase information is shown in Fig. 5b.

3. Reference frequency input

The input circuit can be driven directly by the square-wave output voltage from pin 8 of the TDA2571.
The negative-going transient switches the current source connected to pin 1 from positive to negative.
The input circuit is made such that a differentiated signal of the square-wave from the TDA2571 is also accepted (this enables mains isolation). The input circuit switching level is about 3 V and the input impedance is about 8 kΩ.

4. Re-start count capacitor/remote control input

Counting

An external capacitor (C4 = 47 μF) is connected between pins 4 and 16. This capacitor controls the characteristics of the protection circuits as follows.
If the protection circuits are required to operate, e.g. over-current at pin 6, the duty factor will be set to zero thus turning off the power supply.
After a short interval (determined by the time constant on pin 5) the power supply will be restarted via the slow start circuit.
If the fault condition has cleared, then normal operation will be resumed. If the fault condition is persistent, the duty factor of the pulses is again reduced to zero and the protection cycle is repeated.

The number of times this action is repeated (n) for a persisting fault condition is now determined by: n = C4/C5.

APPLICATION INFORMATION (continued)

Remote control input

For this application the capacitor on pin 4 has to be replaced by a resistor with a value between 4,7 and 18 kΩ. When the externally applied voltage $V_{4\text{-}16} > 5{,}6$ V, the circuit switches off; switching on occurs when $V_{4\text{-}16} < 4{,}5$ V and the normal starting-up procedure is followed. Pin 4 is internally connected to an emitter-follower, with an emitter voltage of 1,5 V.

5. Slow start and transfer characteristics for low feedback voltages

Slow start

An external shunt capacitor (C5 = 4,7 μF) and resistor (R5 = 270 kΩ) are connected between pins 5 and 16. The network controls the rate at which the duty factor increases from zero to its steady-state value after switch-on. It provides protection against surges in the power transistor.

Transfer characteristic for low feedback voltages

The duty factor transfer characteristic for low feedback voltages can be influenced by R5. The transfer for three different resistor values is given in Fig. 7.

'Smooth' remote ON/OFF

The ON/OFF information should be applied to pin 5 via a high ohmic resistor, a high OFF-level gives a slow rising voltage at pin 5, which results in a slowly decreasing duty factor.

6. Over-current protection input

A voltage proportional to the current in the power switching device is applied to the integrated circuit between pins 6 and 16. The circuit trips on both positive and negative polarity. When the tripping level is reached, the output pulse is immediately blocked and the starting circuit is activated again.

7. Over-voltage protection input

When the voltage applied to this pin exceeds the threshold level the protection circuit will operate. The tripping level is about the same as the reference voltage on pin 10.

8. Feedback voltage input

The control loop input is applied to pin 8. This pin is internally connected to one input of a differential amplifier, functioning as an amplitude comparator, the other input of which is connected to the reference source on pin 10.
Under normal operating conditions, the voltage on pin 8 will be about equal to the reference voltage on pin 10. For further information refer to the Figs 7 and 8.

9. 12 V positive supply

The maximum voltage that may be applied is 14 V. Where this is derived from an unstabilized supply rail, a regulator diode (12 V) should be connected between pins 9 and 16 to ensure that the maximum voltage does not exceed 14 V. When the voltage on this pin falls below a minimum of 8,6 V (typically 9,4 V), the protection circuit will switch-off the power supply.

10. Reference input

An external reference diode must be connected between this pin and pin 16.
The reference voltage must be between 5,6 and 6,6 V. The IC delivers about 1 mA into the external regulator diode. When the external load on the regulator diode approaches this current, replenishment of the current can be obtained by connecting a suitable resistor between pins 9 and 10. A higher reference voltage value up to 7,5 V is allowed when use is made of a duty factor limiting resistor < 27 kΩ between pins 12 and 16.

11. Output

An external resistor determines the output current fed into the base of the driver transistor. The output circuit uses an n-p-n transistor with 3 series-connected clamping diodes to the internal 12 V supply rail. This provides a low impedance in the "ON" state, that is with the drive transistor turned-off.

12. Maximum duty factor adjustment/smoothing

Maximum duty factor adjustment

Pin 12 is connected to the output voltage of the amplitude comparator ($V_{10\text{-}8}$). This voltage is internally connected to one input of a differential amplifier, the other input of which is connected to the sawtooth voltage of the horizontal oscillator. A high voltage on pin 12 results in a low duty factor. This enables the maximum duty factor to be adjusted by limiting the voltage by connecting pin 12 to the emitter of an n-p-n transistor used as a voltage source.
Fig. 9 plots the maximum duty factor as a function of the voltage applied to pin 12. If some spread is acceptable the maximum duty factor can also be limited by connecting a resistor from pin 12 to pin 16. A resistor of 12 kΩ limits the maximum duty factor to about 50%. This application also reduces the total IC gain.

Smoothing

Any double pulsing of the IC due to circuit layout can be suppressed by connecting a capacitor of about 470 pF between pins 12 and 16.

13. Oscillator timing network

The timing network comprises a capacitor between pins 13 and 16, and a resistor between pin 13 and the reference voltage on pin 10.
The charging current for the capacitor (C13) is derived from the voltage reference diode connected to pin 10 and discharged via an internal resistor of about 330 Ω.

14. Reactance stage reference voltage

This pin is connected to an emitter follower which determines the nominal reference voltage for the reactance stage (1,4 V for reference voltage $V_{10\text{-}16} = 6{,}1$ V). Free-running frequency is obtained when pins 14 and 15 are short-circuited.

15. Reactance stage input

The output voltage of the phase detector (pin 1) is connected to pin 15 via a resistor. The voltage applied to pin 15 shifts the upper level of the voltage sensor of the oscillator thus changing the oscillator frequency and phase. The time constant network is connected between 14 and 15. Control sensitivity is typically 5 kHz/V.

16. Negative supply (ground)

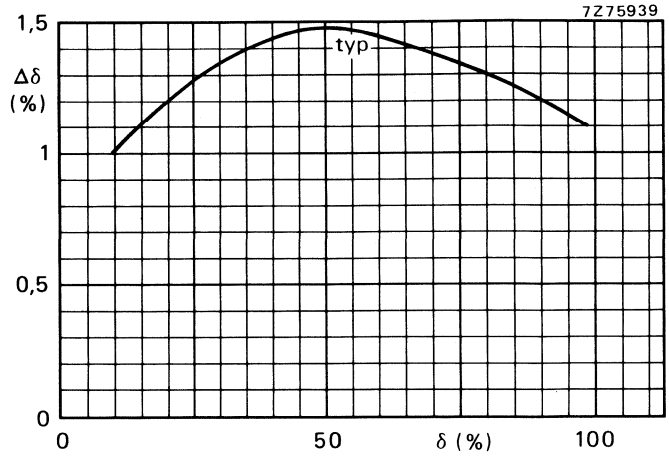


Fig. 6 Duty factor change as a function of initial duty factor; at 1 mV error amplifier input change; $\Delta V_{8\text{-}10(p\text{-}p)}$ = 1 mV.

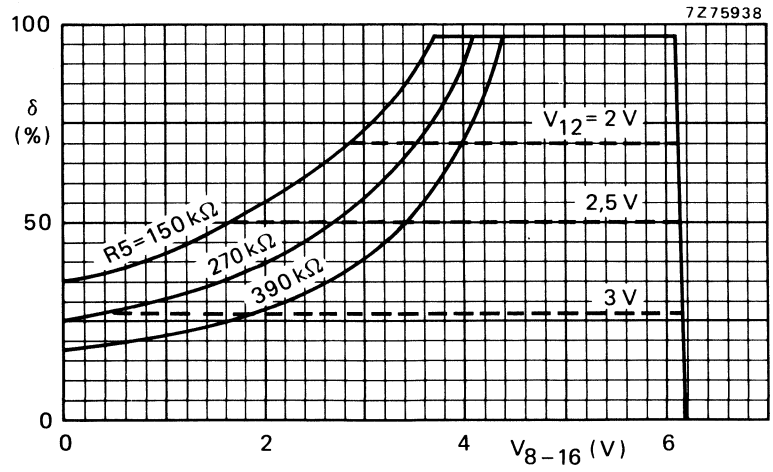


Fig. 7 Duty factor of output pulses as a function of feedback input voltage ($V_{8\text{-}16}$) with R5 as a parameter and $V_{12\text{-}16}$ as a limiting value; $V_{10\text{-}16}$ = 6,1 V.

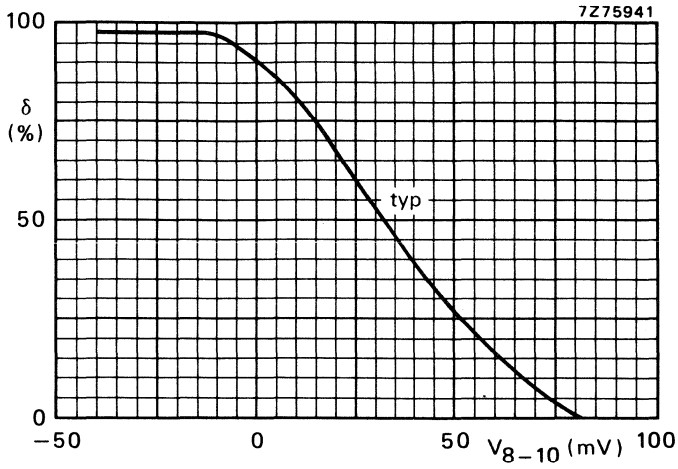


Fig. 8 Duty factor of output pulses as a function of error amplifier input (V_{8-10}); V_{10-16} = 6,1 V.

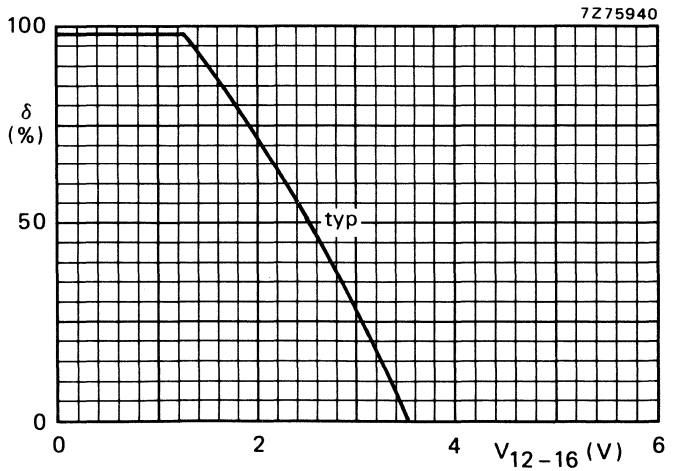


Fig. 9 Maximum duty factor limitation as a function of the voltage applied to pin 12; V_{10-16} = 6,1 V.

HORIZONTAL COMBINATION

The TDA2593 is a monolithic integrated circuit intended for use in colour television receivers in combination with TDA2510, TDA2520, TDA2560 as well as with TDA3500, TDA3510 and TDA3520. The circuit incorporates the following functions:

- horizontal oscillator based on the threshold switching principle
- phase comparison between sync pulse and oscillator voltage (φ_1)
- internal key pulse for phase detector (φ_1) (additional noise limiting)
- phase comparison between line flyback pulse and oscillator voltage (φ_2)
- larger catching range obtained by coincidence detector (φ_3; between sync and key pulse)
- switch for changing the filter characteristic and the gate circuit (VCR-operation)
- sync separator
- noise separator
- vertical sync separator and output stage
- colour burst keying and line flyback blanking pulse generator
- phase shifter for the output pulse
- output pulse duration switching
- output stage with separate supply voltage for direct drive of thyristor deflection circuits
- low supply voltage protection

QUICK REFERENCE DATA

Supply voltage	$V_{1\text{-}16}$	typ.	12 V
Supply current	I_1	typ.	30 mA
Input signals			
Sync separator input voltage (peak-to-peak value)	$V_{9\text{-}16(p\text{-}p)}$		3 to 4 V
Noise separator input voltage (peak-to-peak value)	$V_{10\text{-}16(p\text{-}p)}$		3 to 4 V
Pulse duration switch input voltage			
at t = 7 μs (thyristor driving)	$V_{4\text{-}16}$		9,4 to $V_{1\text{-}16}$ V
at t = 14 μs + t_d (transistor driving)	$V_{4\text{-}16}$		0 to 3,5 V
at t = 0 (input 4 open or $V_{3\text{-}16}$ = 0)	$V_{4\text{-}16}$		5,4 to 6,6 V
Output signals			
Vertical sync output pulse (peak-to peak value)	$V_{8\text{-}16(p\text{-}p)}$	typ.	11 V
Burst gating output pulse (peak-to-peak value)	$V_{7\text{-}16(p\text{-}p)}$	typ.	11 V
Line drive pulse (peak-to-peak value)	$V_{3\text{-}16(p\text{-}p)}$	typ.	10,5 V

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

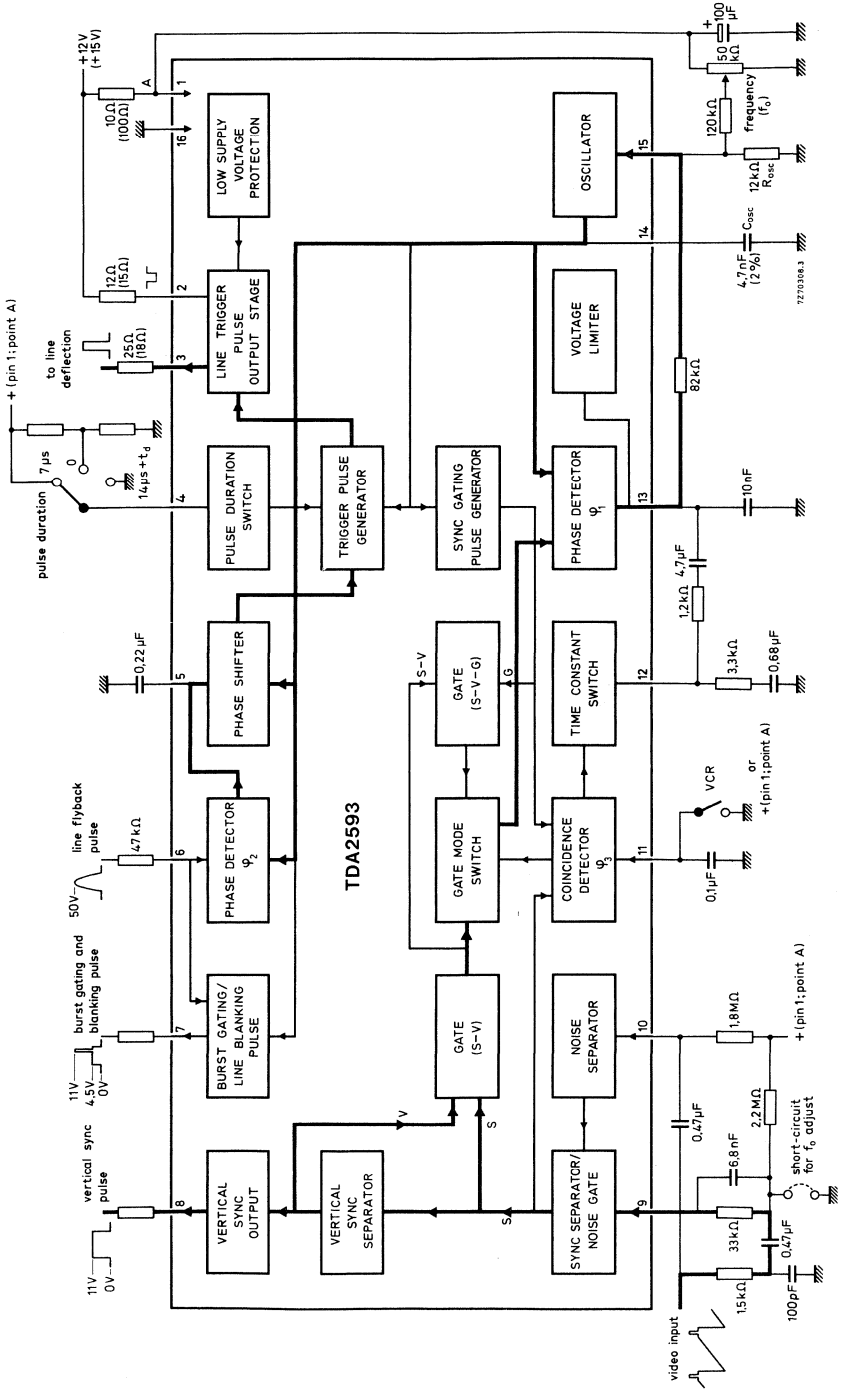


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage				
at pin 1 (voltage source)	V_{1-16}	max.	13,2	V
at pin 2	V_{2-16}	max.	18	V
Voltages				
Pin 4	V_{4-16}	max.	13,2	V
Pin 9	$\pm V_{9-16}$	max.	6	V
Pin 10	$\pm V_{10-16}$	max.	6	V
Pin 11	V_{11-16}	max.	13,2	V
Currents				
Pins 2 and 3 (thyristor driving) (peak value)	$I_{2M}, -I_{3M}$	max.	650	mA
Pins 2 and 3 (transistor driving) (peak value)	$I_{2M}, -I_{3M}$	max.	400	mA
Pin 4	I_4	max.	1	mA
Pin 6	$\pm I_6$	max.	10	mA
Pin 7	$-I_7$	max.	10	mA
Pin 11	I_{11}	max.	2	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature	T_{stg}		−25 to + 125	°C
Operating ambient temperature	T_{amb}		0 to + 70	°C

CHARACTERISTICS at $V_{1-16} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1

Sync separator

Input switching voltage	V_{9-16}	typ.	0,8	V
Input keying current	I_9		5 to 100	μA
Input leakage current at $V_{9-16} = -5$ V	I_9	<	1	μA
Input switching current	I_9	⩽	5	μA
Switch off current	I_9	>	100	μA
		typ.	150	μA
Input signal (peak-to-peak value)	$V_{9-16(p-p)}$		3 to 4	V*

* Permissible range 1 to 7 V.

Noise separator				
Input switching voltage	$V_{10\text{-}16}$	typ.	1,4	V
Input keying current	I_{10}		5 to 100	μA
Input switching current	I_{10}	>	100	μA
		typ.	150	μA
Input leakage current at $V_{10\text{-}16} = -5$ V	I_{10}	<	1	μA
Input signal (peak-to-peak value)	$V_{10\text{-}16(p\text{-}p)}$		3 to 4	V *
Permissible superimposed noise signal (peak-to-peak value)	$V_{10\text{-}16(p\text{-}p)}$	<	7	V
Line flyback pulse				
Input current	I_6	typ.	1	mA
			0,02 to 2	mA
Input switching voltage	$V_{6\text{-}16}$	typ.	1,4	V
Input limiting voltage	$V_{6\text{-}16}$		−0,7 to + 1,4	V
Switching on VCR				
Input voltage	$V_{11\text{-}16}$		0 to 2,5	V
	$V_{11\text{-}16}$		9 to $V_{1\text{-}16}$	V
Input current	$-I_{11}$	<	200	μA
	I_{11}	<	2	mA
Pulse duration switch				
For t = 7 μs (thyristor driving)				
Input voltage	$V_{4\text{-}16}$		9,4 to $V_{1\text{-}16}$	V
Input current	I_4	>	200	μA
For t = 14 μs + t_d (transistor driving)				
Input voltage	$V_{4\text{-}16}$		0 to 3,5	V
Input current	$-I_4$	>	200	μA
For t = 0; $V_{3\text{-}16} = 0$ or input pin 4 open				
Input voltage	$V_{4\text{-}16}$		5,4 to 6,6	V
Input current	I_4	typ.	0	μA

* Permissible range 1 to 7 V.

Vertical sync pulse (positive-going)			
Output voltage (peak-to-peak value)	$V_{8\text{-}16(p\text{-}p)}$	>	10 V
		typ.	11 V
Output resistance	R_8	typ.	2 kΩ
Delay between leading edge of input and output signal	t_{on}	typ.	15 μs
Delay between trailing edge of input and output signal	t_{off}	typ.	t_{on} μs
Burst gating pulse (positive-going)			
Output voltage (peak-to-peak value)	$V_{7\text{-}16(p\text{-}p)}$	>	10 V
		typ.	11 V
Output resistance	R_7	typ.	70 Ω
Pulse duration; $V_{7\text{-}16}$ = 7 V	t_p	typ.	4 μs
			3,7 to 4,3 μs
Phase relation between middle of sync pulse at the input and the leading edge of the burst gating pulse; $V_{7\text{-}16}$ = 7 V	t	typ.	2,65 μs
			2,15 to 3,15 μs
Output trailing edge current	I_7	typ.	2 mA
Line flyback-blanking pulse (positive-going)			
Output voltage (peak-to-peak value)	$V_{7\text{-}16(p\text{-}p)}$		4 to 5 V
Output resistance	R_7	typ.	70 Ω
Output trailing edge current	I_7	typ.	2 mA
Line drive pulse (positive-going)			
Output voltage (peak-to-peak value)	$V_{3\text{-}16(p\text{-}p)}$	typ.	10,5 V
Output resistance			
for leading edge of line pulse	R_3	typ.	2,5 Ω
for trailing edge of line pulse	R_3	typ.	20 Ω
Pulse duration (thyristor driving)			
$V_{4\text{-}16}$ = 9,4 to $V_{1\text{-}16}$ V	t_p	typ.	7 μs
			5,5 to 8,5 μs
Pulse duration (transistor driving)			
$V_{4\text{-}16}$ = 0 to 4 V; t_{fp} = 12 μs	t_p		14 + t_d μs*
Supply voltage for switching off the output pulse	$V_{1\text{-}16}$	typ.	4 V
Overall phase relation			
Phase relation between middle of sync pulse and the middle of the flyback pulse	t	typ.	2,6 μs**
Tolerance of phase relation	$\lvert \Delta t \rvert$	<	0,7 μs

* t_d = switch-off delay of line output stage.
** Line flyback pulse duration t_{fp} = 12 μs.

The adjustment of the overall phase relation and consequently the leading edge of the line drive pulse occurs automatically by phase control φ_2. If additional adjustment is applied it can be arranged by current supply at pin 5 such that	$\Delta I_5/\Delta t$	typ.	30	$\mu A/\mu s$
Oscillator				
Threshold voltage low level	$V_{14\text{-}16}$	typ.	4,4	V
Threshold voltage high level	$V_{14\text{-}16}$	typ.	7,6	V
Discharge current	$\pm I_{14}$	typ.	0,47	mA
Frequency; free running (C_{osc} = 4,7 nF; R_{osc} = 12 kΩ)	f_o	typ.	15,625	kHz
Spread of frequency	$\Delta f_o/f_o$	<	± 5	%*
Frequency control sensitivity	$\Delta f_o/\Delta I_{15}$	typ.	31	Hz/μA
Adjustment range of network in circuit (Fig. 1)	$\Delta f_o/f_o$	typ.	± 10	%
Influence of supply voltage on frequency	$\frac{\Delta f_o/f_o}{\Delta V/V_{nom}}$	<	± 0,05	%*
Change of frequency when $V_{1\text{-}16}$ drops to 5 V	Δf_o	<	± 10	%*
Temperature coefficient of oscillator frequency		<	$\pm 10^{-4}$	Hz/K*
Phase comparison φ_1				
Control voltage range	$V_{13\text{-}16}$		3,8 to 8,2	V
Control current (peak value)	$\pm I_{13M}$		1,9 to 2,3	mA
Output leakage current at $V_{13\text{-}16}$ = 4 to 8 V	I_{13}	<	1	μA
Output resistance				
at $V_{13\text{-}16}$ = 4 to 8 V	R_{13}	high ohmic		**
at $V_{13\text{-}16}$ < 3,8 V or > 8,2 V	R_{13}	low ohmic		▲
Control sensitivity		typ.	2	kHz/μs
Catching and holding range (82 kΩ beteeen pins 13 and 15)	Δf	typ.	± 780	Hz
Spread of catching and holding range	$\Delta(\Delta f)$	typ.	± 10	%*

* Excluding external component tolerances.
** Current source.
▲ Emitter follower.

Phase comparison φ_2 and phase shifter

Control voltage range	$V_{5\text{-}16}$		5,4 to 7,6	V
Control current (peak value)	$\pm I_{5M}$	typ.	1	mA
Output resistance				
at $V_{5\text{-}16}$ = 5,4 to 7,6 V			high ohmic	*
at $V_{5\text{-}16} < 5{,}4$ V or $> 7{,}6$ V	R_5	typ.	8	kΩ
Input leakage current				
$V_{5\text{-}16}$ = 5,4 to 7,6 V	I_5	<	5	μA
Permissible delay between leading edge of output pulse and leading edge of flyback pulse (t_{fp} = 12 μs)	t_d	<	15	μs
Static control error	$\Delta t/\Delta t_d$	<	0,2	%

Coincidence detector φ_3

Output voltage	$V_{11\text{-}16}$		0,5 to 6	V
Output current (peak value)				
without coincidence	I_{11M}	typ.	0,1	mA
with coincidence	$-I_{11M}$	typ.	0,5	mA

Time constant switch

Output voltage	$V_{12\text{-}16}$	typ.	6	V
Output current (limited)	$\pm I_{12}$	<	1	mA
Output resistance				
at $V_{11\text{-}16}$ = 2,5 to 7 V	R_{12}	typ.	0,1	kΩ
at $V_{11\text{-}16} < 1{,}5$ V or > 9 V	R_{12}	typ.	60	kΩ

Internal gating pulse

Pulse duration	t_p	typ.	7,5	μs

* Current source.

HORIZONTAL COMBINATION

The TDA2594 is a monolithic integrated circuit intended for use in colour television receivers.
The circuit incorporates the following functions:

- Horizontal oscillator based on the threshold switching principle.
- Phase comparison between sync pulse and oscillator voltage (φ_1).
- Internal key pulse for phase detector (φ_1) (additional noise limiting).
- Phase comparison between line flyback pulse and oscillator voltage (φ_2).
- Larger catching range obtained by coincidence detector (φ_3; between sync and key pulse).
- Switch for changing the filter characteristic and the gate circuit (VCR-operation).
- Sync separator.
- Noise separator.
- Vertical sync separator and output stage.
- Colour burst keying and line flyback blanking pulse generator and clamp circuit for vertical blanking.
- Phase shifter for the output pulse.
- Output pulse duration for transistor deflection systems.
- External switching off of the line trigger pulse.
- Output stage with separate supply voltage.
- Low supply voltage protection.
- Transmitter identification and muting circuit, and vertical sync switch-off.

QUICK REFERENCE DATA

Supply voltage	$V_{1\text{-}18} = V_S$	typ.	12 V
Supply current	I_1	typ.	30 mA
Input signals			
Sync separator input voltage (peak-to-peak value)	$V_{11\text{-}18(p\text{-}p)}$	typ.	3 V*
Noise separator input voltage (peak-to-peak value)	$V_{12\text{-}18(p\text{-}p)}$	typ.	3 V*
Pulse duration switch input voltage			
at t = 14 μs + t_d (transistor driving)	$V_{4\text{-}18}$		0 to 3,5 V
at t = 0 ($V_{3\text{-}18}$ = 0); input 4 open (I_4 = 0)	$V_{4\text{-}18}$		5,4 to 6,6 V
Output signals			
Vertical sync output pulse (peak-to-peak value)	$V_{8\text{-}18(p\text{-}p)}$	typ.	11 V
Burst key output pulse (peak-to-peak value)	$V_{7\text{-}18(p\text{-}p)}$	typ.	11 V
Line drive-pulse (peak-to-peak value)	$V_{3\text{-}18(p\text{-}p)}$	typ.	10 V

* Permissible range: 1 to 7 V.

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

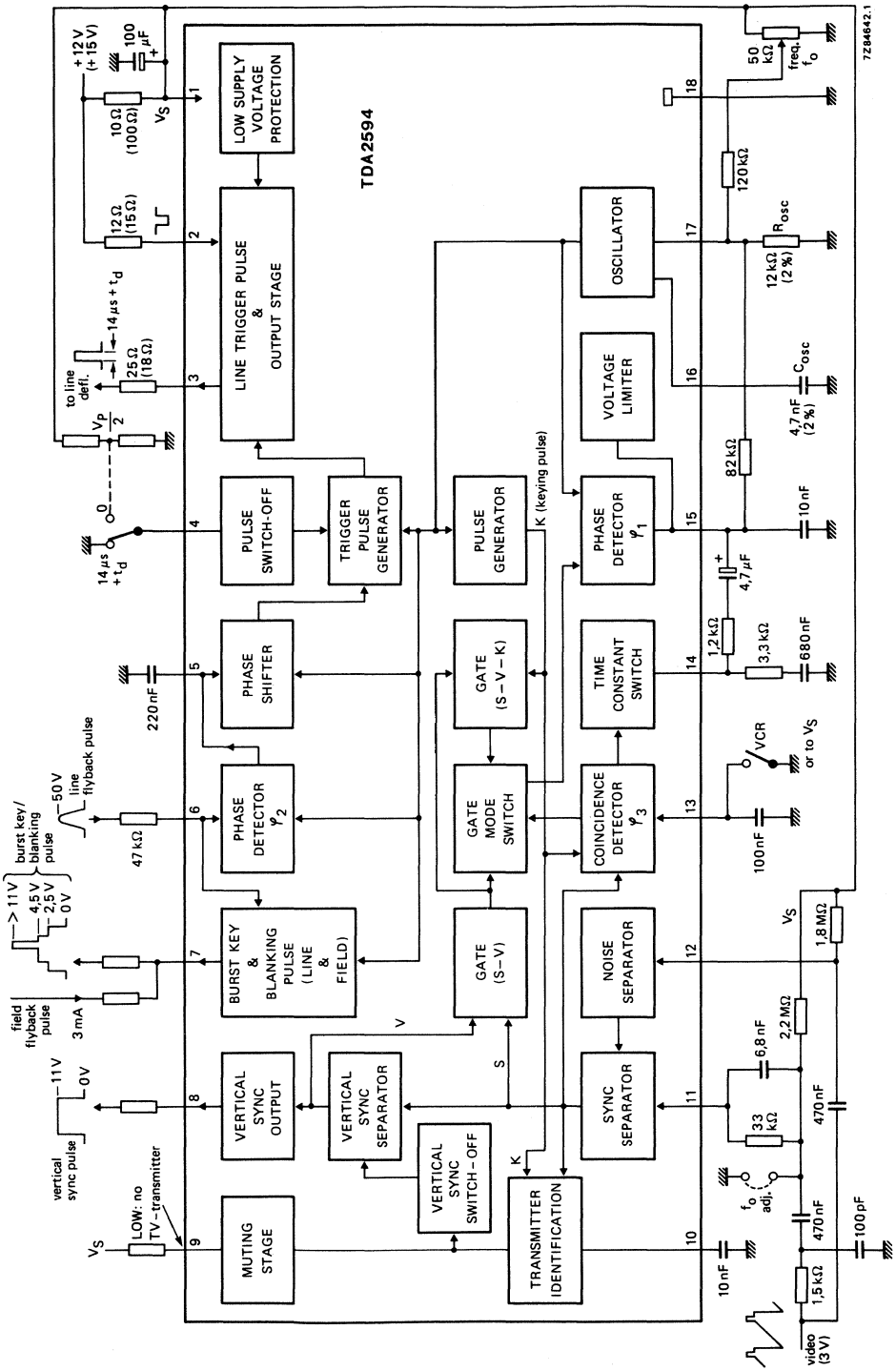


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage			
at pin 1 (voltage source)	$V_{1-18} = V_S$	max.	13,2 V
at pin 2	V_{2-18}	max.	18 V
Voltages			
Pin 4	V_{4-18}	max.	13,2 V
Pin 9	V_{9-18}	max.	18 V
	$-V_{9-18}$	max.	0,5 V
Pin 11	$\pm V_{11-18}$	max.	6 V
Pin 12	$\pm V_{12-18}$	max.	6 V
Pin 13	V_{13-18}	max.	13,2 V
Currents			
Pins 2 and 3 (transistor driving) (peak value)	$I_{2M}, -I_{3M}$	max.	400 mA
Pin 4	I_4	max.	1 mA
Pin 6	$\pm I_6$	max.	10 mA
Pin 7	$-I_7$	max.	5 mA
Pin 9	I_9	max.	10 mA
Pin 13	I_{13}	max.	2 mA
Total power dissipation	P_{tot}	max.	800 mW
Storage temperature range	T_{stg}		−25 to + 125 °C
Operating ambient temperature range	T_{amb}		0 to + 70 °C

CHARACTERISTICS at $V_{1-18} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1

Sync separator (pin 11)

Input switching voltage	V_{11-18}	typ.	0,8 V
Input keying current	I_{11}		5 to 100 μA
Input leakage current at $V_{11-18} = -5$ V	I_{11}	⩽	1 μA
Input switching current	I_{11}	⩽	5 μA
Switch off current	I_{11}	⩾	100 μA
		typ.	150 μA
Input signal (peak-to-peak value)	$V_{11-18(p-p)}$		3 to 4 V*

* Permissible range 1 to 7 V.

Noise separator (pin 12)			
Input switching voltage	V_{12-18}	typ.	1,4 V
Input keying current	I_{12}		5 to 100 μA
Input switching current	I_{12}	⩾ typ.	100 μA 150 μA
Input leakage current at $V_{12-18} = -5$ V	I_{12}	⩽	1 μA
Input signal (peak-to-peak value)	$V_{12-18(p-p)}$		3 to 4 V*
Permissible superimposed noise signal (peak-to-peak value)	$V_{12-18(p-p)}$	⩽	7 V
Line flyback pulse (pin 6)			
Input current	I_6	⩾ typ.	0,02 mA 1 mA
Input switching voltage	V_{6-18}	typ.	1,4 V
Input limiting voltage	V_{6-18}		−0,7 to +1,4 V
Switching on VCR (pin 13)			
Input voltage	V_{13-18} or: V_{13-18}		0 to 2,5 V 9 to V_S V
Input current	$-I_{13}$ or: I_{13}	⩽ ⩽	200 μA 2 mA
Pulse switching off (pin 4)			
For t = 0; input pin 4 open or $V_{3-18} = 0$			
Input voltage	V_{4-18}		5,4 to 6,6 V
Input current	I_4	typ.	0 μA
Vertical sync pulse (positive-going) (pin 8)			
Output voltage (peak-to-peak value)	$V_{8-18(p-p)}$	⩾ typ.	10 V 11 V
Output resistance	R_8	typ.	2 kΩ
Delay between leading edge of input and output signal	t_{on}	typ.	15 μs
Delay between trailing edge of input and output signal	t_{off}	⩾	t_{on} μs
Switching off the vertical sync pulse	V_{10-18}	⩽	3 V
Burst key pulse (positive-going) (pin 7)			
Output voltage	V_{7-18}	⩾ typ.	10 V 11 V
Output resistance	R_7	typ.	70 Ω
Pulse duration; $V_{7-18} = 7$ V	t_p	typ. 	4 μs 3,7 to 4,3 μs
Phase relation between middle of sync pulse at the input and the leading edge of the burst key pulse; $V_{7-18} = 7$ V	t	typ. 	2,65 μs 2,15 to 3,15 μs
Output trailing edge current	I_7	typ.	2 mA
Saturation voltage during line scan	V_{7-18}	⩽	1 V

* Permissible range 1 to 7 V.

Line flyback-blanking pulse (positive-going) (pin 7)

Output voltage	V_{7-18}	4,1 to 4,9	V
Output resistance	R_7	typ. 70	Ω
Output trailing edge current	I_7	typ. 2	mA

Field flyback/blanking pulse (pin 7)

Output voltage with externally forced in current I_7 = 2,4 to 3,6 mA	V_{7-18}	2 to 3	V
Output resistance at I_7 = 3 mA	R_7	typ. 70	Ω

TV-transmitter identification output (pin 9; open collector)

Output voltage at I_9 = 3 mA; no TV-transmitter	V_{9-18}	⩽ 0,5	V
Output resistance at I_9 = 3 mA; no TV-transmitter	R_9	⩽ 100	Ω
Output current at $V_{10-18} \geqslant 3$ V; TV-transmitter identified	I_9	⩽ 5	μA

TV-transmitter identification (pin 10)

When receiving a TV signal the voltage V_{10-18} will change from ⩽ 1 V to ⩾ 7 V.

Line drive pulse (positive-going)

Output voltage (peak-to-peak value)	$V_{3-18(p-p)}$	typ. 10	V
Output resistance			
for leading edge of line pulse	R_3	typ. 2,5	Ω
for trailing edge of line pulse	R_3	typ. 20	Ω
Pulse duration (transistor driving) V_{4-18} = 0 to 3,5 V; $-I_4 \geqslant 200$ μA; t_{fp} = 12 μs	t_p	$14 + t_d$	μs*
Supply voltage for switching off the output pulse	V_{1-18}	typ. 4	V

Overall phase relation

Phase relation between middle of sync pulse and the middle of the flyback pulse	Δt	typ. 2,6 ± 0,7	μs**

The adjustment of the overall phase relation and consequently the leading edge of the line drive pulse occurs automatically by phase control φ_2.

If additional adjustment is applied it can be arranged by current supply at pin 5, such that:

Supplying current	$\Delta I/\Delta t$	typ. 30	μA/μs

* t_d = switch-off delay of line output stage.

** Line flyback pulse duration t_{fp} = 12 μs.

Oscillator (pins 16 and 17)				
Threshold voltage low level	V_{16-18}	typ.	4,4	V
Threshold voltage high level	V_{16-18}	typ.	7,6	V
Charging current	$\pm I_{16}$	typ.	0,47	mA
Frequency; free running (C_{osc} = 4,7 nF; R_{osc} = 12 kΩ)	f_o	typ.	15,625	kHz
Spread of frequency	Δf_o	⩽	± 5	%▲
Frequency control sensitivity	$\Delta f_o/\Delta_{17}$	typ.	31	Hz/μA
Adjustment range of network in circuit (Fig. 1)	Δf_o	typ.	± 10	%
Influence of supply voltage on frequency; reference at V_S = 12 V	$\frac{\Delta f_o/f_o}{\Delta V/V_{nom}}$	⩽	± 0,05	%▲
Change of frequency when V_S drops to 5 V; reference at V_S = 12 V	Δf_o	⩽	± 10	%▲
Temperature coefficient of oscillator frequency	TC	⩽	$\pm 10^{-4}$	K^{-1}▲
Phase comparison $\varphi 1$ (pin 15)				
Control voltage range	V_{15-18}		4,1 to 7,9	V
Control current (peak value)	$\pm I_{15M}$		1,8 to 2,2	mA
Output leakage current at V_{15-18} = 4,3 to 7,7 V	I_{15}	⩽	1	μA
Output resistance				
at V_{15-18} = 4,3 to 7,7 V	R_{13}	high ohmic		*
at V_{15-18} ⩽ 4,1 V or ⩾ 7,9 V	R_{13}	low ohmic		**
Control sensitivity		typ.	2	kHz/μs
Catching and holding range (82 kΩ between pins 15 and 17)	Δf	typ.	± 680	Hz
Spread of catching and holding range	Δ(Δf)	typ.	± 12	%▲
Phase comparison $\varphi 2$ **and phase shifter** (pin 5)				
Control voltage range	V_{5-18}		5,4 to 7,6	V
Control current (peak value)	$\pm I_{5M}$	typ.	1	mA
Output resistance at V_{5-18} = 5,4 to 7,6 V	R_5	high ohmic		*
Input leakage current at V_{5-18} = 5,4 to 7,6 V	I_5	⩽	5	μA
Permissible delay between leading edge of output pulse and leading edge of flyback pulse (t_{fp} = 12 μs)	t_d	⩽	15,5	μs
Static control error	$\Delta t/\Delta t_d$	⩽	0,2	%
Coincidence detector $\varphi 3$ (pin 13)				
Output voltage	V_{13-18}		0,5 to 6	V
Output current (peak value)				
without coincidence	I_{13M}	typ.	0,1	mA
with coincidence	$-I_{13M}$	typ.	0,5	mA

* Current source.
** Emitter follower.
▲ Excluding external component tolerances.

Time constant switch (pin 14)

Output voltage	$V_{14\text{-}18}$	typ.	6 V
Output current (limited)	$\pm I_{14}$	typ.	1 mA
Output resistance			
at $V_{13\text{-}18}$ = 3,5 to 7 V	R_{14}	typ.	0,1 kΩ
at $V_{13\text{-}18} \leqslant 2{,}5$ V or $\geqslant 9$ V	R_{14}	typ.	60 kΩ

Internal keying pulse

Pulse duration	t_p	typ.	7,5 μs

HORIZONTAL COMBINATION

GENERAL DESCRIPTION

The TDA2595 is a monolithic integrated circuit intended for use in colour television receivers.

Features

- Positive video input; capacitively coupled (source impedance $< 200\ \Omega$)
- Adaptive sync separator; slicing level at 50% of sync amplitude
- Internal vertical pulse separator with double slope integrator
- Output stage for vertical sync pulse or composite sync depending on the load; both are switched off at muting
- φ_1 phase control between horizontal sync and oscillator
- Coincidence detector φ_3 for automatic time-constant switching; overruled by the VCR switch
- Time-constant switch between two external time-constants or loop-gain; both controlled by the coincidence detector φ_3
- φ_1 gating pulse controlled by coincidence detector φ_3
- Mute circuit depending on TV transmitter identification
- φ_2 phase control between line flyback and oscillator; the slicing levels for φ_2 control and horizontal blanking can be set separately
- Burst keying and horizontal blanking pulse generation, in combination with clamping of the vertical blanking pulse (three-level sandcastle)
- Horizontal drive output with constant duty cycle inhibited by the protection circuit or the supply voltage sensor
- Detector for too low supply voltage
- Protection circuit for switching off the horizontal drive output continuously if the input voltage is below 4 V or higher than 8 V
- Line flyback control causing the horizontal blanking level at the sandcastle output continuously in case of a missing flyback pulse
- Spot-suppressor controlled by the line flyback control

QUICK REFERENCE DATA

Supply voltage (pin 15)	$V_{15\text{-}5} = V_P$	typ.	12 V
Sync pulse amplitude (positive video)	$V_{i(p\text{-}p)}$	min.	50 mV
Horizontal output current	I_4	typ.	50 mA

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

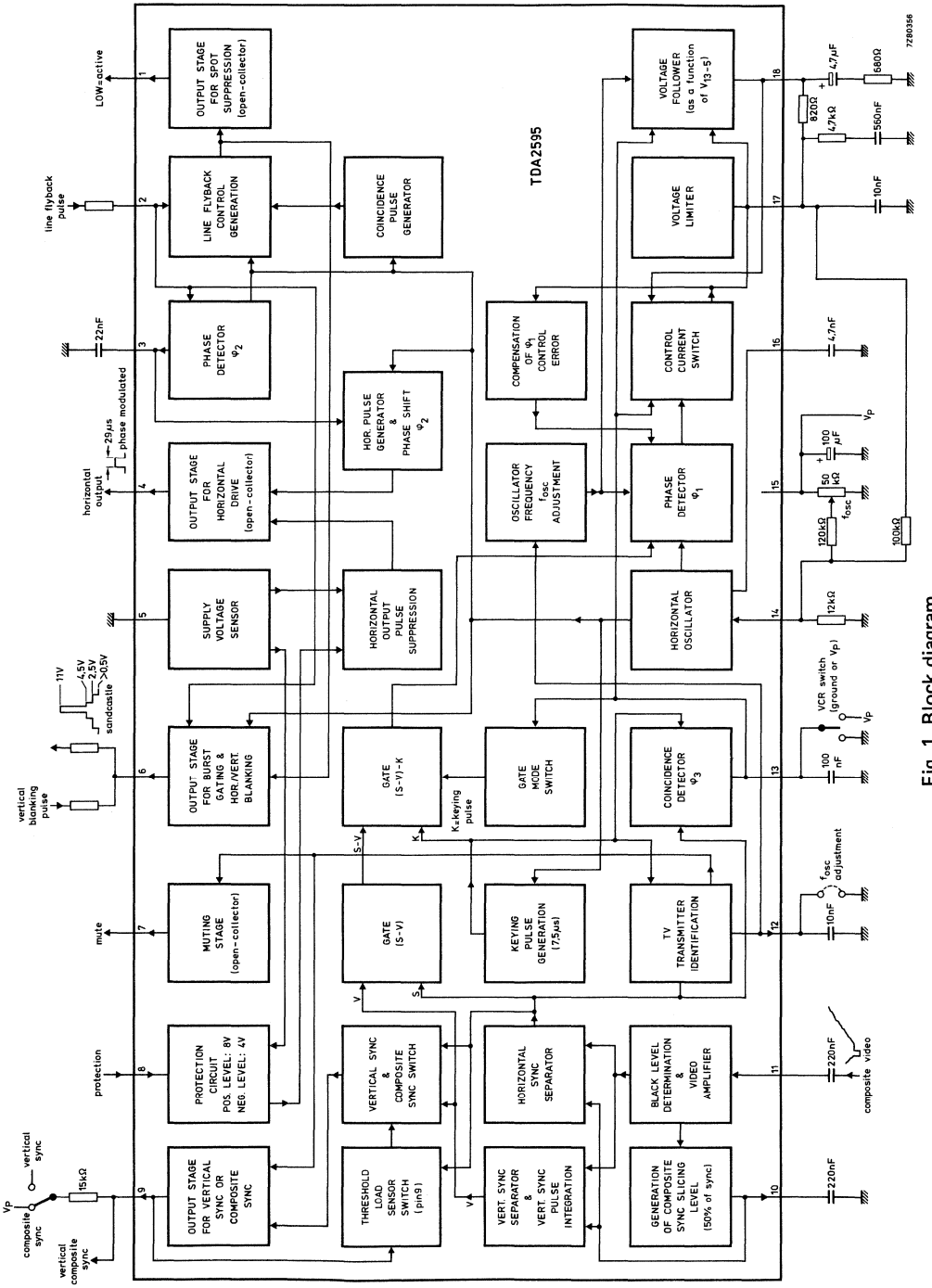


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 15)	$V_{15-5} = V_P$	max.	13,2	V
Voltages at:				
pins 1, 4 and 7	$V_{1;4;7-5}$	max.	18	V
pins 8, 13 and 18	$V_{8;13;18-5}$	max.	V_P	V
pin 11 (range)	V_{11-5}		−0,5 to + 6	V
Currents at:				
pin 1	I_1	max.	10	mA
pin 2 (peak value)	$\pm I_{2M}$	max.	10	mA
pin 4	I_4	max.	100	mA
pin 6 (peak value)	$\pm I_{6M}$	max.	6	mA
pin 7	I_7	max.	10	mA
pin 8 (range)	I_8		−5 to + 1	mA
pin 9 (range)	I_9		−10 to + 3	mA
pin 18	$\pm I_{18}$	max.	10	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature range	T_{stg}		−25 to + 125	°C
Operating ambient temperature range	T_{amb}		0 to + 70	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; measured in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Composite video input and sync separator (pin 11) (internal black level determination)					
Input signal (positive video; standard signal; peak-to-peak value)	$V_{11\text{-}5(p\text{-}p)}$	0,2	1	3	V
Sync pulse amplitude (independent of video content)	$V_{11\text{-}5(p\text{-}p)}$	50	–	–	mV
Generator resistance	R_G	–	–	200	Ω
Input current during:					
video	I_{11}	–	5	–	μA
sync pulse	$-I_{11}$	–	40	–	μA
black level	$-I_{11}$	–	25	–	μA
Composite sync generation (pin 10) horizontal slicing level at 50% of the sync pulse amplitude for $V_{11\text{-}5(p\text{-}p)} < 1{,}5$ V					
Capacitor current during:					
video	I_{10}	–	16	–	μA
sync pulse	$-I_{10}$	–	170	–	μA
Vertical sync pulse generation slicing level at 30% (60% between black level and horizontal slicing level); pin 9					
Output voltage	$V_{9\text{-}5}$	10	–	–	V
Pulse duration	t_p	–	190	–	μs
Delay with respect to the vertical sync pulse (leading edge)	t_d	–	45	–	μs
Pulse-mode control					
output current for vertical sync pulse (dual integrated)		no current applied at pin 9			
output current for horizontal and vertical sync pulse (non-integrated separated signal)		current applied via a resistor of 15 kΩ from V_P to pin 9			

parameter	symbol	min.	typ.	max.	unit
Horizontal oscillator (pins 14 and 16)					
Frequency; free running	f_{osc}	–	15 625	–	Hz
Reference voltage for f_{osc}	V_{14-5}	–	6	–	V
Frequency control sensitivity	$\Delta f_{osc}/\Delta I_{14}$	–	31	–	Hz/μA
Adjustment range of circuit Fig. 1	Δf_{osc}	–	± 10	–	%
Spread of frequency	Δf_{osc}	–	–	5	%
Frequency dependency (excluding tolerance of external components)					
with supply voltage (V_P = 12 V)	$\frac{\Delta f_{osc}/f_{osc}}{\Delta V_{15-5}/V_{15-5}}$	–	± 0,05	–	
with supply voltage drop of 5 V	Δf_{osc}	–	–	10	%
with temperature	TC	–	–	$\pm 10^{-4}$	K^{-1}
Capacitor current during:					
discharging	$+I_{16}$	–	1024	–	μA
charging	$-I_{16}$	–	313	–	μA
Sawtooth voltage timing (pin 14)					
rise time	t_r	–	49	–	μs
fall time	t_f	–	15	–	μs
Horizontal output pulse (pin 4)					
Output voltage LOW at I_4 = 50 mA	V_{4-5}	–	–	0,5	V
Pulse duration (HIGH)	t_p	–	29 ± 1,5	–	μs
Supply voltage for switching off the output pulse (pin 15)	V_P	–	4	–	V
Hysteresis for switching on the output pulse	ΔV_P	–	250	–	mV

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Phase comparison φ_1 (pin 17)					
Control voltage range	$V_{17\text{-}5}$	3,55	–	8,3	V
Leakage current at $V_{17\text{-}5}$ = 3,55 to 8,3 V	I_{17}	–	–	1	μA
Control current for external time-constant switch	$\pm I_{17}$	1,8	2	2,2	mA
Control current at $V_{18\text{-}5} = V_{15\text{-}5}$ and $V_{13\text{-}5} < 2$ V or $V_{13\text{-}5} > 9{,}5$ V	$\pm I_{17}$	–	8	–	mA
Control current at $V_{18\text{-}5} = V_{15\text{-}5}$ and $V_{13\text{-}5}$ = 2 to 9,5 V	$\pm I_{17}$	1,8	2	2,2	mA
Horizontal oscillator control					
control sensitivity	S_φ	6	–	–	kHz/μs
catching and holding range	$\pm\Delta f_{osc}$	–	680	–	Hz
spread of catching and holding range	$\pm\Delta f_{osc}$	–	10	–	%
Internal keying pulse at $V_{13\text{-}5}$ = 2,9 to 9,5 V	t_p	–	7,5	–	μs
Time-constant switch					
slow time-constant at	$V_{13\text{-}5}$	9,5	–	2	V
fast time-constant at	$V_{13\text{-}5}$	2	–	9,5	V
Impedance converter offset voltage (slow time-constant)	$\pm V_{17\text{-}18}$	–	–	3	mV
Output resistance					
slow time-constant	$R_{18\text{-}5}$	–	–	10	Ω
fast time-constant	$R_{18\text{-}5}$	high impedance			
Leakage current	I_{18}	–	–	1	μA

parameter	symbol	min.	typ.	max.	unit
Coincidence detector φ_3 (pin 13)					
Output voltage					
without coincidence with composite video signal	V_{13-5}	–	–	1	V
without coincidence without composite video signal (noise)	V_{13-5}	–	–	2	V
with coincidence with composite video signal	V_{13-5}	–	6	–	V
Output current					
without coincidence with composite video signal	I_{13}	–	50	–	μA
with coincidence with composite video signal	$-I_{13}$	–	300	–	μA
Switching current					
at $V_{13-5} = V_P - 0{,}5$ V	I_{13}	–	–	100	μA
at $V_{13-5} = 0{,}5$ V (average value)	$I_{13(av)}$	–	–	100	μA
Phase comparison φ_2 (pins 2 and 3) (see note 1)					
Input for line flyback pulse (pin 2)					
Switching level for φ_2 comparison and flyback control	V_{2-5}	–	3	–	V
Switching level for horizontal blanking	V_{2-5}	–	0,3	–	V
Input voltage limiting	V_{2-5}	–	–0,7	–	V
	or:	–	+4,5	–	V
Switching current					
at horizontal flyback	I_2	0,01	1	–	mA
at horizontal scan	I_2	–	–	2	μA
Maximum negative input current	$-I_2$	–	–	500	μA
Phase detector output (pin 3)					
Control current for φ_2	$\pm I_3$	–	1	–	mA
Control range	$\Delta t_{\varphi 2}$	–	19	–	μs
Static control error	$\Delta t/\Delta t_d$	–	–	0,2	%
Leakage current	I_3	–	–	5	μA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Phase comparison φ_2 (pins 2 and 3) (continued)					
Phase relation between middle of the horizontal sync pulse and the middle of the line flyback pulse at t_{fp} = 12 μs (note 2)	Δt	–	2,6 ± 0,7	–	μs
If additional adjustment is required, it can be arranged by applying a current at pin 3	$\Delta I/\Delta t$	–	30	–	μA/μs
Burst gating pulse (pin 6) (note 3)					
Output voltage	V_{6-5}	10	11	–	V
Pulse duration	t_p	3,7	4	4,3	μs
Phase relation between middle of sync pulse at the input and the leading edge of the burst gating pulse at V_{6-5} = 7 V	$t_{\varphi 6}$	2,15	2,65	3,15	μs
Output trailing edge current	I_6	–	2	–	mA
Horizontal blanking pulse (pin 6) (note 3)					
Output voltage	V_{6-5}	4,1	4,5	4,9	V
Output trailing edge current	I_6	–	2	–	mA
Saturation voltage at horizontal scan	V_{6-5sat}	–	–	0,5	V
Clamping circuit for vertical blanking pulse (pin 6) (note 3)					
Output voltage at I_6 = 2,8 mA	V_{6-5}	2,15	2,5	3	V
Minimum output current at $V_{6-5} > 2,15$ V	I_{6min}	–	2,3	–	mA
Maximum output current at $V_{6-5} < 3$ V	I_{6max}	–	3,3	–	mA
TV-transmitter identification (pin 12) (note 4)					
Output voltage					
no TV transmitter	V_{12-5}	–	–	1	V
TV transmitter identified	V_{12-5}	7	–	–	V

parameter	symbol	min.	typ.	max.	unit
Mute output (pin 7)					
Output voltage at I_7 = 3 mA no TV transmitter	V_{7-5}	–	–	0,5	V
Output resistance at I_7 = 3 mA no TV transmitter	R_{7-5}	–	–	100	Ω
Output leakage current at $V_{12-5} > 3$ V TV transmitter identified	I_7	–	–	5	μA
Protection circuit (beam-current/ EHT voltage protection) (pin 8)					
No-load voltage for $I_8 = 0$ (operative condition)	V_{8-5}	–	6	–	V
Threshold at positive-going voltage	V_{8-5}	–	8 ± 0,8	–	V
Threshold at negative-going voltage	V_{8-5}	–	4 ± 0,4	–	V
Current limiting for V_{8-5} = 1 to 8,5 V	$\pm I_8$	–	60	–	μA
Input resistance for $V_{8-5} > 8,5$ V	R_{8-5}	–	3	–	kΩ
Internal response delay of threshold switch	t_d	–	10	–	μs
Control output of line flyback pulse control (pin 1)					
Saturation voltage at standard operation; I_1 = 3 mA	V_{1-5sat}	–	–	0,5	V
Output leakage current in case of disturbance of line flyback pulse	I_1	–	–	5	μA

Notes to the characteristics

1. Phase comparison between horizontal oscillator and the line flyback pulse. Generation of a phase modulated (φ_2) horizontal output pulse with constant duration.
2. t_{fp} is the line flyback pulse duration.
3. Three-level sandcastle pulse.
4. If pin 12 is connected to V_P the vertical output is active independent of synchronization state.

5 W AUDIO POWER AMPLIFIER

The TDA2611A is a monolithic integrated circuit in a 9-lead single in-line (SIL) plastic package with a high supply voltage audio amplifier. Special features are:

- **possibility for increasing the input impedance**
- single in-line (SIL) construction for easy mounting
- very suitable for application in mains-fed apparatus
- extremely low number of external components
- thermal protection
- well defined open loop gain circuitry with simple quiescent current setting and fixed integrated closed loop gain

QUICK REFERENCE DATA

Supply voltage range	V_P		6 to 35 V
Repetitive peak output current	I_{ORM}	<	1,5 A
Output power at d_{tot} = 10%			
V_P = 18 V; R_L = 8 Ω	P_o	typ.	4,5 W
V_P = 25 V; R_L = 15 Ω	P_o	typ.	5 W
Total harmonic distortion at P_o < 2 W; R_L = 8 Ω	d_{tot}	typ.	0,3 %
Input impedance	$\|Z_i\|$	typ.	45 kΩ
Total quiescent current at V_P = 18 V	I_{tot}	typ.	25 mA
Sensitivity for P_o = 2,5 W; R_L = 8 Ω	V_i	typ.	55 mV
Operating ambient temperature	T_{amb}		−25 to + 150 °C
Storage temperature	T_{stg}		−55 to + 150 °C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

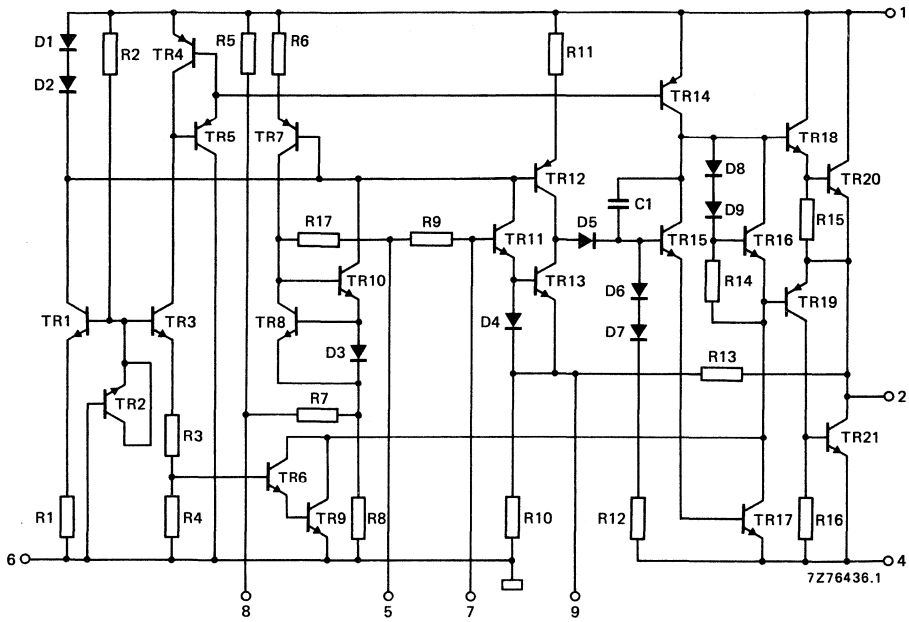


Fig. 1 Circuit diagram; pin 3 not connected.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	35 V
Non-repetitive peak output current	I_{OSM}	max.	3 A
Repetitive peak output current	I_{ORM}	max.	1,5 A
Total power dissipation	see derating curves Fig. 2		
Storage temperature	T_{stg}		−55 to + 150 °C
Operating ambient temperature	T_{amb}		−25 to + 150 °C

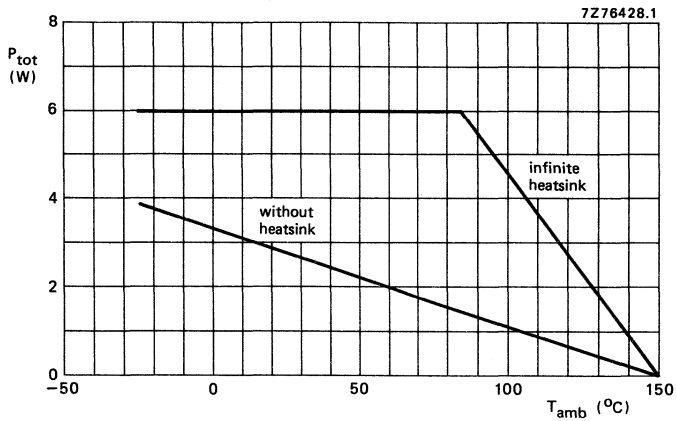


Fig. 2 Power derating curves.

HEATSINK EXAMPLE

Assume V_P = 18 V; R_L = 8 Ω; T_{amb} = 60 °C maximum; T_j = 150 °C (max. for a 4 W application into an 8 Ω load, the maximum dissipation is about 2,2 W).
The thermal resistance from junction to ambient can be expressed as:

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{150 - 60}{2,2} = 41\ K/W.$$

Since $R_{th\ j\text{-}tab}$ = 11 K/W and $R_{th\ tab\text{-}h}$ = 1 K/W, $R_{th\ h\text{-}a}$ = 41 − (11 + 1) = 29 K/W.

D.C. CHARACTERISTICS

Supply voltage range	V_P		6 to 35 V
Repetitive peak output current	I_{ORM}	<	1,5 A
Total quiescent current at V_P = 18 V	I_{tot}	typ.	25 mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 18 V; R_L = 8 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3

A.F. output power at d_{tot} = 10%			
V_P = 18 V; R_L = 8 Ω	P_o	>	4 W
		typ.	4,5 W
V_P = 12 V; R_L = 8 Ω	P_o	typ.	1,7 W
V_P = 8,3 V; R_L = 8 Ω	P_o	typ.	0,65 W
V_P = 20 V; R_L = 8 Ω	P_o	typ.	6 W
V_P = 25 V; R_L = 15 Ω	P_o	typ.	5 W
Total harmonic distortion at P_o = 2 W	d_{tot}	typ.	0,3 %
		<	1 %
Frequency response		>	15 kHz
Input impedance	$\|Z_i\|$	typ.	45 kΩ *
Noise output voltage at R_S = 5 kΩ; B = 60 Hz to 15 kHz	V_n	typ.	0,2 mV
		<	0,5 mV
Sensitivity for P_o = 2,5 W	V_i	typ.	55 mV
			44 to 66 mV

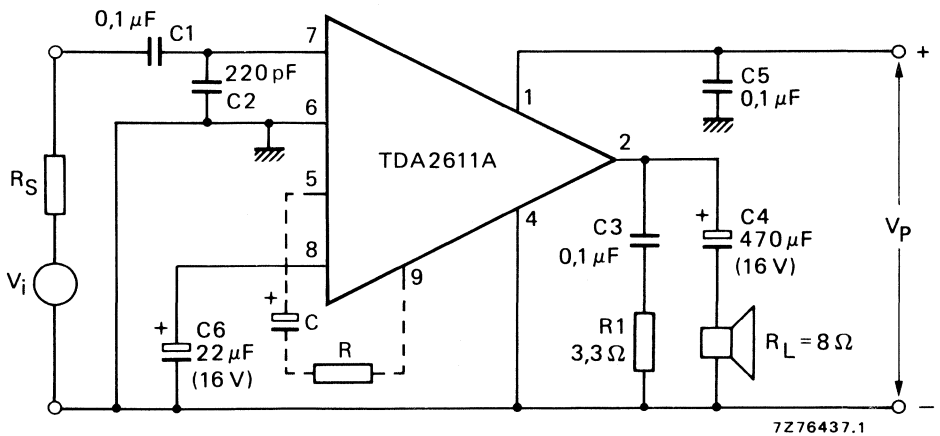


Fig. 3 Test circuit; pin 3 not connected.

* Input impedance can be increased by applying C and R between pins 5 and 9 (see also Figures 6 and 7).

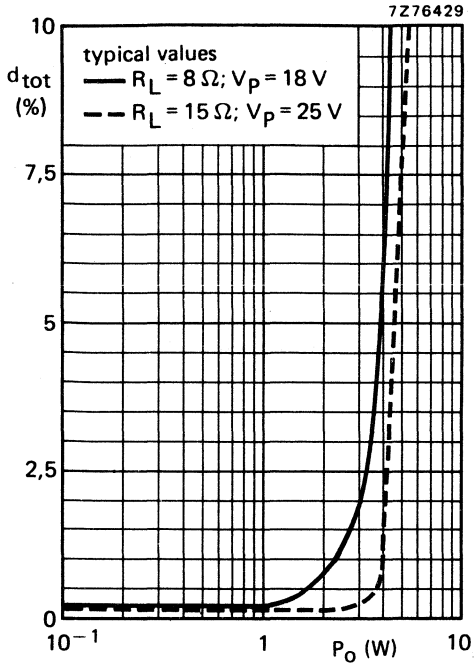


Fig. 4 Total harmonic distortion as a function of output power.

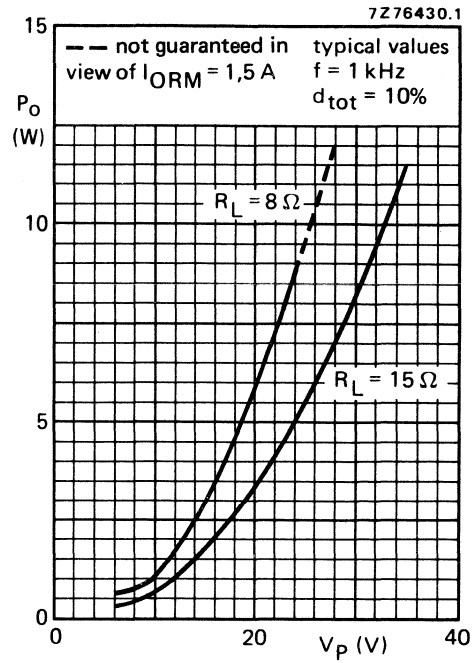


Fig. 5 Output power as a function of supply voltage.

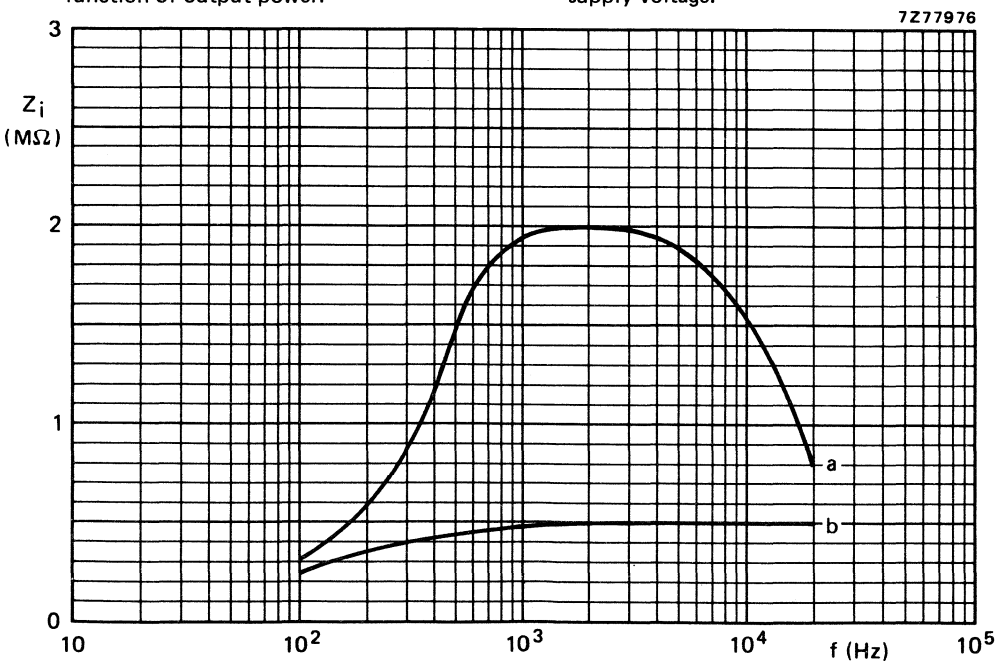


Fig. 6 Input impedance as a function of frequency; curve a for C = 1 μF, R = 0 Ω; curve b for C = 1 μF, R = 1 kΩ; circuit of Fig. 3; C2 = 10 pF; typical values.

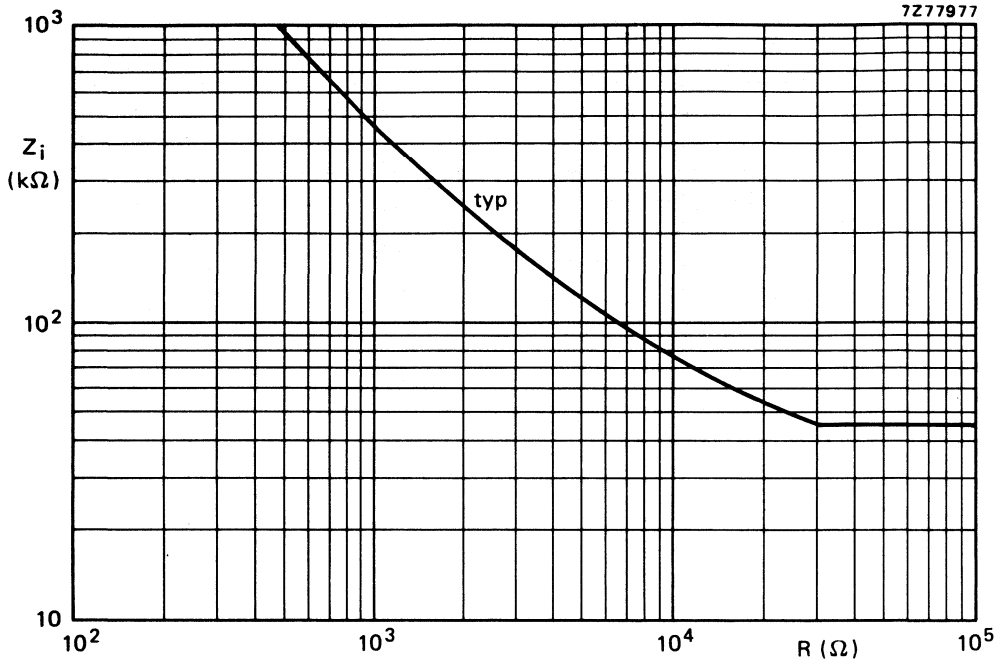


Fig. 7 Input impedance as a function of R in circuit of Fig. 3; C = 1 μF; f = 1 kHz.

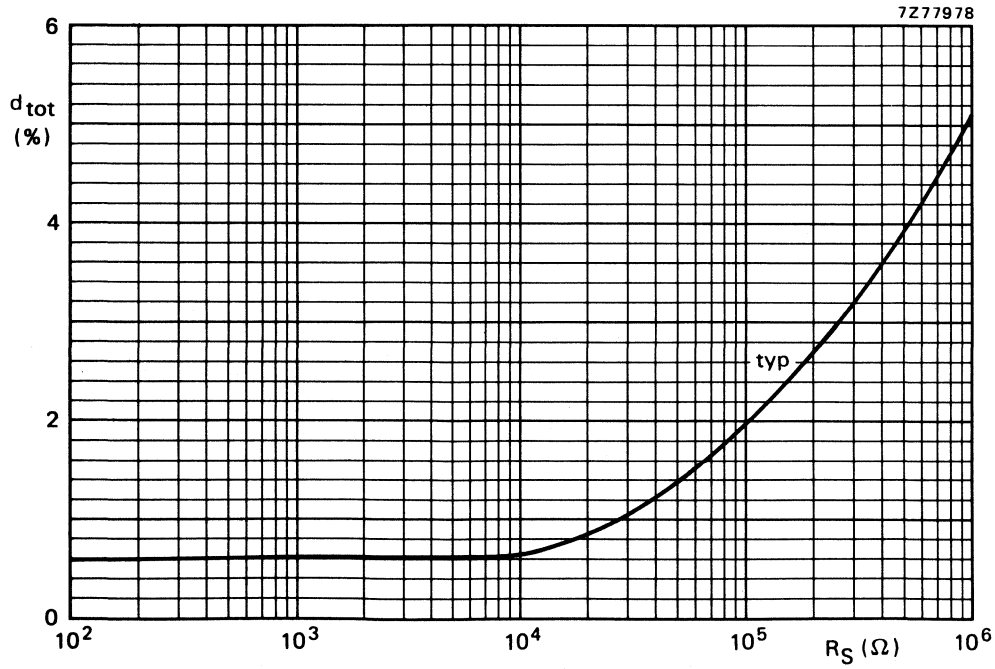


Fig. 8 Total harmonic distortion as a function of R_S in the circuit of Fig. 3; P_o = 3,5 W; f = 1 kHz.

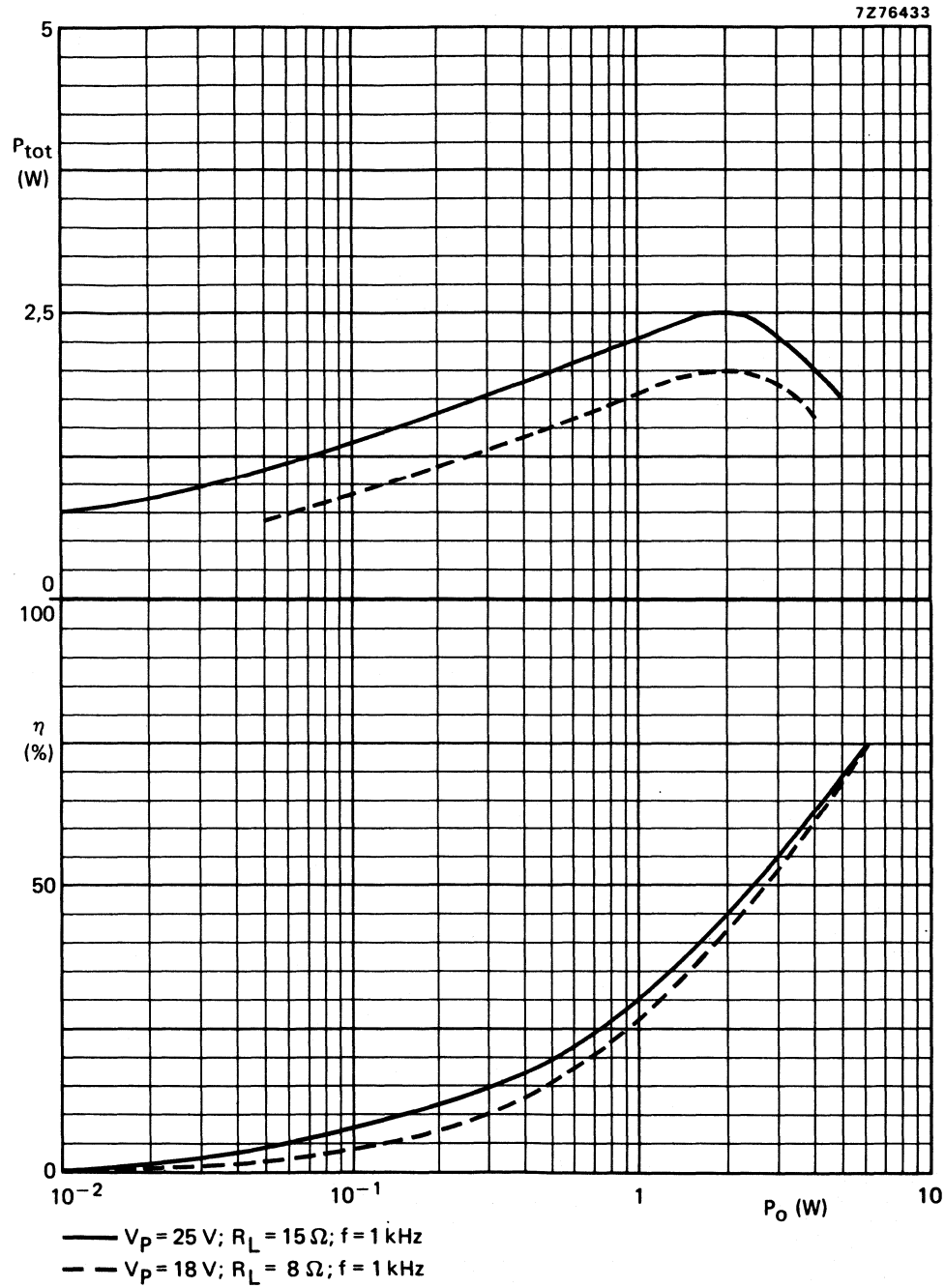


Fig. 9 Total power dissipation and efficiency as a function of output power.

APPLICATION INFORMATION

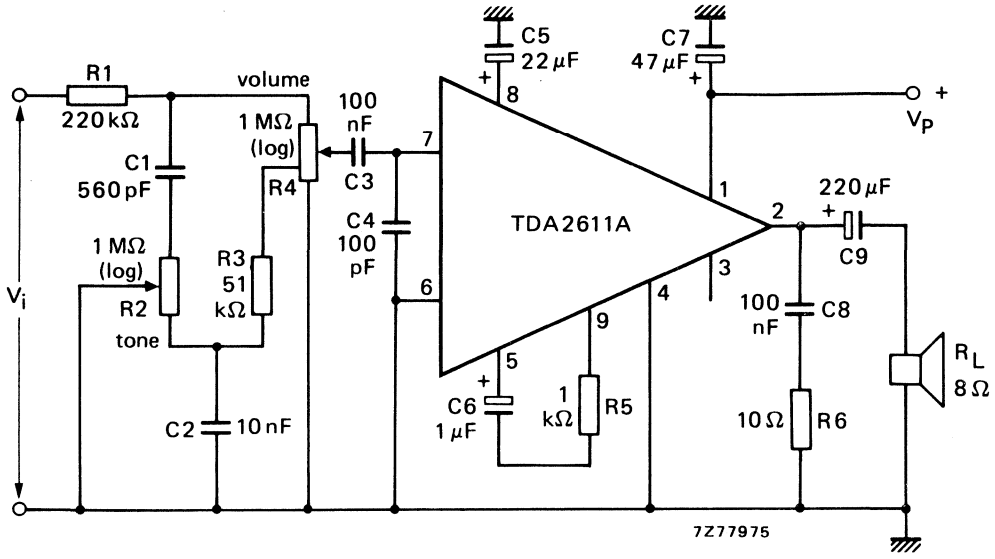


Fig. 10 Ceramic pickup amplifier circuit.

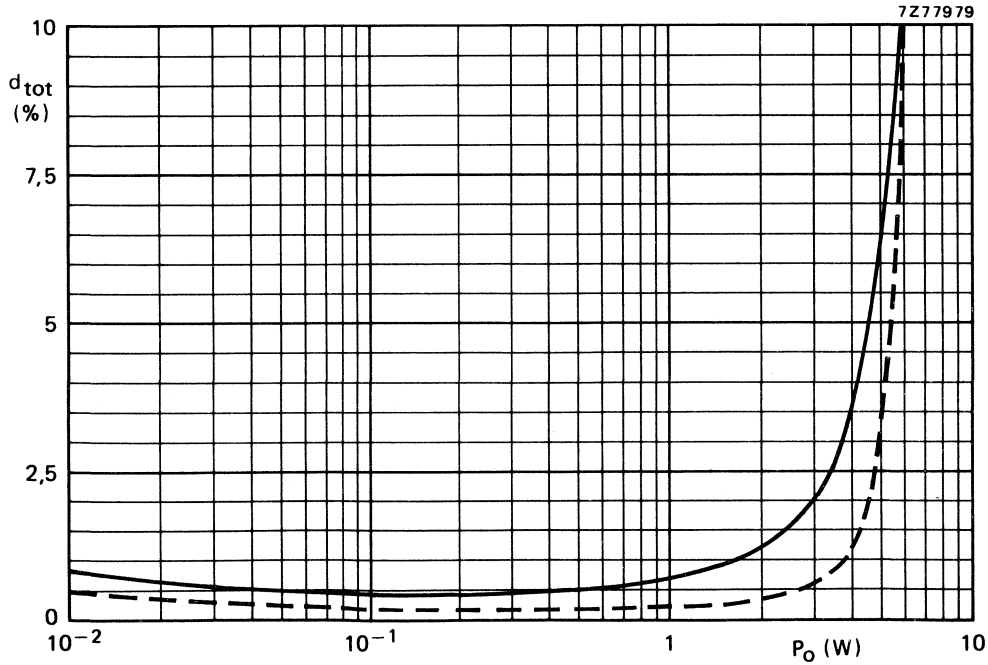


Fig. 11 Total harmonic distortion as a function of output power; —— with tone control; – – – without tone control; in circuit of Fig. 10; typical values.

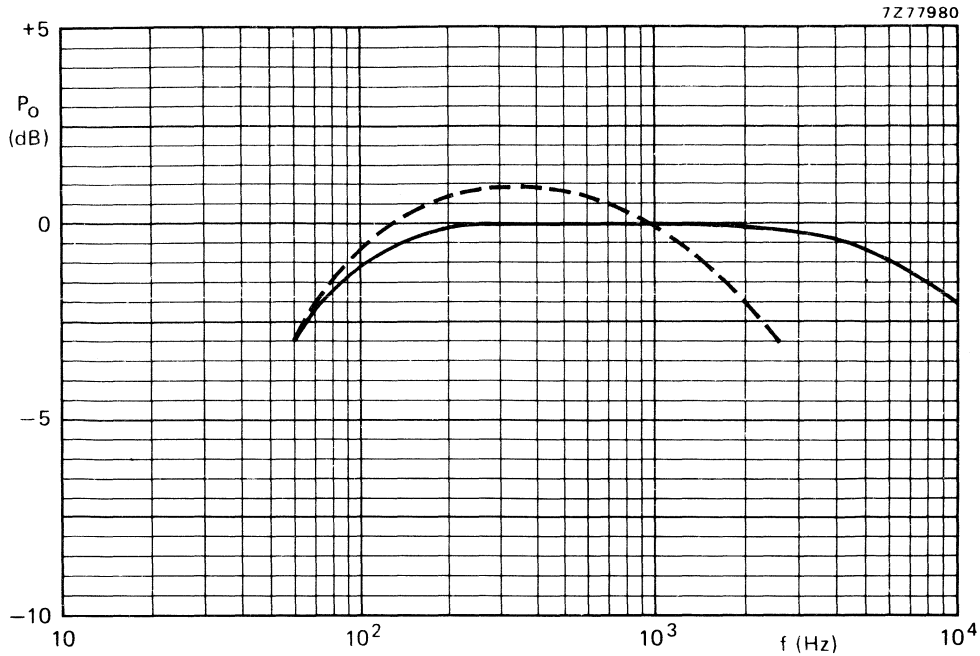


Fig. 12 Frequency characteristics of the circuit of Fig. 10; —— tone control max. high; – – – tone control min. high; P_o relative to 0 dB = 3 W; typical values.

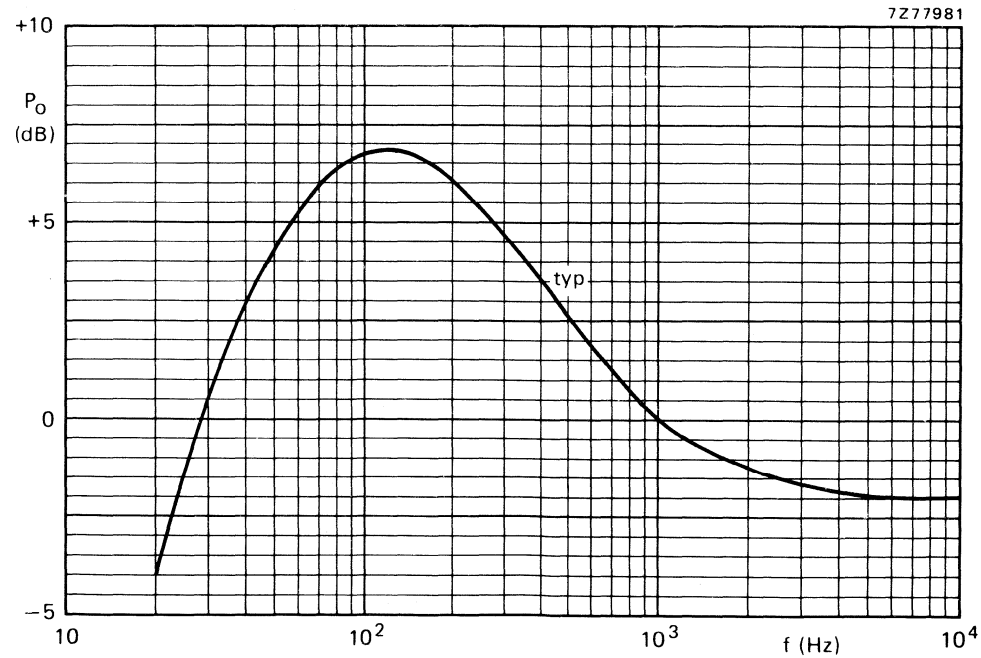


Fig. 13 Frequency characteristic of the circuit of Fig. 10; volume control at the top; tone control max. high.

6 W HI-FI AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA2613 is a hi-fi audio power amplifier encapsulated in a 9-lead SIL plastic power package. The device is especially designed for mains fed applications (e.g. tv and radio).

Features

- Requires very few external components
- Input muted during power-on and off (no switch-on or switch-off clicks)
- Low offset voltage between output and ground
- Hi-fi according to IEC 268 and DIN 45500
- Short-circuit-proof
- Thermally protected

QUICK REFERENCE DATA

Supply voltage range	V_P		15 to 40 V
Output power at THD = 0,5%, V_P = 24 V	P_O	typ.	6 W
Voltage gain	G_V	typ.	30 dB
Supply voltage ripple rejection	SVRR	typ.	60 dB
Noise output voltage	$V_{no(rms)}$	typ.	70 μV

PACKAGE OUTLINE

TDA2613: 9-lead SIL; plastic power (SOT110B).

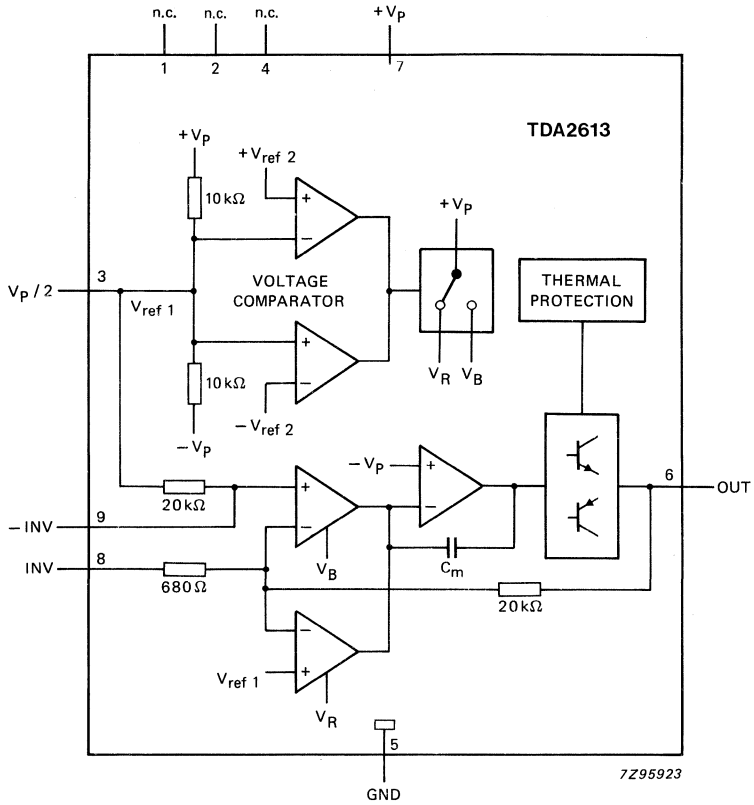


Fig. 1 Block diagram.

PINNING

1. n.c. not connected
2. n.c. not connected
3. $V_P/2$ ½ V_P (asymmetrical) / ground (symmetrical)
4. n.c. not connected
5. GND ground (asymmetrical) / negative supply (symmetrical)
6. OUT output
7. +Vp positive supply
8. INV inverting input
9. −INV non-inverting input

FUNCTIONAL DESCRIPTION

This hi-fi power amplifier is designed for mains fed applications. The device is intended for asymmetrical power supplies, but a symmetrical supply may also be used. An output power of 6 watts (THD = 0,5%) can be delivered into an 8 Ω load with an asymmetrical power supply of 24 V.

The gain is fixed internally at 30 dB. Internal gain fixing gives low gain spread.

A special feature of this device is a mute circuit which suppresses unwanted input signals during switching on and off. Referring to Fig. 4, the 100 μF capacitor creates a time delay when the voltage at pin 3 is lower than an internally fixed reference voltage. During the delay the amplifier remains in the DC operating mode but is isolated from the non-inverting input on pin 9.

Two thermal protection circuits are provided, one monitors the average junction temperature and the other the instantaneous temperature of the power transistors. Both protection circuits activate at 150 °C allowing safe operation to a maximum junction temperature of 150 °C without added distortion.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_P	–	40	V
Non-repetitive peak output current		I_{OSM}	–	4	A
Total power dissipation	see Fig. 2	P_{tot}			
Storage temperature range		T_{stg}	–65	+ 150	°C
Junction temperature		T_j	–	150	°C
Short-circuit time: outputs short-circuited to ground (full signal drive)	see note	t_{sc}	–	1	hour

Note to the Ratings

For asymmetrical power supplies (at short-circuiting of the load) the maximum supply voltage is limited to V_P = 28 V. If the total internal resistance of the supply (R_S) $\geqslant 4\ \Omega$, the maximum unloaded supply voltage is increased to 32 V. For symmetrical power supplies the circuit is short-circuit proof to $V_P = \pm 20$ V.

DEVELOPMENT DATA

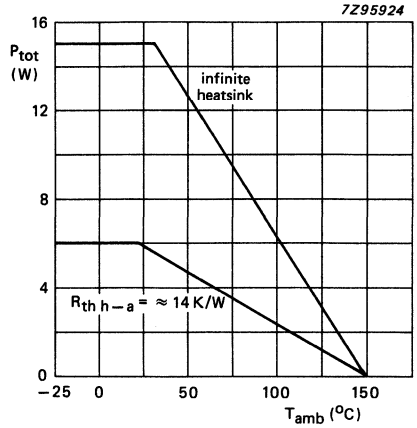


Fig. 2 Power derating curve.

THERMAL RESISTANCE

From junction to case $R_{th\ j\text{-}c} = 8$ K/W

HEATSINK DESIGN EXAMPLE

With derating of 8 K/W, the value of heatsink thermal resistance is calculated as follows:

given $R_L = 8\ \Omega$ and $V_P = 24$ V, the measured maximum dissipation is 4,1 W; then, for a maximum ambient temperature of 60 °C, the required thermal resistance of the heatsink is:

$$R_{th\ h\text{-}a} = \frac{150 - 60}{4{,}1} - 8 \approx 14\ \text{K/W}$$

Note: The metal tab (heatsink) has the same potential as pin 5 (GND).

DEVELOPMENT DATA

CHARACTERISTICS

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating mode		V_P	15	24	40	V
input mute mode		V_P	4	–	10	V
Repetitive peak output current		I_{ORM}	–	–	2,2	A
Operating mode: asymmetrical power supply; test circuit as per Fig. 4; V_P = 24 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current		I_{tot}	10	20	35	mA
Output power	THD = 0,5%	P_o	5	6	–	W
	THD = 10%	P_o	6,5	8,0	–	W
Total harmonic distortion	P_o = 4 W	THD	–	0,15	0,2	%
Power bandwidth	THD = 0,5%; note 1	B	–	20 to 16 k	–	Hz
Voltage gain		G_v	29	30	31	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\|Z_i\|$	14	20	26	kΩ
Supply voltage ripple rejection	note 2	SVRR	40	50	–	dB
Input bias current		I_{ib}	–	0,3	–	μA
DC output offset voltage	with respect to $V_P/2$	V_{os}	–	30	200	mV
Input mute mode: asymmetrical power supply; test circuit as per Fig. 4; V_P = 8 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current		I_{tot}	5	15	20	mA
Output voltage	V_i = 600 mV	V_{out}	–	0,6	1,8	mV
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Supply voltage ripple rejection	note 2	SVRR	35	55	–	dB
DC output offset voltage	with respect to $V_P/2$	V_{os}	–	40	200	mV

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Operating mode: symmetrical power supply; test circuit as per Fig. 3; $V_P = \pm 12$ V; $R_L = 8\ \Omega$; $T_{amb} = 25\ ^oC$; f = 1 kHz						
Total quiescent current		I_{tot}	10	20	35	mA
Output power	THD = 0,5%	P_o	5	6	–	W
	THD = 10%	P_o	6,5	8	–	W
Total harmonic distortion	$P_o = 4$ W	THD	–	0,13	0,2	%
Power bandwidth	THD = 0,5% note 1	B	–	40 to 16 k	–	Hz
Voltage gain		G_v	29	30	31	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	$R_S = 2\ k\Omega$	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\|Z_i\|$	14	20	26	kΩ
Supply voltage ripple rejection		SVRR	40	60	–	dB
DC output offset voltage	with respect to ground	V_{os}	–	30	200	mV

Notes to the characteristics

1. Power bandwidth at $P_{o\ max}$ –3 dB.
2. Ripple rejection at $R_S = 0\ \Omega$, f = 100 Hz to 20 kHz; ripple voltage = 200 mV (r.m.s. value) applied to positive or negative supply rail.

APPLICATION INFORMATION

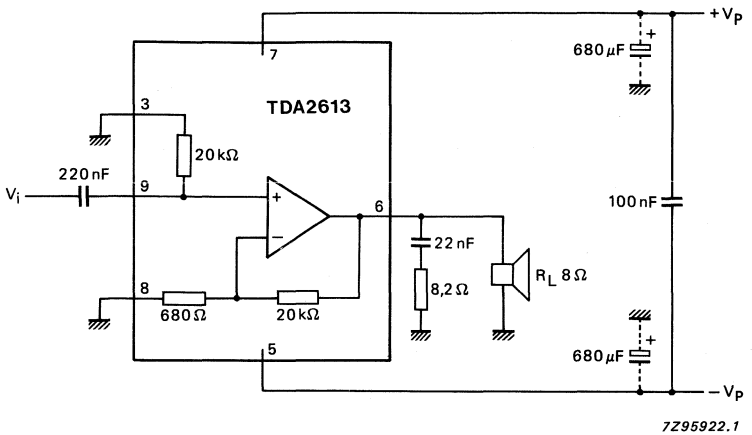


Fig. 3 Test and application circuit; symmetrical power supply.

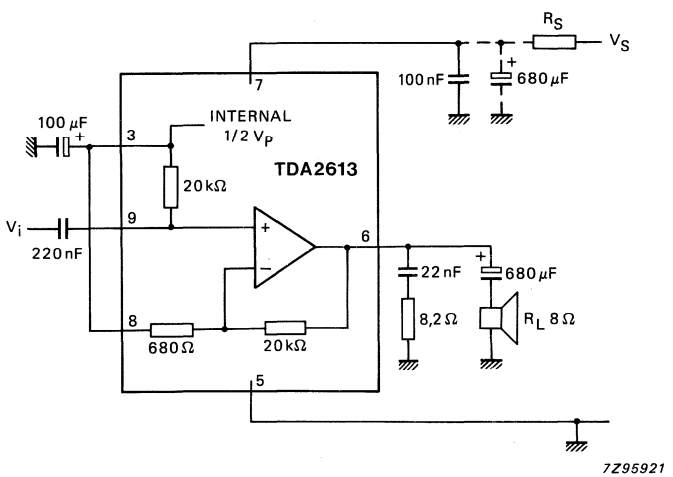


Fig. 4 Test and application circuit; asymmetrical power supply.

DEVELOPMENT DATA

APPLICATION INFORMATION (continued)

Input mute circuit

The input mute circuit operates only during switching on and off of the supply voltage. The circuit compares the ½ supply voltage (at pin 3) with an internally fixed reference voltage (V_{ref}), derived directly from the supply voltage. When the voltage at pin 3 is lower than V_{ref} the non-inverting input (pin 9) is disconnected from the amplifier. The voltage at pin 3 is determined by an internal voltage divider and the external 100 μF capacitor.
During switching on, a time delay is created between the reference voltage and the voltage at pin 3, during which the input terminal is disconnected, (as illustrated in Fig. 5).

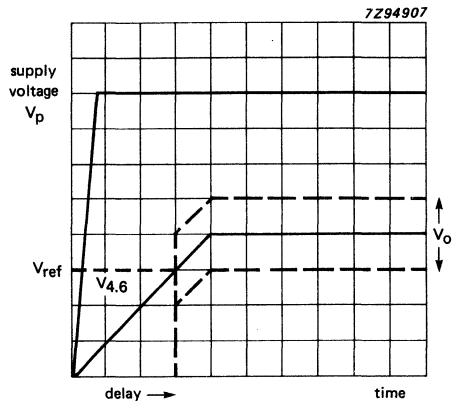


Fig. 5 Input mute circuit; time delay.

VERTICAL DEFLECTION CIRCUIT

The TDA2653A is a monolithic integrated circuit for vertical deflection in large screen colour television receivers, e.g. 30AX and PIL-S4 systems.

The circuit incorporates the following functions:

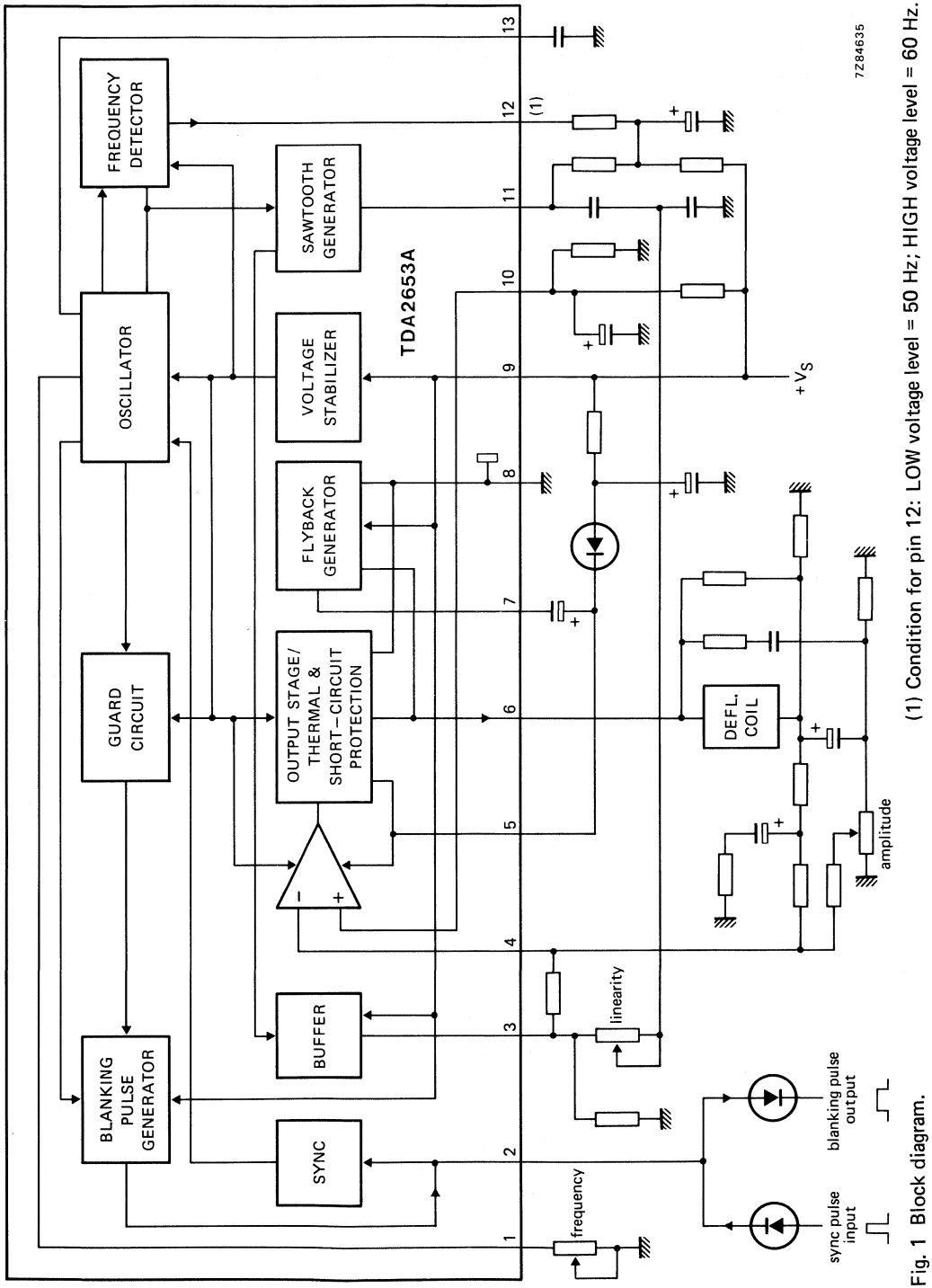
- Oscillator; switch capability for 50 Hz/60 Hz operation.
- Synchronization circuit.
- Blanking pulse generator with guard circuit.
- Sawtooth generator with buffer stage.
- Preamplifier with fed-out inputs.
- Output stage with thermal and short-circuit protection.
- Flyback generator.
- Voltage stabilizer.

QUICK REFERENCE DATA

For 30AX system			
Supply voltage (pin 9)	$V_{9\text{-}8} = V_S$	typ.	26 V
Supply current (pin 5 + pin 9)	$I_5 + I_9 = I_S$	typ.	325 mA
Output current (peak-to-peak value)	$I_{6(p\text{-}p)}$	typ.	2,2 A
Picture frequency	f		50 Hz/60 Hz
Sync input pulse (peak-to-peak value)	$V_{2\text{-}8(p\text{-}p)}$	$\geqslant$	1 V
Thermal resistance from junction to mounting base	$R_{th\ j\text{-}mb}$	$\leqslant$	5 K/W

PACKAGE OUTLINE

13-lead SIL; plastic power (SOT141B).



(1) Condition for pin 12: LOW voltage level = 50 Hz; HIGH voltage level = 60 Hz.

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 9)	$V_{9-8} = V_S$	max.	40 V
Supply voltage output stage (pin 5)	V_{5-8}	max.	58 V
Voltages			
Pin 3	V_{3-11}	max.	7 V
Pin 13	V_{13-8}	max.	7 V
Pins 4 and 10	$V_{4;10-8}$	max.	24 V
Pin 6	V_{6-8}	max.	58 V
	$-V_{6-8}$	max.	0 V
Pins 7 and 11	$V_{7;11-8}$	max.	40 V
Currents			
Pin 1	I_1	max.	0 mA
	$-I_1$	max.	1 mA
Pin 2	$\pm I_2$	max.	10 mA
Pin 3	I_3	max.	0 mA
	$-I_3$	max.	5 mA
Pin 7	I_7	max.	1,2 A
	$-I_7$	max.	1,5 A
Pin 11	I_{11}	max.	50 mA
	$-I_{11}$	max.	1 mA
Pin 12	I_{12}	max.	3 mA
	$-I_{12}$	max.	0 mA

Pins 5, 6 and 8: internally limited by the short-circuit protection circuit.

Total power dissipation: internally limited by the thermal protection circuit.

Storage temperature range	T_{stg}	−25 to + 150 °C
Operating ambient temperature range	T_{amb}	0 °C to limiting value

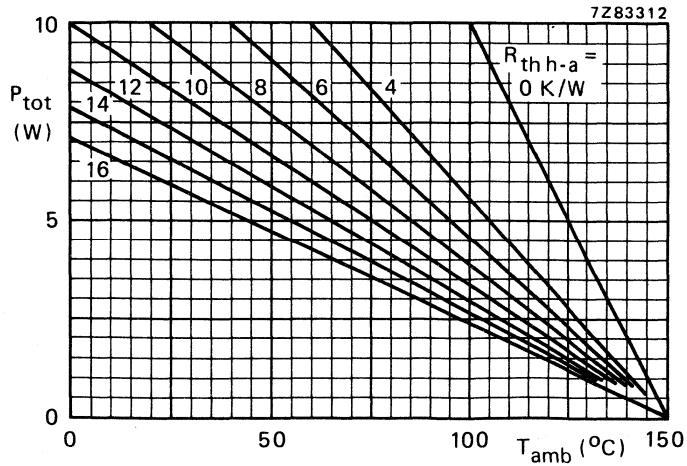


Fig. 2 Total power dissipation. $R_{th\ h\text{-}a}$ includes $R_{th\ mb\text{-}h}$ which is expected when heat-sink compound is used. $R_{th\ j\text{-}mb} \leqslant 5$ K/W.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

Supply voltage/output stage			
Supply voltage	$V_{9-8} = V_S$		9 to 30 V
Output voltage at $-I_6$ = 1,1 A	V_{6-8}	⩾ typ.	$V_{5-8} - 2,2$ V $V_{5-8} - 1,9$ V
at I_6 = 1,1 A	V_{6-8}	typ. ⩽	1,3 V 1,6 V
Flyback generator output voltage at $-I_6$ = 1,1 A	V_{7-8}	typ.	$V_S - 2,2$ V
Peak output current	$\pm I_6$	⩽	1,2 A
Flyback generator peak current	$\pm I_7$	⩽	1,2 A
Feedback			
Input quiescent current	$-I_{4;10}$	typ.	0,1 μA
Synchronization			
Sync input pulse	V_{2-8}		1 to 12 V
Tracking range		typ.	28 %
Oscillator/sawtooth generator			
Oscillator frequency control input voltage	V_{1-8}		6 to 9 V
Sawtooth generator output voltage	V_{3-8} V_{11-8}		0 to $V_S - 1$ V 0 to $V_S - 2$ V
Sawtooth generator output current	$-I_3$		0 to 4 mA
	I_{11}	⩾ ⩽	−2 μA +30 mA
Oscillator temperature dependency T_{case} = 20 to 100 °C	$(\Delta f/f)/\Delta T_{case}$	typ.	10^{-4} K^{-1}
Oscillator voltage dependency V_S = 10 to 30 V	$(\Delta f/f)/\Delta V_S$	typ.	4×10^{-4} V^{-1}
Blanking pulse generator			
Output voltage at V_S = 24 V; I_2 = 1 mA	V_{2-8}	typ.	18,5 V
Output current	$-I_2$	⩽	3 mA
Output resistance	R_{2-8}	typ.	410 Ω
Blanking pulse duration at 50 Hz sync	t_b	typ.	1,4 ± 0,07 ms
50 Hz/60 Hz switch capability			
Saturation voltage; LOW voltage level	V_{12-8}	typ.	1 V
Output leakage current	I_{12}	typ.	1 μA

Thermal resistance/junction temperature

From junction to mounting base	$R_{th\ j\text{-}mb}$	⩽	5 K/W
Junction temperature; switching point thermal protection	T_j	typ.	150 ± 8 °C

PINNING

1. Oscillator adjustment
2. Synchronization input/blanking output
3. Sawtooth generator output
4. Preamplifier input
5. Positive supply of output stage
6. Output
7. Flyback generator output
8. Ground
9. Positive supply (V_S)
10. Reference voltage
11. Sawtooth capacitor
12. 50 Hz/ 60 Hz switching voltage
13. Oscillator capacitor

APPLICATION INFORMATION

The function is described against the corresponding pin number

1, 13. Oscillator

The oscillator frequency is determined by a potentiometer at pin 1 and a capacitor at pin 13.

2. Sync input/blanking output

Combination of sync input and blanking output. The oscillator has to be synchronized by a positive-going pulse between 1 and 12 V. The integrated frequency detector delivers a switching level at pin 12.
The blanking pulse amplitude is 20 V with a load of 1 mA.

3. Sawtooth generator output

The sawtooth signal is fed via a buffer stage to pin 3. It delivers the signal which is used for linearity control, and drive of the preamplifier. The sawtooth is applied via a shaping network to pin 11 (linearity) and via a resistor to pin 4 (preamplifier).

4. Preamplifier input

The d.c. voltage is proportional to the output voltage (d.c. feedback). The a.c. voltage is proportional to the sum of the buffered sawtooth voltage at pin 3 and the voltage, with opposite polarity, at the feedback resistor (a.c. feedback).

5. Positive supply of output stage

This supply is obtained from the flyback generator. An electrolytic capacitor between pins 7 and 5, and a diode between pins 5 and 9 have to be connected for proper operation of the flyback generator.

6. Output of class-B power stage

The vertical deflection coil is connected to this pin, via a series connection of a coupling capacitor and a feedback resistor, to ground.

7. Flyback generator output

An electrolytic capacitor has to be connected between pins 7 and 5 to complete the flyback generator.

8. Negative supply (ground)

Negative supply of output stage and small signal part.

9. Positive supply

The supply voltage at this pin is used to supply the flyback generator, voltage stabilizer, blanking pulse generator and buffer stage.

APPLICATION INFORMATION (continued)

10. Reference voltage of preamplifier

    External adjustment and decoupling of reference voltage of the preamplifier.

11. Sawtooth capacitor

    This sawtooth capacitor has been split to realize linearity control.

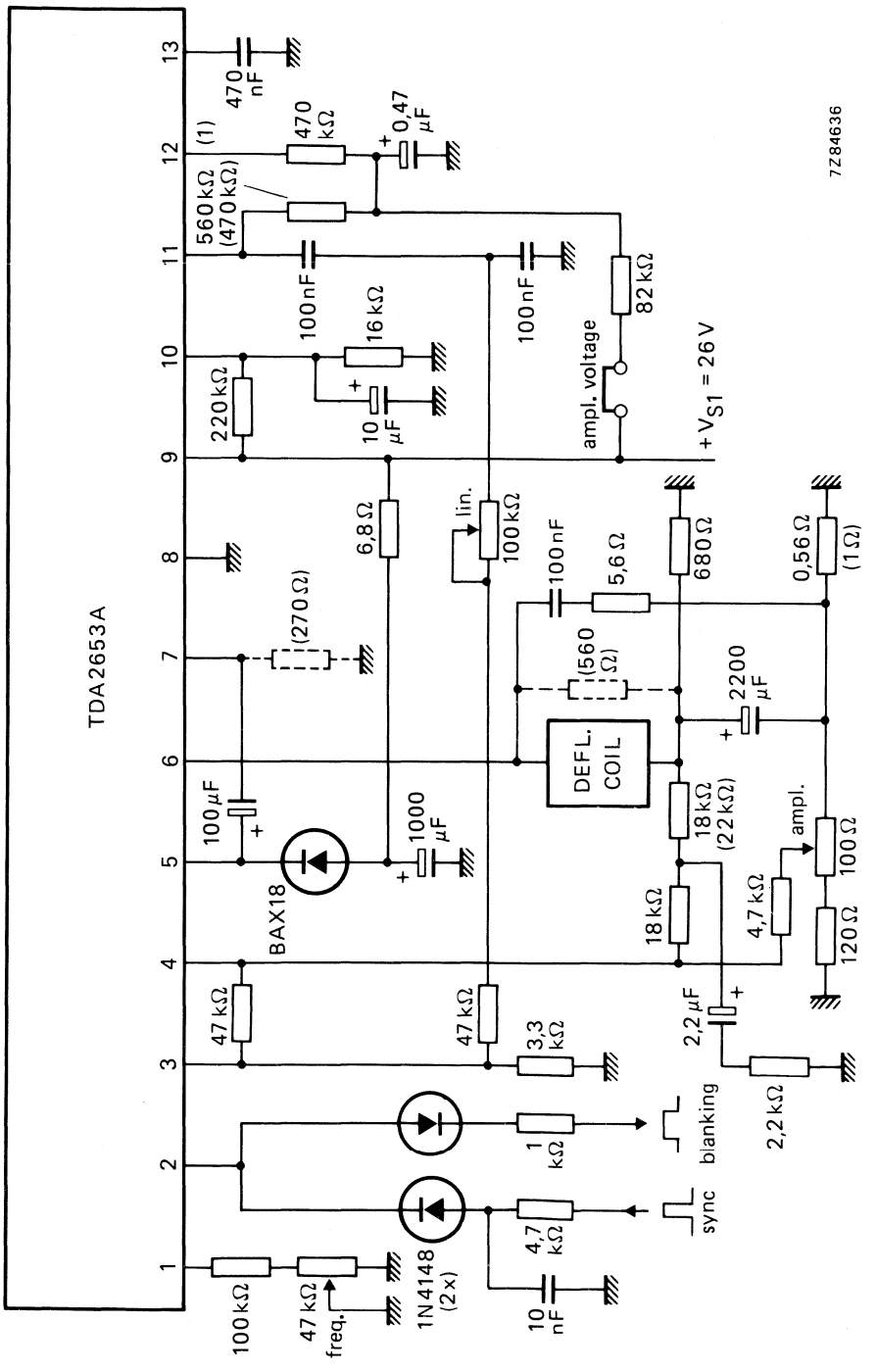
12. 50 Hz/60 Hz switching level

    This pin delivers a LOW voltage level for 50 Hz and a HIGH voltage level for 60 Hz. The amplitudes of the sawtooth signals can be made equal for 50 Hz and 60 Hz with these levels.

The following application data are measured in Figs 3 and 4.

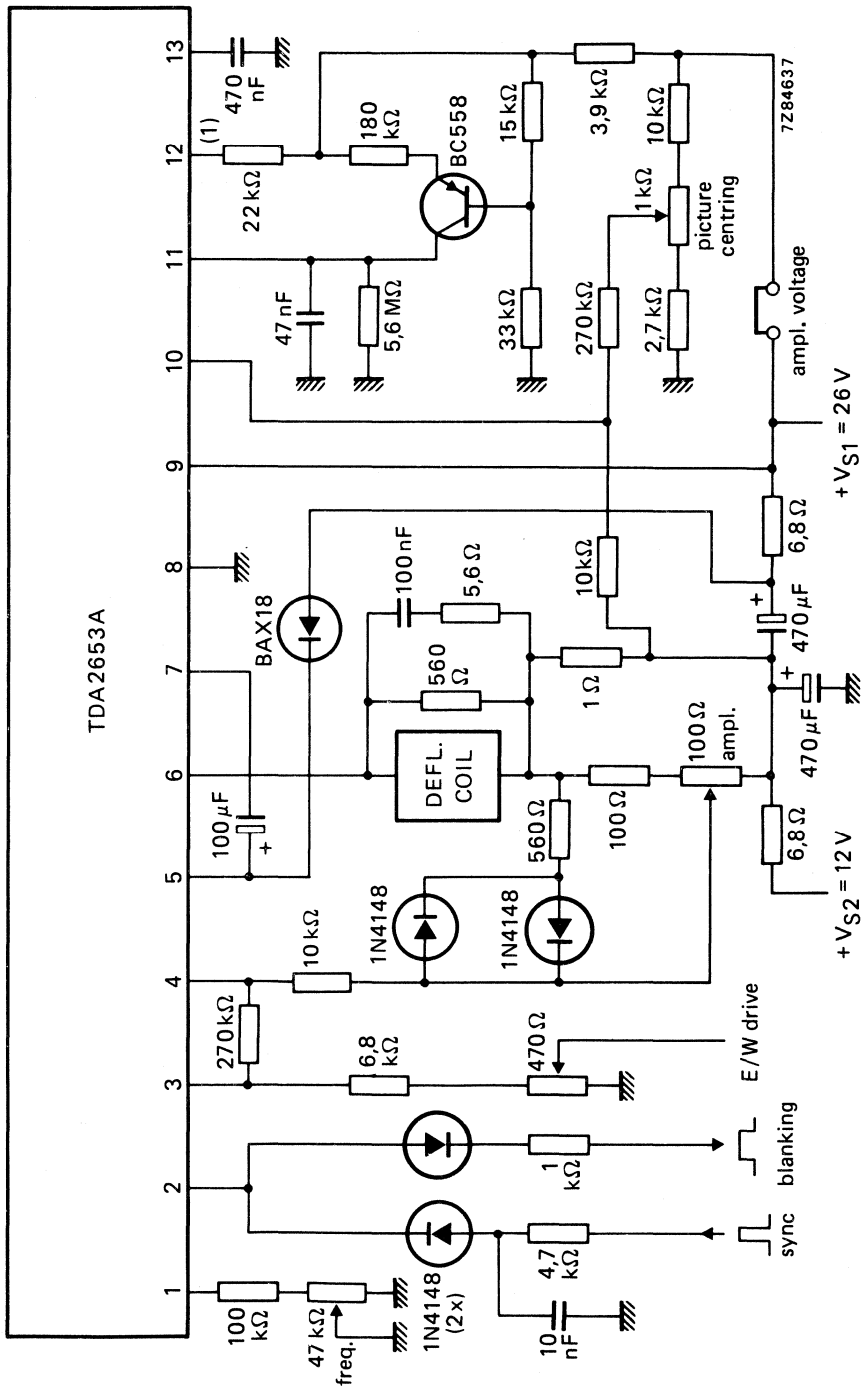
			30AX system (26 V) Fig. 3	30AX system (26 V/12 V) Fig. 4	PIL-S4 system Fig. 3
System supply voltages	V_{S1}	typ.	26	26	26 V
	V_{S2}	typ.	–	12	– V
System supply currents	I_{S1}	typ.	315	330	195 mA
	I_{S2}	typ.	–	–35	– mA
Output voltage	$V_{6\text{-}8}$	typ.	14	14,6	13,5 V
Output voltage (peak value)	$V_{6\text{-}8}$	typ.	42	42	49 V
Deflection current (peak-to-peak value)	$I_{6(p\text{-}p)}$	typ.	2,2	2,2	1,32 A
Flyback time	t_{fl}	typ.	1	0,9	1,1 ms
Total power dissipation per package	P_{tot}	typ.	4,1	4	3 W
		max.	4,8	4,8	3,4 W*
Oscillator frequency unsynchronized	f	typ.	46,5	46,5	46,5 Hz

* Calculated with $\Delta V_S = +5\%$ and $\Delta R_{yoke} = -7\%$.



(1) Condition for pin 12: LOW voltage level = 50 Hz; HIGH voltage level = 60 Hz.

Fig. 3 Typical vertical deflection circuit for 30AX system (26 V). The values given in parentheses and the dotted components are valid for the PIL-S4 system.



(1) Condition for pin 12: LOW voltage level = 50 Hz; HIGH voltage level = 60 Hz.

Fig. 4 Typical vertical deflection circuit for 30AX system (V_{S1} = 26 V, V_{S2} = 12 V) in quasi-bridge connection.

VERTICAL DEFLECTION CIRCUIT

The TDA2654 is a monolithic integrated circuit for vertical deflection in monochrome and tiny-vision colour television receivers.

The circuit incorporates the following functions:

- Oscillator
- Synchronization circuit
- Blanking pulse generator
- Sawtooth generator
- S-correction and linearity circuit
- Comparator and drive circuit
- Output stage
- Flyback dissipation limiting circuit
- Supply for pre-stages via internal voltage divider
- Thermal protection circuit
- Controlled switch-on

QUICK REFERENCE DATA

Supply voltage range (ref. to tab = ground)	V_P		10 to 35	V
Output current (peak-to-peak value)	$I_{9(p-p)}$	max.	2	A
Total power dissipation	P_{tot}	max.	5	W
Operating junction temperature	T_j	max.	150	°C
Thermal resistance from junction to tab	$R_{th\ j\text{-}tab}$	=	12	°C/W

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

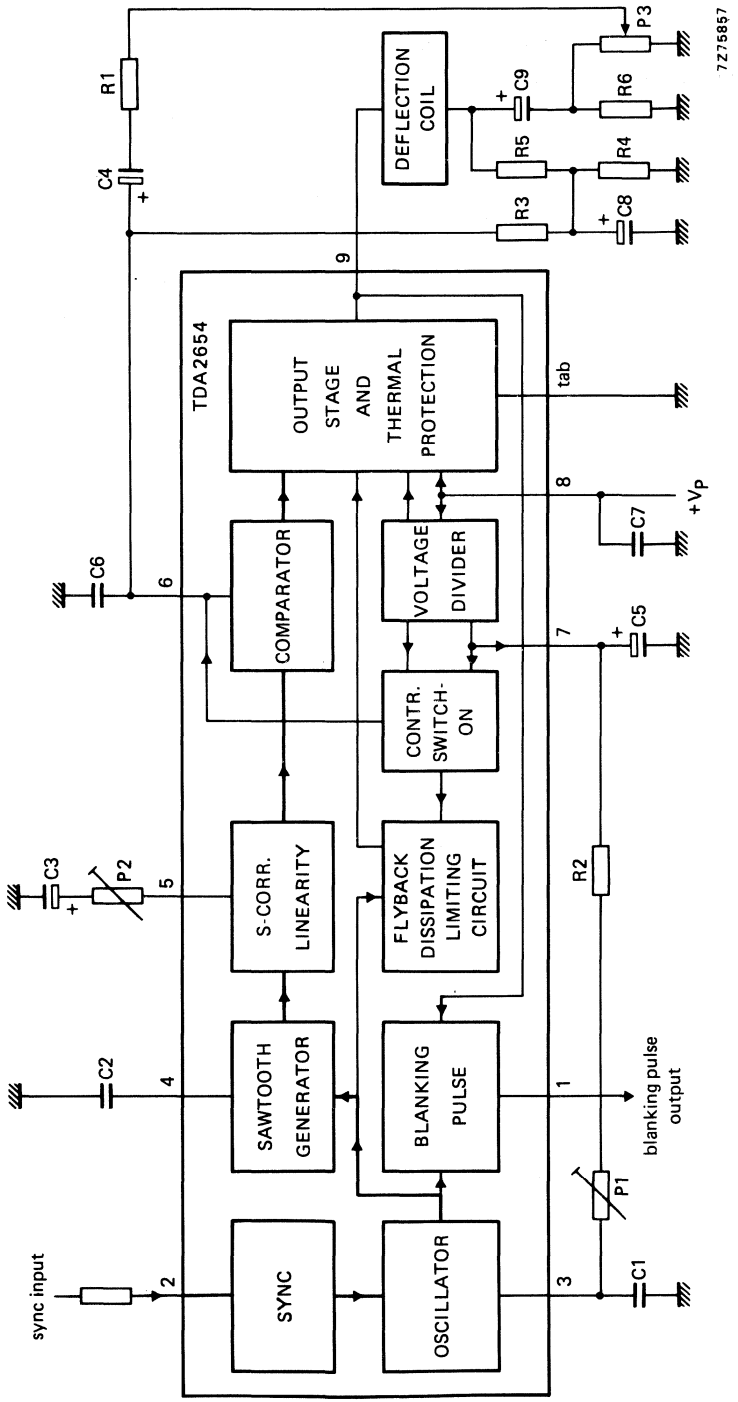


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

All voltages and currents refer to the tab (ground) connection.

Voltages			
Pin 2	V_2	max.	5 V
Pin 3	V_3	max.	17 V
Pin 4	V_4	max.	17 V
Pin 5	V_5	max.	6 V
Pin 6	V_6	max.	13 V
Pin 7	V_7	max.	18 V
Pin 8	V_8 (V_P)	max.	35 V
Currents			
Pin 1	$+I_1$	max.	1 mA
	$-I_1$	max.	5 mA
Pin 2	I_2	max.	2,5 mA
Pin 3	I_3	max.	30 mA
Pin 4	I_4	max.	30 mA
Pin 5	$\pm I_5$	max.	1 mA
Pin 6	$\pm I_6$	max.	3 mA
Pin 9 (repetitive)	$\pm I_9$	max.	1 A
Pin 9 (non-repetitive)	$\pm I_9$	max.	1,5 A
Total power dissipation (see also Fig. 2)	P_{tot}	max.	5 W
Storage temperature	T_{stg}	−25 to + 150	°C
Operating junction temperature	T_j	max.	150 °C

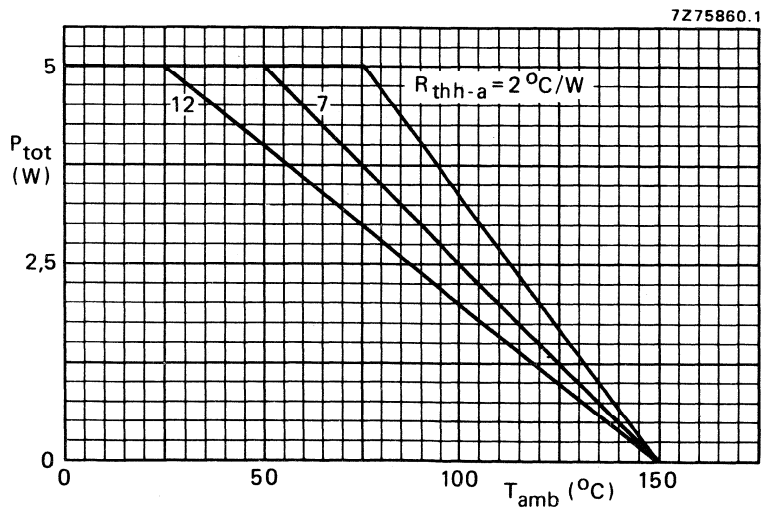


Fig. 2 Total power dissipation. The graph takes into account an $R_{th\ tab-h}$ = 1 °C/W which is to be expected when the tab is connected to a heatsink with one 3 mm bolt, without using heatsink compound. $R_{th\ j-tab}$ = 12 °C/W.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified; voltages and currents ref. to tab (ground)

			monochrome (Fig. 3)	tiny-vision colour (Fig. 4)	
Supply voltage (pin 8)	V_P	typ.	25	31	V
Supply current (pin 8)	I_P	typ.	165	150	mA
Total power dissipation	P_{tot}	typ.	3,1	3,5	W
Output voltage (peak-to-peak value)	$V_{9\,(p\text{-}p)}$	typ.	22	28	V
Blanking pulse; I_1 = 1 mA	V_1	typ.	11,5	14,5	V
Blanking pulse duration	t_p	typ.	1,3	1,4	ms
D.C. input voltage (pin 6)	V_6	typ.	3,4	4,4	V
Deflection current (peak-to-peak value)	$I_{9\,(p\text{-}p)}$	typ.	1,1	0,92	A
Flyback time	t	typ.	1,3	1,32	ms
Free running oscillator frequency	f_{osc}	typ.	46	46	Hz
Oscillator thermal drift		typ.	–0,01	–0,01	Hz/°C
Oscillator voltage shift		typ.	–0,13	–0,12	Hz/V
Tracking range oscillator		typ.	18	18	%
Synchronization input voltage	V_2	>	1	1	V
Voltage divider ratio	V_7/V_8	typ.	0,52	0,52	
Input resistance pin 7	R_7	typ.	2,8	2,8	kΩ
Recommended thermal resistance of heatsink for T_{amb} up to 70 °C	$R_{th\ h\text{-}a}$	<	13	10	°C/W

PINNING

1. Blanking pulse output
2. Synchronization input
3. Oscillator timing network
4. Sawtooth generator
5. S-correction and linearity control
6. Feedback input
7. Voltage divider
8. Positive supply
9. Output

Tab. Negative supply (ground)

APPLICATION INFORMATION (see also Fig. 1)

The function is described against the corresponding pin number

1. Blanking pulse output

When the IC is adjusted on a free running frequency of 46 Hz the internal blanking pulse generator delivers a blanking pulse with a duration between 1,2 ms and 1,5 ms. The circuit is, however, made such that when the flyback time of the deflection current is longer, the blanking pulse corresponds to the flyback time. The output voltage is also high when the voltage at pin 9 is lower than nominal 5 V. An external blanking circuit is recommended when tiny-vision receivers are operated from a car-battery.

2. Synchronization input

The oscillator has to be synchronized by a positive-going pulse. The circuit is made such that synchronization is inhibited during the flyback time.

APPLICATION INFORMATION (continued)

3. Oscillator

The oscillator frequency is set by the potentiometer P1 and resistor R2 between pins 3 and 7 and capacitor C1 between pin 3 and ground. For 50 Hz systems the free running frequency is preferably adjusted to 46 Hz.

4. Sawtooth generator

This pin supplies the charging and discharging currents of the capacitor between pin 4 and ground (C2).

5. S-correction and linearity control

The amount of S-correction can be set by the value of C3. For 110° deflection coils, e.g. AT1040/15, a capacitor of 15 μF will give the right value for S-correction. For 90° deflection systems (e.g. AT1235/00) a nearly linear deflection current is required, this can be achieved by increasing C3 to 100 μF. The linearity can be adjusted by potentiometer P2.

6. Output current feedback

To this pin is applied a part of the output current measured across R6 and superimposed on a d.c. voltage derived from the voltage across the output coupling capacitor. This signal is compared with the internal reference sawtooth. The internal reference sawtooth has an amplitude of about 0,6 V peak to peak and a d.c. level of about 3,4 V, for a supply voltage of 25 V at pin 8.

7. Internal voltage divider decoupling

The voltage on this pin is about half the supply voltage at pin 8 and is applied to the bases of emitter followers supplying the pre-stages of the IC. This voltage controls the amplitude of the internal reference sawtooth. In this way tracking with the line deflection system is achieved when the supply voltage at pin 8 is derived from the line output transformer.

8. Positive supply

The value depends on the deflection coil.

9. Output

The deflection coil is connected to ground via coupling capacitor C9 and current sensing resistor R6. The line frequency superimposed on the output voltage may be too high due to the current feedback system. The line frequency ripple can be decreased by connecting a resistor across the deflection coil. The flyback time can be influenced by the resistor divider (R4, R5) for the d.c. feedback to pin 6. It should be noted that the output voltage shows a negative swing of about 1 V during the first (positive current) part of the flyback.

Tab

The tab is used as negative supply (ground) connection. Therefore, the tab should be well connected to the negative side of the power supply.

Controlled switch-on

This feature is achieved by charging the a.c. coupling capacitor (C4; connected to pin 6) from an internal current source of about 2 mA (voltage limited to maximum 15 V) for a short period after switch-on. The charging time can be influenced by the value of C5 (connected to pin 7). Discharging of C4 results in a slowly increasing deflection current after a delay of about 1 second. The blanking voltage at pin 1 is high during this delay.

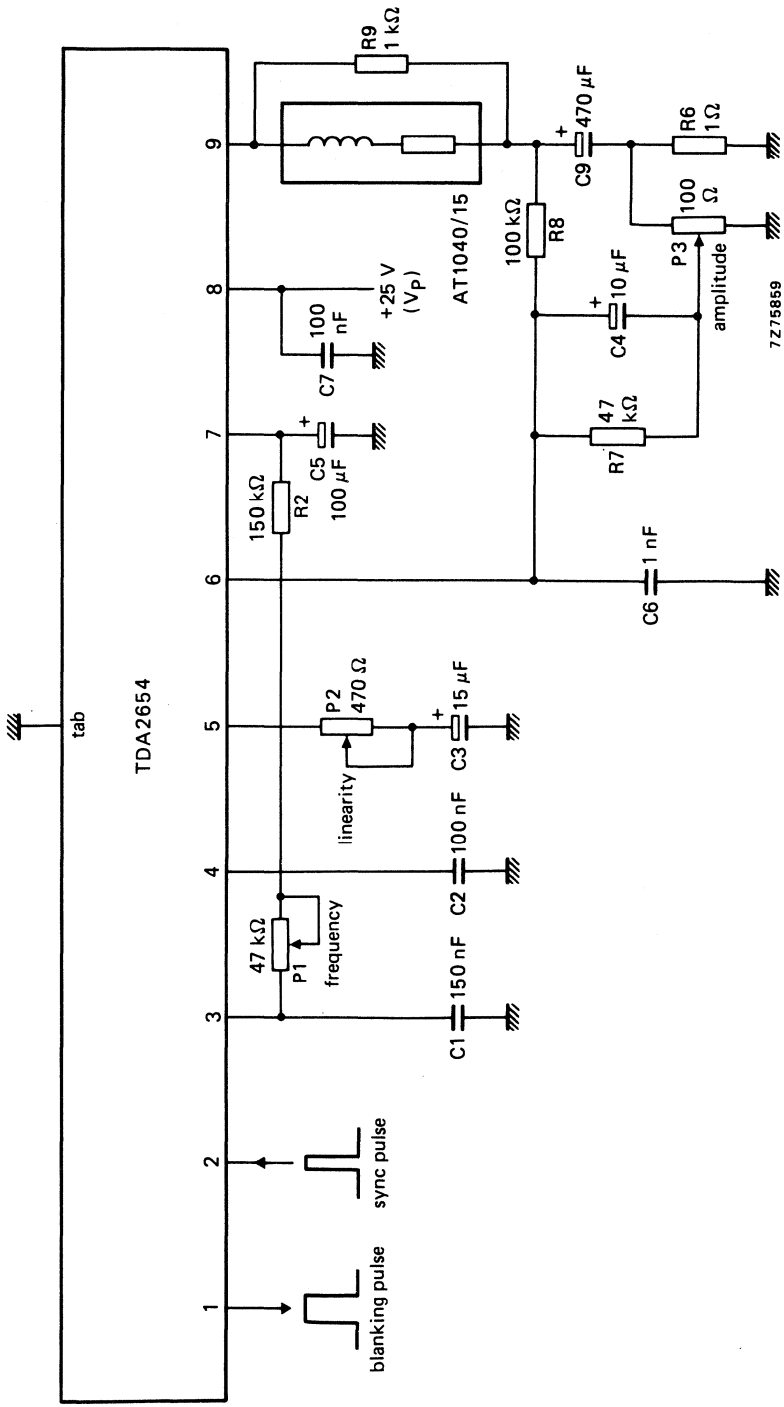


Fig. 3 Monochrome 110° vertical deflection system.

APPLICATION INFORMATION (continued)

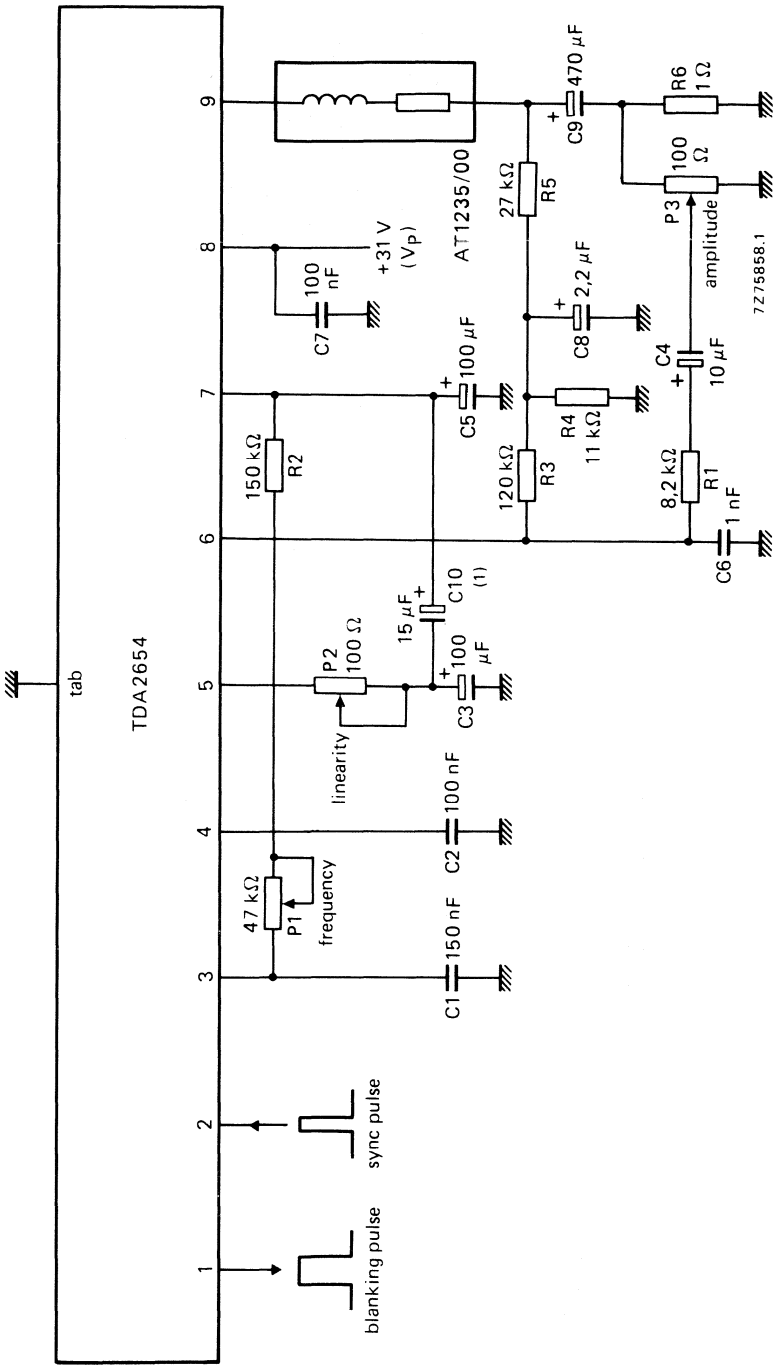


Fig. 4 Colour 90° vertical deflection system.

(1) Only required when rapid variations in the supply voltage are expected.

VERTICAL DEFLECTION CIRCUIT

GENERAL DESCRIPTION

The TDA2655B is a monolithic integrated circuit for vertical deflection in colour television receivers with 90° picture tubes.

Features

- Synchronization circuit
- Vertical oscillator; 50/60 Hz switch
- Sawtooth generator with buffer stage
- Preamplifier with fed-out inputs
- Output stage with termal and short-circuit protection
- Flyback generator
- Blanking pulse generator with guard circuit
- Voltage stabilizer
- Frequency detector with memory and storage

QUICK REFERENCE DATA

For 90° deflection; measured with respect to cooling fin (ground)

			concept 1*	concept 2*	
System supply voltages	V_{P1}	typ.	22	22	V
	V_{P2}	typ.	12	–	V
System supply currents	I_{P1}	typ.	135	140	mA
	$-I_{P2}$	typ.	8	–	mA
Deflection current (peak-to-peak value)	$I_{9(p-p)}$	typ.	450	450	mA
Synchronization input voltage (peak-to-peak value)	$V_{5(p-p)}$	min.	1	1	V

*Concept 1: with two supply voltages ; concept 2: with one supply voltage. (See also Figs 2 and 3).

PACKAGE OUTLINE

12-lead DIL; plastic with metal cooling fin (SOT150).

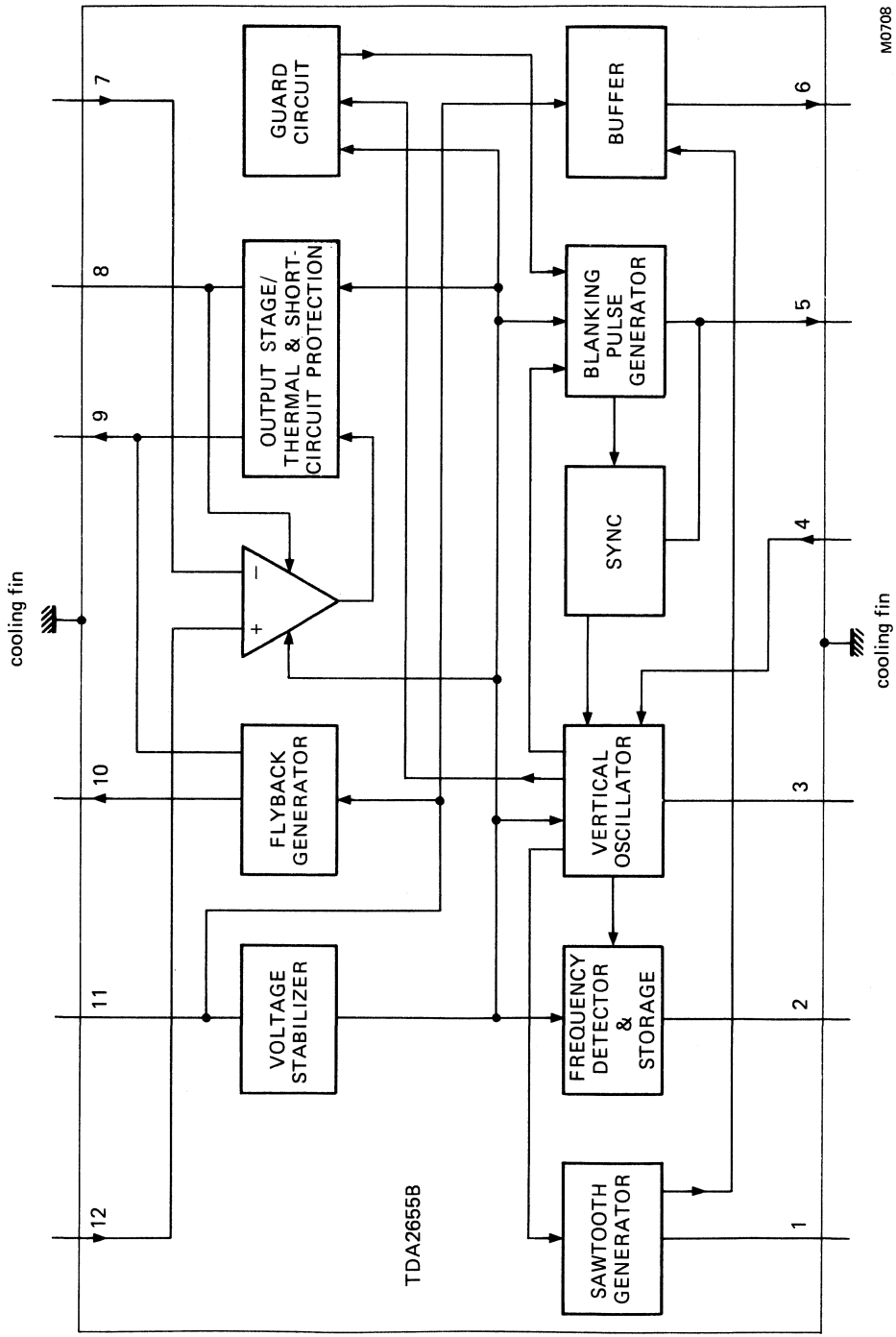


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

with respect to cooling fin (ground)

Supply voltage (pin 11)	$V_{11} = V_P$	max.	40	V
Supply voltage output stage (pin 8)	V_8	max.	60	V
Pin 9	V_9	max.	60	V
	$-V_9$	max.	0	V
Pin 10	V_{10}	max.	40	V
Pin 3	V_3	max.	7	V
Pin 1	V_1	max.	40	V
Pin 6	V_6	max.	7	V
Pins 7 and 12	$V_7; V_{12}$	max.	24	V

Currents

Pin 10	I_{10}	max.	1,2	A
	$-I_{10}$	max.	1,5	A
Pin 5	$\pm I_5$	max.	10	mA
Pin 2	I_2	max.	3	mA
Pin 1	I_1	max.	50	mA
	$-I_1$	max.	0,1	mA
Pin 6	$-I_6$	max.	5	mA
Pin 4	$-I_4$	max.	1	mA
Pin 8, pin 9 and cooling fin	internally limited by the short-circuit protection circuit			

Temperatures

Total power dissipation	internally limited by the short-circuit protection circuit	
Storage temperature range	T_{stg}	−55 to +150 °C
Operating ambient temperature range	T_{amb}	0 °C to limiting values

PINNING

pin number	function	pin number	function
1.	sawtooth capacitor	7.	feedback input
2.	frequency storage information	8.	positive supply of output stage
3.	oscillator capacitor	9.	output
4.	oscillator resistor (adjustment)	10.	flyback generator output
5.	synchronization input/blanking output	11.	positive supply (V_P)
6.	sawtooth buffer stage output	12.	preamplifier input

CHARACTERISTICS

V_P = 22 V; T_{amb} = 25 °C; these characteristics are measured with respect to cooling fin (ground), unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply voltage/output stage					
Supply voltage	$V_{11} = V_P$	9	–	30	V
Output voltage					
at I_9 = 0,75 A	V_9	–	1,2	1,4	V
at $-I_9$ = 0,75 A	V_9	$(V_P - 1,9)$	$(V_P - 1,7)$	–	V
Flyback generator output voltage at I_{10} = 0,75 A	V_{10}	–	$(V_P - 2,0)$	–	V
Supply currents (without load)					
pin 11	I_{11}	–	10	–	mA
pin 8	I_8	–	3	–	mA
Output current	$\pm I_9$	–	–	1,2	A
Flyback generator peak current	$\pm I_{10}$	–	–	1,2	A
Feedback					
Preamplifier quiescent input currents	$-I_7 = -I_{12}$	–	0,1	–	μA
Synchronization					
Sync input voltage range	V_5	1,0	–	–	V
Synchronizing range		–	28	–	%
Oscillator/sawtooth generator					
Frequency setting input voltage	V_4	6	–	9	V
Sawtooth generator output voltage (peak value)	$V_{1(m)}$	0	$(V_P - 2)$	–	V
Sawtooth generator output current	I_1	–	–	30	mA
Sawtooth generator leakage current	$-I_1$	2	–	–	μA
Oscillator temperature dependency T_{case} = 20 to 100 °C	$(\Delta f/f)/\Delta T_{case}$	–	10^{-4}	–	K^{-1}
Oscillator voltage dependency V_P = 10 to 30 V	$(\Delta f/f)/\Delta V_P$	–	10^{-3}	–	V^{-1}
Blanking pulse generator					
Output voltage (at I_5 = 1 mA)	V_5	–	20	–	V
Output resistance	R_5	–	410	–	Ω
Output current (at V_P = 21 V)	$-I_5$	–	–	5	mA
Blanking pulse duration at 50 Hz sync	t_b	1,33	1,4	1,47	ms
50/60 Hz frequency detector					
Output saturation voltage (LOW level for 50 Hz)	V_2	–	1	–	V
Leakage current	I_2	–	1	–	μA

parameter	symbol	min.	typ.	max.	unit
Buffer stage					
Output voltage	$V_{6(m)}$	0	$(V_P - 1)$	–	V
Output current	$-I_6$	–	–	4	mA
Thermal resistance					
From junction to case (cooling fin)	$R_{th\ j\text{-}c}$	–	–	15	K/W
Junction temperature					
Switching point thermal protection	T_j	142	150	158	°C

APPLICATION INFORMATION

The following application data is obtained from measurements made on the circuits shown in Figs 2 and 3, application circuits for 90° deflection systems. Measurements are made with respect to the cooling fin (ground).

			Fig. 2 concept 1*	Fig. 3 concept 2*	
System supply voltages	V_{P1}	typ.	22	22	V
	V_{P2}	typ.	12	–	V
Supply currents	I_{P1}	typ.	135	140	mA
	$-I_{P2}$	typ.	8	–	mA
Output voltage (d.c. value)	V_9	typ.	12,2	13,8	V
Output voltage (peak-to-peak value)	$V_{9(p\text{-}p)}$	typ.	42	43	V
Output current (peak value)	$-I_{9(m)}$	typ.	450	450	mA
Deflection current (peak-to-peak value)	$I_{defl\ (p\text{-}p)}$	typ.	850	850	mA
Flyback time	t_{fl}	typ.	0,9	1,0	ms
Oscillator frequency adjustment without sync	f_o	typ.	46,5	46,5	Hz
Total power dissipation per package (see note)	P_{tot}	max.	1,8	1,8	W
Ambient temperature	T_{amb}	max.	70	70	°C
Thermal resistance (junction to ambient)	$R_{th\ j\text{-}a}$	max.	40	40	K/W

*Concept 1 : with two supply voltages; concept 2 : with one supply voltage.

Note

Calculated with ΔV_{P1} of +5% and ΔR_{defl} of −7%.

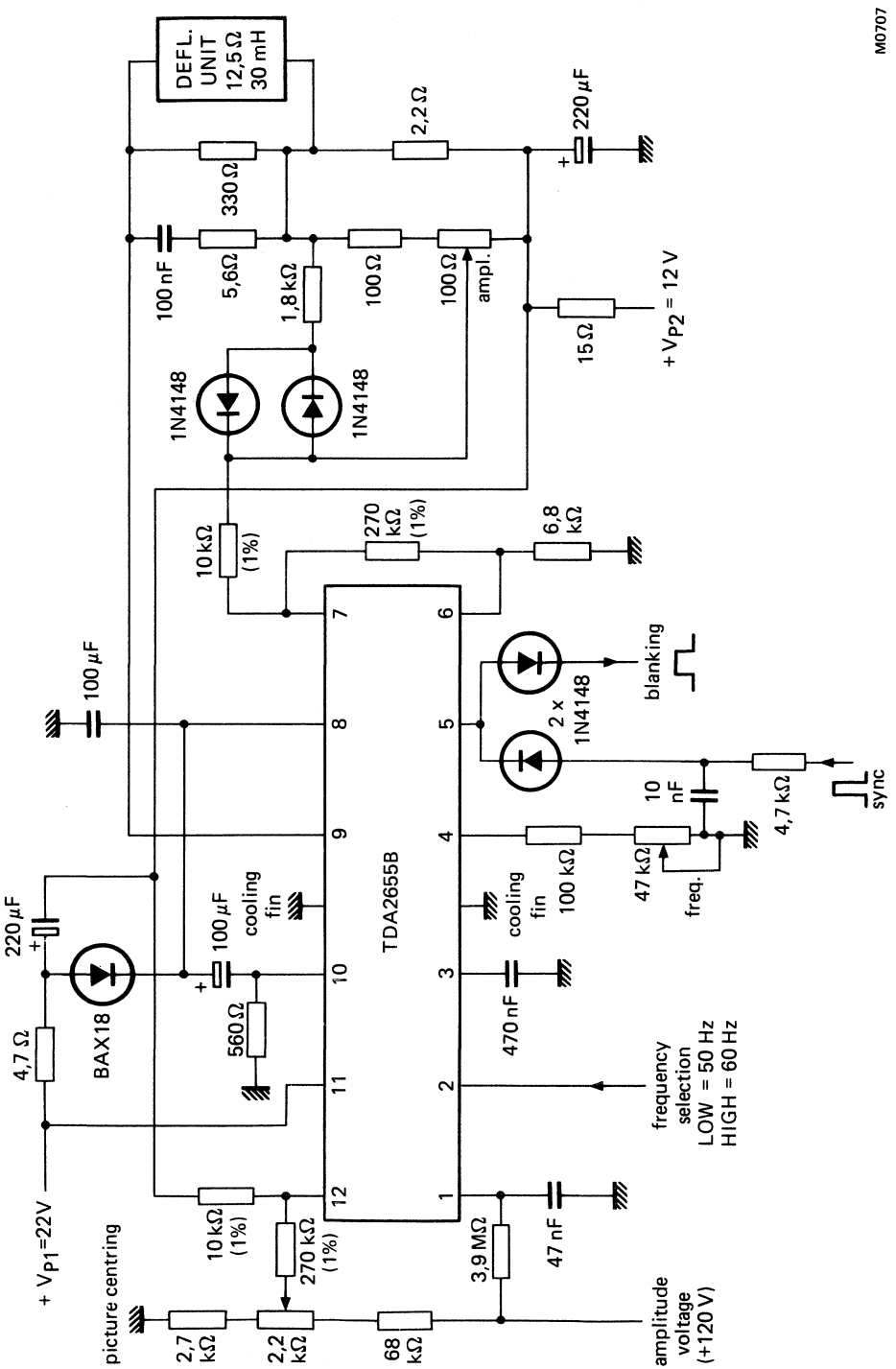


Fig. 2 Typical application circuit with two supply voltages; for use with 90° picture tubes.

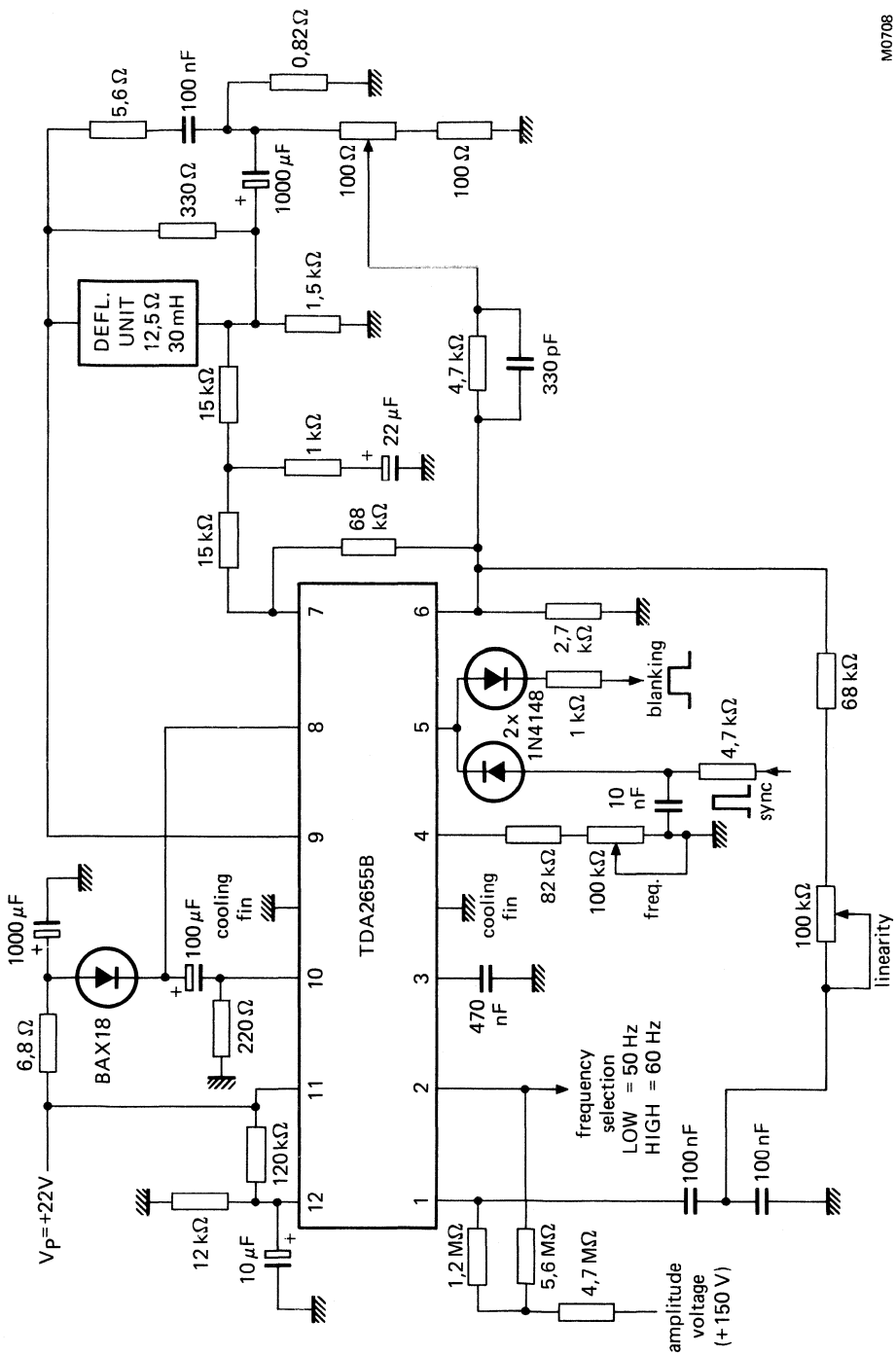


Fig. 3 Typical application circuit for a single supply voltage; for use with 90° picture tubes.

VERTICAL DEFLECTION CIRCUIT

The TDA2658 is a monolithic integrated circuit for vertical deflection in small screen colour television receivers and monitors.

The circuit incorporates the following functions:

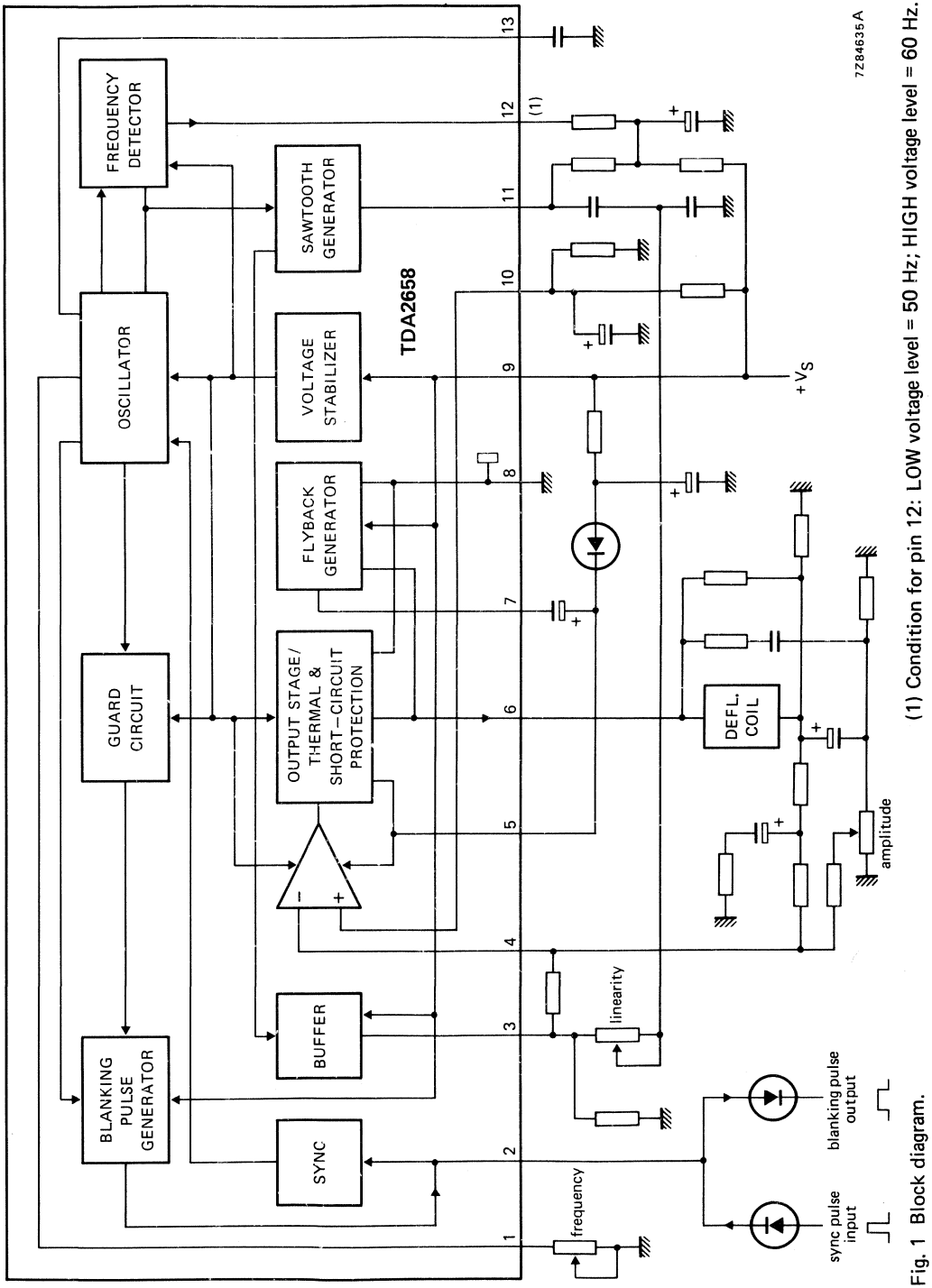
- Oscillator; switch capability for 50 Hz/60 Hz operation.
- Synchronization circuit.
- Blanking pulse generator with guard circuit.
- Sawtooth generator with buffer stage.
- Preamplifier with fed-out inputs.
- Output stage with thermal and short-circuit protection.
- Flyback generator.
- Voltage stabilizer.

QUICK REFERENCE DATA

Supply voltage (pin 9)	$V_{9-8} = V_S$	typ.	26	V
Supply current (pin 5 + pin 9)	$I_5 + I_9 = I_S$	typ.	250	mA
Output current (peak-to-peak value)	$I_{6(p-p)}$	typ.	1,6	A
Picture frequency	f		50 Hz/60	Hz
Sync input pulse (peak-to-peak value)	$V_{2-8(p-p)}$	$\geqslant$	1	V
Thermal resistance from junction to mounting base	$R_{th\ j-mb}$	$\leqslant$	5	K/W

PACKAGE OUTLINE

13-lead SIL; plastic power (SOT141B).



(1) Condition for pin 12: LOW voltage level = 50 Hz; HIGH voltage level = 60 Hz.

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 9)	$V_{9-8} = V_S$	max.	40 V
Supply voltage output stage (pin 5)	V_{5-8}	max.	58 V
Voltages			
Pin 3	V_{3-11}	max.	7 V
Pin 13	V_{13-8}	max.	7 V
Pins 4 and 10	$V_{4;10-8}$	max.	24 V
Pin 6	V_{6-8}	max.	58 V
	$-V_{6-8}$	max.	0 V
Pins 7 and 11	$V_{7;11-8}$	max.	40 V
Currents			
Pin 1	I_1	max.	0 mA
	$-I_1$	max.	1 mA
Pin 2	$\pm I_2$	max.	10 mA
Pin 3	I_3	max.	0 mA
	$-I_3$	max.	5 mA
Pin 7	I_7	max.	0,9 A
	$-I_7$	max.	1,1 A
Pin 11	I_{11}	max.	50 mA
	$-I_{11}$	max.	1 mA
Pin 12	I_{12}	max.	3 mA
	$-I_{12}$	max.	0 mA

Pins 5, 6 and 8: internally limited by the short-circuit protection circuit.

Total power dissipation: internally limited by the thermal protection circuit.

Storage temperature range	T_{stg}	−25 to + 150 °C
Operating ambient temperature range	T_{amb}	0 °C to limiting value

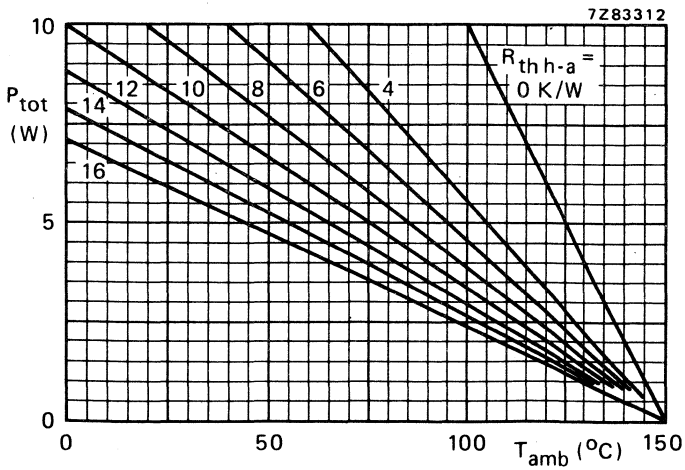


Fig. 2 Total power dissipation. $R_{th\ h\text{-}a}$ includes $R_{th\ mb\text{-}h}$ which is expected when heat-sink compound is used. $R_{th\ j\text{-}mb} \leqslant 5$ K/W.

CHARACTERISTICS

T_{amb} = 25 °C; V_S = 26 V; unless otherwise specified.

Supply voltage/output stage			
Supply voltage	$V_{9-8} = V_S$		9 to 30 V
Output voltage			
at $-I_6$ = 0,75 A	V_{6-8}	⩾	$V_{5-8} - 2{,}2$ V
		typ.	$V_{5-8} - 1{,}9$ V
at I_6 = 0,75 A	V_{6-8}	typ.	1,3 V
		⩽	1,6 V
Flyback generator output voltage at $-I_6$ = 0,75 A	V_{7-8}	typ.	$V_S - 2{,}2$ V
Peak output current	$\pm I_6$	⩽	0,9 A
Flyback generator peak current	$\pm I_7$	⩽	0,9 A
Feedback			
Input quiescent current	$-I_{4;10}$	typ.	0,1 μA
Synchronization			
Sync input pulse	V_{2-8}		1 to 12 V
Tracking range		typ.	28 %
Oscillator/sawtooth generator			
Oscillator frequency control input voltage	V_{1-8}		6 to 9 V
Sawtooth generator output voltage	V_{3-8}		0 to $V_S - 1{,}5$ V
	V_{11-8}		0 to $V_S - 1{,}5$ V
Sawtooth generator output current	$-I_3$		0 to 4 mA
	I_{11}	⩾	−2 μA
		⩽	+30 mA
Oscillator temperature dependency			
T_{case} = 20 to 100 °C	$(\Delta f/f)/\Delta T_{case}$	typ.	10^{-4} K^{-1}
Oscillator voltage dependency			
V_S = 10 to 30 V	$(\Delta f/f)/\Delta V_S$	typ.	4×10^{-4} V^{-1}
Blanking pulse generator			
Output voltage			
at V_S = 24 V; I_2 = 1 mA	V_{2-8}	typ.	18,5 V
Output current	$-I_2$	⩽	3 mA
Output resistance	R_{2-8}	typ.	410 Ω
Blanking pulse duration at 50 Hz sync	t_b	typ.	1,4 ± 0,07 ms
50 Hz/60 Hz switch capability			
Saturation voltage; LOW voltage level	V_{12-8}	typ.	1 V
Output leakage current	I_{12}	typ.	1 μA

Thermal resistance/junction temperature

From junction to mounting base	$R_{th\ j\text{-}mb}$	⩽	5 K/W
Junction temperature; switching point thermal protection	T_j	typ.	150 ± 8 °C

PINNING

1. Oscillator adjustment
2. Synchronization input/blanking output
3. Sawtooth generator output
4. Preamplifier input
5. Positive supply of output stage
6. Output
7. Flyback generator output
8. Ground
9. Positive supply (V_S)
10. Reference voltage
11. Sawtooth capacitor
12. 50 Hz/ 60 Hz switching voltage
13. Oscillator capacitor

APPLICATION INFORMATION

The function is described against the corresponding pin number

1, 13. Oscillator

The oscillator frequency is determined by a potentiometer at pin 1 and a capacitor at pin 13.

2. Sync input/blanking output

Combination of sync input and blanking output. The oscillator has to be synchronized by a positive-going pulse between 1 and 12 V. The integrated frequency detector delivers a switching level at pin 12.
The blanking pulse amplitude is 20 V with a load of 1 mA (V_S = 26 V).

3. Sawtooth generator output

The sawtooth signal is fed via a buffer stage to pin 3. It delivers the signal which is used for linearity control, and drive of the preamplifier. The sawtooth is applied via a shaping network to pin 11 (linearity) and via a resistor to pin 4 (preamplifier).

4. Preamplifier input

The d.c. voltage is proportional to the output voltage (d.c. feedback). The a.c. voltage is proportional to the sum of the buffered sawtooth voltage at pin 3 and the voltage, with opposite polarity, at the feedback resistor (a.c. feedback).

5. Positive supply of output stage

This supply is obtained from the flyback generator. An electrolytic capacitor between pins 7 and 5, and a diode between pins 5 and 9 have to be connected for proper operation of the flyback generator.

6. Output of class-B power stage

The vertical deflection coil is connected to this pin, via a series connection of a coupling capacitor and a feedback resistor, to ground.

7. Flyback generator output

An electrolytic capacitor has to be connected between pins 7 and 5 to complete the flyback generator.

8. Negative supply (ground)

Negative supply of output stage and small signal part.

9. Positive supply

The supply voltage at this pin is used to supply the flyback generator, voltage stabilizer, blanking pulse generator and buffer stage.

APPLICATION INFORMATION (continued)

10. Reference voltage of preamplifier

    External adjustment and decoupling of reference voltage of the preamplifier.

11. Sawtooth capacitor

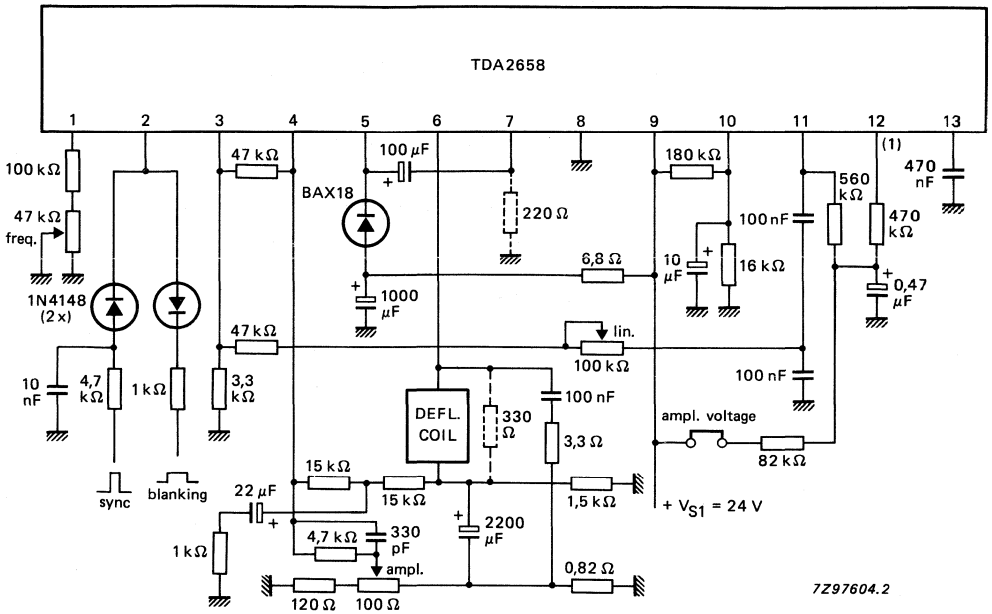
    This sawtooth capacitor has been split to realize linearity control.

12. 50 Hz/60 Hz switching level

    This pin delivers a LOW voltage level for 50 Hz and a HIGH voltage level for 60 Hz. The amplitudes of the sawtooth signals can be made equal for 50 Hz and 60 Hz with these levels.

The following application data are measured in Fig. 3

System supply voltages	V_{S1}	typ.	24	V
System supply currents	I_{S1}	typ.	145	mA
Output voltage	V_{6-8}	typ.	14	V
Output voltage (peak value)	V_{6-8}	typ.	44	V
Deflection current (peak-to-peak value)	$I_{6(p-p)}$	typ.	1	A
Flyback time	t_{fl}	typ.	1	ms
Total power dissipation per package	P_{tot}	typ. max.	1,7 2,2	W W
Oscillator frequency unsynchronized	f	typ.	46,5	Hz



(1) Condition for pin 12: LOW voltage level = 50 Hz; HIGH voltage level = 60 Hz.

Fig. 3 Typical vertical deflection circuit.

TV STEREO/DUAL SOUND IDENTIFICATION DECODER

The TDA2795 is a monolithic integrated circuit for stereo/dual sound in television receivers.

The circuit incorporates the following functions:

- Controlled pilot signal amplifier.
- Envelope demodulator.
- Two separate signal paths for processing the identification frequencies: operational amplifier for active filter, integral evaluation circuit with TTL compatible 'open collector' outputs.
- Stereo indicator driver.

QUICK REFERENCE DATA

Supply voltage	V_S	typ.	12 V
Supply current	I_S	typ.	8 mA
Nominal input voltage at f = 54,6875 kHz	V_i	typ.	10 mV
Input impedance	$\|Z_i\|$	$\geqslant$	500 kΩ
Operational amplifier			
open loop voltage gain at 200 Hz	G_o	$\geqslant$	78 dB
input resistance	R_i	$\geqslant$	1 MΩ
output resistance	R_o	$\leqslant$	3,5 kΩ
Supply voltage range	V_S		10,8 to 13,2 V
Operating ambient temperature range	T_{amb}		0 to + 70 °C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

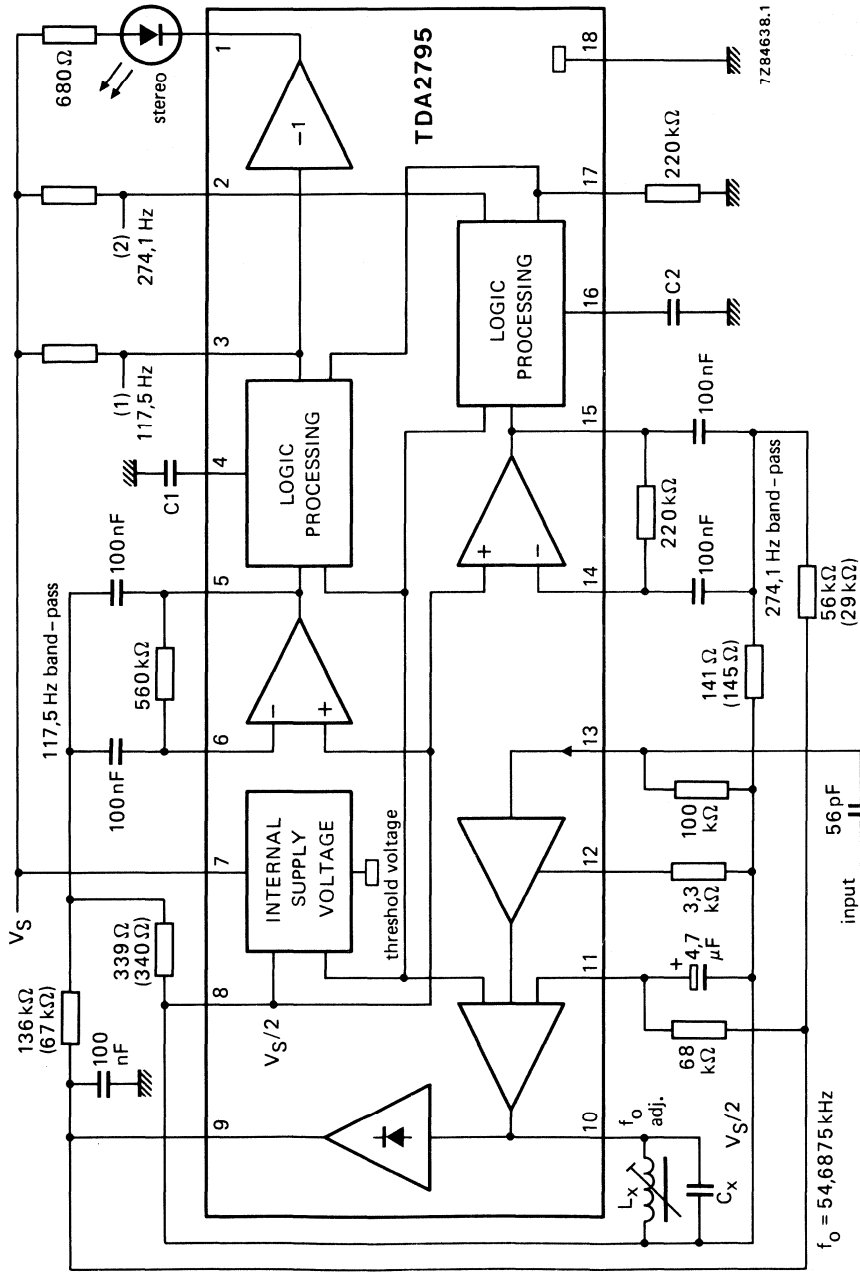


Fig. 1 Block diagram; C1 and C2 values 22 to 150 nF (dependent on switching time); values given in parenthesis are for G = 4 at 117,5/274,1 Hz; C_x = 3,3 nF.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 7)	$V_{7-18} = V_S$	max.	15 V
Signal input (pin 13)	V_{13-18}	max.	V_S V
	$-V_{13-18}$	max.	0,5 V
Switch outputs (pins 1, 2 and 3)	V_{1-18}	max.	18 V
	I_1	max.	50 mA
	$V_{2;3-18}$	max.	15 V
	$I_{2;3}$	max.	5 mA
	$-V_{1;2;3-18}$	max.	0,5 V
Total power dissipation	P_{tot}	max.	800 mW
Storage temperature range	T_{stg}		−25 to +125 °C
Operating ambient temperature range	T_{amb}		0 to + 70 °C

CHARACTERISTICS

V_S = 12 V; T_{amb} = 25 °C, unless otherwise specified; measured in Fig. 1, at V_i = 10 mV; f = 54,6875 kHz amplitude modulated with f_{m1} = 117,5 Hz or f_{m2} = 274,1 Hz; $m_1 = m_2$ = 50%.

Supply voltage range	V_S	10,8 to	13,2 V
Supply current	I_S	typ.	8 mA
		⩽	12 mA

Pilot signal amplifier and envelope demodulator

Maximum input voltage (peak-to-peak value)	$V_{i(p-p)}$	typ.	2 V
Input impedance	$\|Z_{13-18}\|$	⩾	500 kΩ
Voltage gain (V_{9-18}/V_{13-18}) at V_i = 1 mV	G_{v9-13}	typ.	42 dB
Start of control at V_i	see Fig. 3		
Control range	ΔG_v	⩾	40 dB
Controlled output voltage (r.m.s. value) (pin 9)	$V_{o(rms)}$	typ.	550 mV

Operational amplifiers

Input bias current (pins 6 and 14)	$\pm I_6; \pm I_{14}$	⩽	70 nA
Open loop voltage gain at f = 200 Hz	G_o	⩾	78 dB
Available output current (pins 5 and 15)	$\pm I_5; \pm I_{15}$	⩾	1,5 mA
Output resistance (pins 5 and 15)	R_o	typ.	2 kΩ
		⩽	3,5 kΩ
Allowable load capacitance	C_L	⩽	30 pF
Output offset voltage at R_{5-6} = 560 kΩ	$\pm V_{o5-8}$	⩽	70 mV

CHARACTERISTICS (continued)

Evaluation circuitry

Switch-on threshold voltage (pins 5 and 15)	$V_5; V_{15}$	typ.	1,0 V
Switch hysteresis	$\frac{V_{5on}}{V_{5off}} = \frac{V_{15on}}{V_{15off}}$	typ.	3,8 ± 0,5 dB
Switch outputs (pins 2 and 3)			
allowable output current	$I_3; I_2$	$\leqslant$	2 mA
saturation voltage at $I_3 = I_2 = 1{,}5$ mA	$V_{3;2\text{-}18sat}$	$\leqslant$	0,35 V
leakage voltage at $I_3 = I_2 \leqslant 5\ \mu A$	$V_{3;2\text{-}18}$	$\leqslant$	15 V
Indicator driver (pin 1)			
allowable output current	I_1	$\leqslant$	40 mA
saturation voltage at $I_1 = 20$ mA	$V_{1\text{-}18sat}$	$\leqslant$	0,8 V
leakage voltage at $I_1 < 10\ \mu A$	$V_{1\text{-}18}$	$\leqslant$	18 V

Internal reference voltage

Reference voltage (pin 8)	$V_{8\text{-}18}$	typ.	6 V
Available output current (pin 8)	$-I_8$	$\geqslant$	2 mA
	$+I_8$	$\geqslant$	0,6 mA

Reference current source

Reference voltage (pin 17)	$V_{17\text{-}18}$	typ.	5,3 V
Internal bias resistor	R_{i17}	typ.	5 kΩ
Allowable load resistor (pin 17)	R_L		180 to 270 kΩ

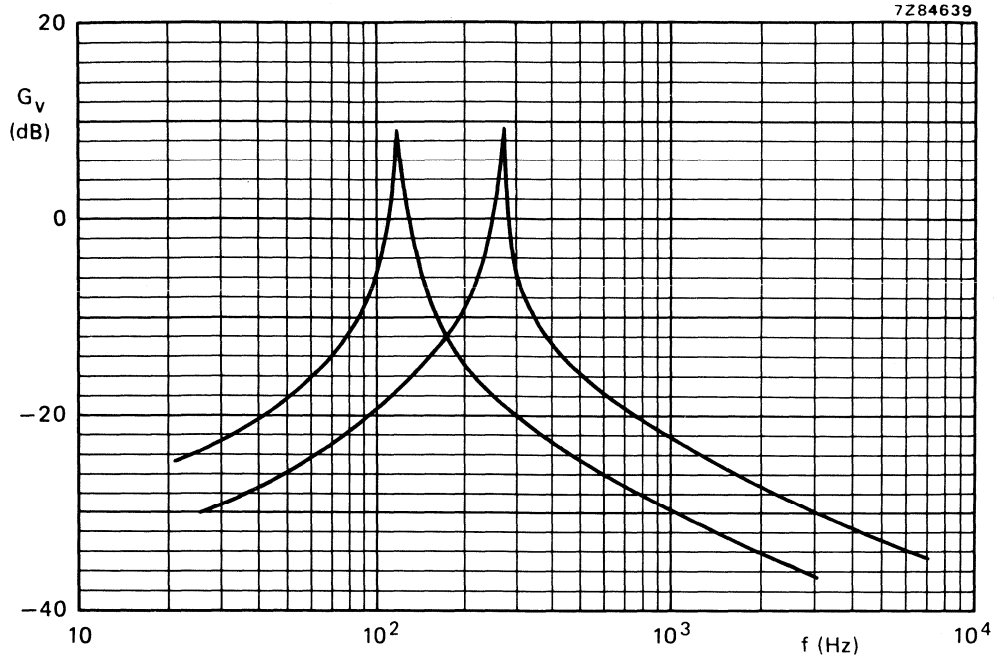


Fig. 2 Band-pass curves for 117,5 Hz and 274,1 Hz.

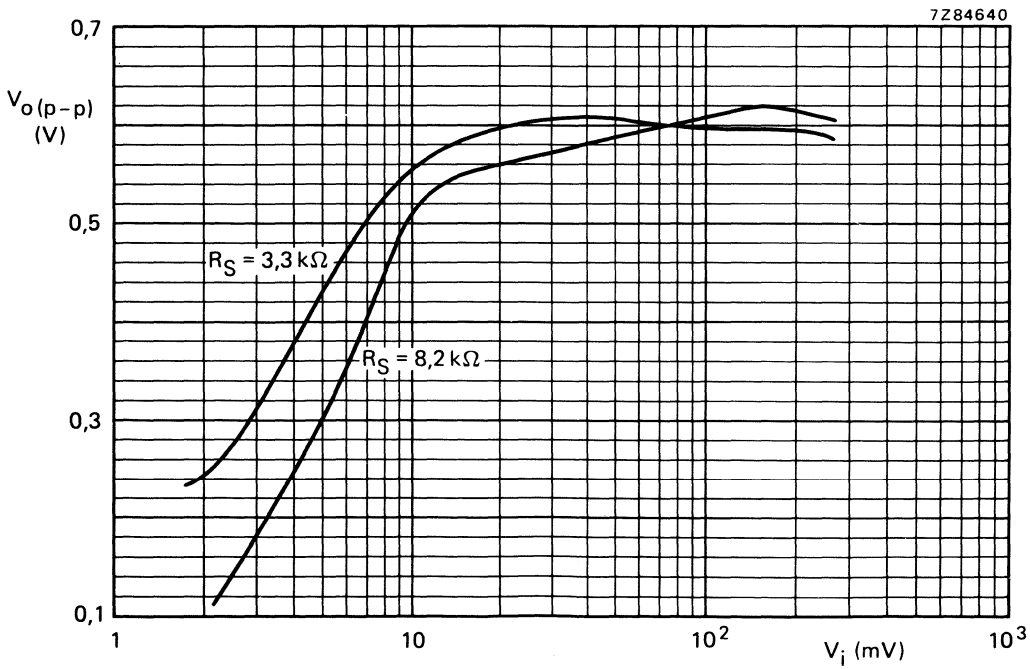


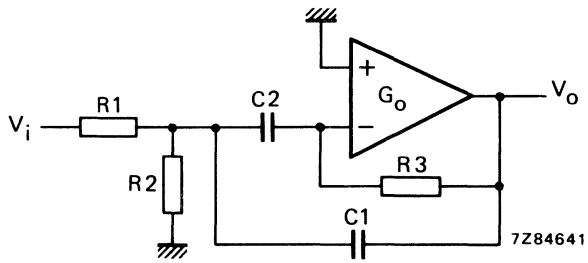
Fig. 3 Controlled output voltage as a function of the input signal (Q_o = 80); pilot frequency f_o = 54,6875 kHz; R_S is source resistance.

GENERAL FILTER CALCULATIONS

1. Gain

Amplifier conditions: $G_o >> G_v$ and $G_o >> 2 \cdot Q^2$

$$G_v = - \frac{\frac{p}{R1 \cdot C1}}{p^2 + p\frac{C1 + C2}{R3 \cdot C1 \cdot C2} + \frac{R1 + R2}{R1 \cdot R2 \cdot R3 \cdot C1 \cdot C2}}, \text{ in which: } p = j\omega; G_v = \frac{V_o}{V_i}$$



2. Resonance frequency

$$\omega_r = \frac{1}{\sqrt{\frac{R1 \cdot R2}{R1 + R2} \cdot R3 \cdot C1 \cdot C2}}$$

3. Gain at $\omega = \omega_r$

$$-G_{vr} = \frac{C2}{C1 + C2} \cdot \frac{R3}{R1}$$

4. Quality

$$Q = \frac{\sqrt{C1 \cdot C2}}{C1 + C2} \cdot \sqrt{\frac{R3\,(R1 + R2)}{R1 \cdot R2}}$$

5. Recommended components

C1 and C2: 5% MKC (metallized polycarbonate film capacitor)
R1, R2 and R3: 2% MR (metal film resistor)

or:

C1 and C2: 5% MKT (metallized polyester film capacitor)
R1, R2 and R3: 2% CR (carbon film resistor)

INFRARED RECEIVER

The TDA3047 is for infrared reception with low power consumption.
The difference between the TDA3047 and TDA3048 is the polarity of the output signal.

Features

- H.F. amplifier with a control range of 66 dB
- Synchronous demodulator and reference amplifier
- A.G.C. detector
- Pulse shaper
- Q-factor killing of the input selectivity, which is controlled by the a.g.c. circuit
- Input voltage limiter

QUICK REFERENCE DATA

Supply voltage (pin 8)	$V_P = V_{8-16}$	typ.	5 V
Supply current (pin 8)	$I_P = I_8$	typ.	2,1 mA
Input signal (peak-to-peak value) (100% AM; f = 36 kHz)	$V_{2-15(p-p)}$	0,03 to 200	mV
Output signal (peak-to-peak value)	$V_{9-16(p-p)}$	typ.	4,5 V

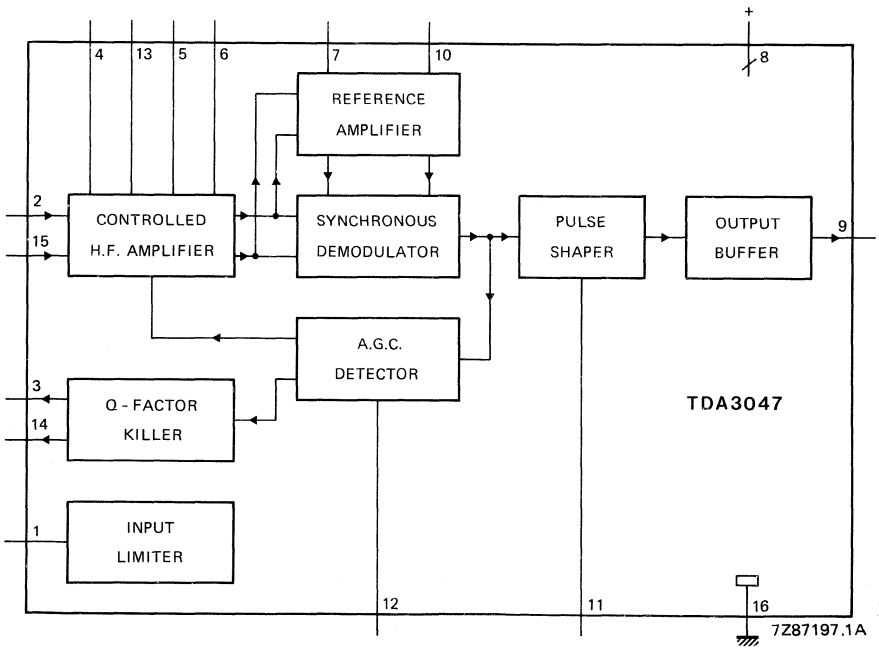


Fig. 1 Block diagram of TDA3047.

PACKAGE OUTLINES

TDA3047P: 16-lead DIL; plastic (SOT38).
TDA3047T: 16-lead mini-pack; plastic (SO16L; SOT162A).

FUNCTIONAL DESCRIPTION

General

The circuit operates from a 5 V supply and has a current consumption of 2 mA. The output is a current source which can drive or suppress a current of $> 75\ \mu A$ with a voltage swing of 4,5 V. The Q-killer circuit eliminates distortion of the output pulses due to the decay of the tuned input circuit at high input voltages. The input circuit is protected against signals of > 600 mV by an input limiter. The typical input is an AM signal at a frequency of 36 kHz. Figures 3 and 4 show the circuit diagrams for the application of narrow-band and wide-band receivers respectively. Circuit description of the eight sections shown in Fig. 1 are given below.

Controlled h.f. amplifier

The input signal is amplified by the gain-controlled amplifier. This circuit comprises three d.c. amplifier stages connected in cascade. The overall gain of the circuit is approximately 83 dB and the gain control range is in the order of 66 dB. Gain control is initially active in the second amplifier stage and is transferred to the first stage as limiting in the second stage occurs, thus maintaining optimum signal-to-noise ratio. Offset voltages in the d.c. coupled amplifier are minimized by two negative feedback loops; these also allow the circuit to have some series resistance of the decoupling capacitor. The output signal of the amplifier is applied to the reference amplifier and to the synchronous demodulator inputs.

Reference amplifier

The reference amplifier amplifies and limits the input signal. The voltage gain is approximately 0 dB. The output signal of this amplifier is applied to the synchronous demodulator.

Synchronous demodulator

In the synchronous demodulator the input signal and reference signal are multiplied. The demodulator output current is 25 μA peak-to-peak. The output signal of the demodulator is fed to the input of the a.g.c. detector and to the input of the pulse-shaper circuit.

A.G.C. detector

The a.g.c. detector comprises two n-p-n transistors operating as a differential pair. The top level of the output signal from the synchronous demodulator is detected by the a.g.c. circuit. Noise pulses are integrated by an internal capacitor. The output signal is amplified and applied to the first and second stages of the amplifier and to the Q-factor killer circuit.

Pulse-shaper

The pulse-shaper comprises two n-p-n transistors operating as a differential pair connected in parallel with the a.g.c. differential pair. The slicing level of the pulse shaper is lower than the slicing level of the a.g.c. detector. The output of the pulse-shaper is determined by the voltage of the capacitor connected to pin 11, which is applied directly to the output buffer.

Output buffer

The voltage of the pulse-shaper capacitor is fed to the base of the first transistor of a differential pair. To obtain a correct RC-5 code, a hysteresis circuit protects the output against spikes. The output at pin 9 is active *high*.

Q-factor killer

Figure 3 shows the Q-factor killer in the narrow-band application. In this application it is necessary to decrease the Q-factor of the input selectivity particularly when large input signals occur at pins 2 and 15. In the narrow-band application the output of the Q-factor killer can be directly coupled to the input; pin 3 to pin 2 and pin 14 to pin 15.

Input limiter

In the narrow-band application high voltage peaks can occur on the input of the selectivity circuit. The input limiter limits these voltage peaks to approximately 0,7 V. Limiting is 0,9 V max. at I_1 = 3 mA.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 8)	$V_P = V_{8\text{-}16}$	max.	13,2 V
Output current pulse shaper (pin 11)	I_{11}	max.	10 mA
Voltages between pins*			
pins 2 and 15	$V_{2\text{-}15}$	max.	4,5 V
pins 4 and 13	$V_{4\text{-}13}$	max.	4,5 V
pins 5 and 6	$V_{5\text{-}6}$	max.	4,5 V
pins 7 and 10	$V_{7\text{-}10}$	max.	4,5 V
pins 9 and 11	$V_{9\text{-}11}$	max.	4,5 V
Storage temperature range	T_{stg}		−65 to + 150 °C
Operating ambient temperature range	T_{amb}		−25 to + 125 °C

* All pins except pin 11 are short-circuit protected.

CHARACTERISTICS

$V_P = V_{8-16} = 5$ V; $T_{amb} = 25$ °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 8)					
Supply voltage	$V_P = V_{8-16}$	4,65	5,0	5,35	V
Supply current	$I_P = I_8$	1,2	2,1	3,0	mA
Controlled h.f. amplifier (pins 2 and 15)					
Minimum input signal (peak-to-peak value)					
at f = 36 kHz (note 1)	$V_{2-15(p-p)}$	–	15	25	μV
at f = 36 kHz (note 2)	$V_{2-15(p-p)}$	–	–	5	μV
A.G.C. control range (without Q-killing)		60	66	–	dB
Input signal for correct operation (peak-to-peak value; note 3)	$V_{2-15(p-p)}$	0,03	–	200	mV
Q-killing inactive ($I_3 = I_{14} < 0{,}5$ μA) (peak-to-peak value)	$V_{2-15(p-p)}$	–	–	140	μV
Q-killing active ($I_{14} = I_3$ = max.) (peak-to-peak value)	$V_{2-15(p-p)}$	28	–	–	mV
Q-killing range		see Fig. 2			
Inputs					
Input voltage (pin 2)	V_{2-16}	2,25	2,45	2,65	V
Input voltage (pin 15)	V_{15-16}	2,25	2,45	2,65	V
Input resistance (pin 2)	R_{2-15}	10	15	20	kΩ
Input capacitance (pin 2)	C_{2-15}	–	3	–	pF
Input limiting (pin 1) at I_1 = 3 mA	V_{1-16}	–	0,8	0,9	V
Outputs					
Output voltage *high* (pin 9) at $-I_9 = 75$ μA	$-V_{9-8}$	–	0,1	0,5	V
Output voltage *low* (pin 9) at $I_9 = 75$ μA	V_{9-16}	–	0,1	0,5	V
Output current; output voltage *high*					
at $V_{9-16} = 4{,}5$ V	$-I_9$	75	120	–	μA
at $V_{9-16} = 3{,}0$ V	$-I_9$	75	130	–	μA
at $V_{9-16} = 1{,}0$ V	$-I_9$	75	140	–	μA
Output current; output voltage *low*					
at $V_{9-16} = 0{,}5$ V	$-I_9$	75	120	–	μA
Output resistance between pins 7 and 10	R_{7-10}	3,1	4,7	6,2	kΩ

Notes

1. Voltage pin 9 is *high*; $-I_9 = 75$ μA.
2. Voltage pin 9 remains *low*.
3. Undistorted output pulse with 100% AM input.

parameter	symbol	min.	typ.	max.	unit
Pulse shaper (pin 11)					
Trigger level in positive direction (voltage pin 9 changes from *high* to *low*)	V_{11-16}	3,75	3,9	4,05	V
Trigger level in negative direction (voltage pin 9 changes from *low* to *high*)	V_{11-16}	3,4	3,55	3,7	V
Hysteresis of trigger levels	ΔV_{11-16}	0,25	0,35	0,45	V
A.G.C. detector (pin 12)					
A.G.C. capacitor charge current	$-I_{12}$	3,4	5,0	6,6	μA
A.G.C. capacitor discharge current	I_{12}	67	100	133	μA
Q-factor killer (pins 3 and 14)					
Output current (pin 3) at $V_{12-16} = 2$ V	$-I_3$	2,5	7,5	20	μA
Output current (pin 14) at $V_{12-16} = 2$ V	$-I_{14}$	2,5	7,5	20	μA

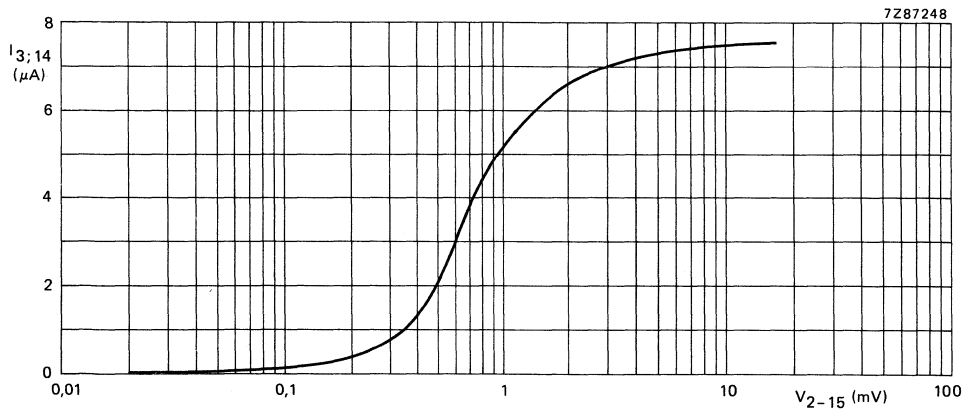
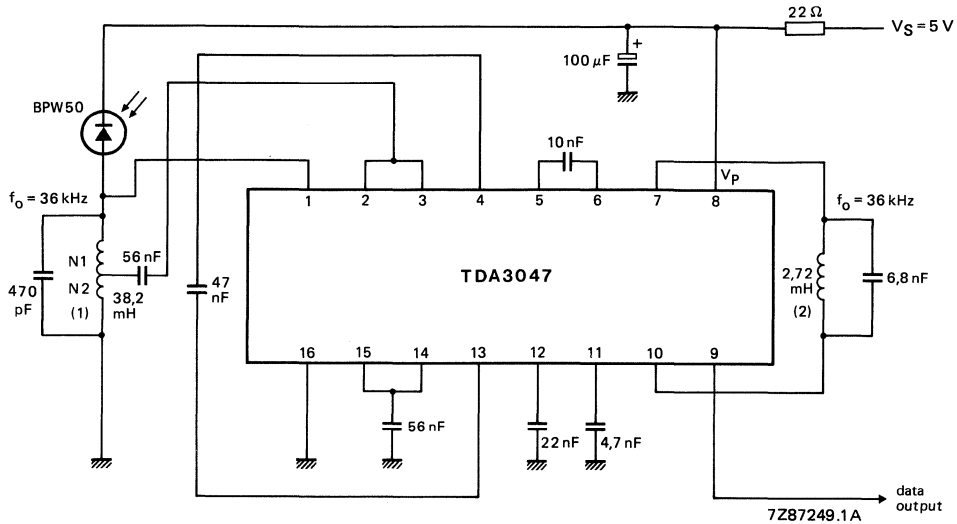


Fig. 2 Typical Q-factor killer current (pins 3 and 14) as a function of the peak-to-peak input voltage (V_{2-15}); $I_{3,14}$ is measured to ground, $V_{2-15(p-p)}$ is a symmetrical square wave. Measured in Fig. 4; $V_P = 5$ V.

APPLICATION INFORMATION



(1) N1 = 3,21
N2 = 1
Q = 16

(2) Q = 6

Fig. 3 Narrow-band receiver using TDA3047.

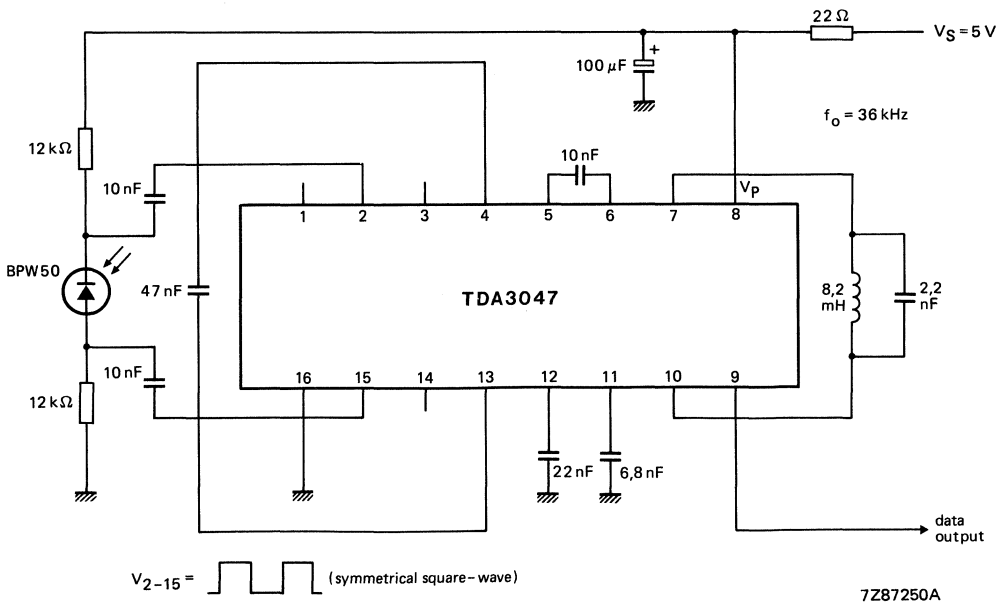


Fig. 4 Wide-band receiver with TDA3047.

For better sensitivity both 12 kΩ resistors may have a higher value.

INFRARED RECEIVER

The TDA3048 is for infrared reception with low power consumption.
The difference between the TDA3048 and TDA3047 is the polarity of the output signal.

Features

- H.F. amplifier with a control range of 66 dB
- Synchronous demodulator and reference amplifier
- A.G.C. detector
- Pulse shaper
- Q-factor killing of the input selectivity, which is controlled by the a.g.c. circuit
- Input voltage limiter

QUICK REFERENCE DATA

Supply voltage (pin 8)	$V_P = V_{8-16}$	typ.	5 V
Supply current (pin 8)	$I_P = I_8$	typ.	2,1 mA
Input signal (peak-to-peak value) (100% AM; f = 36 kHz)	$V_{2-15(p-p)}$		0,03 to 200 mV
Output signal (peak-to-peak value)	$V_{9-16(p-p)}$	typ.	4,5 V

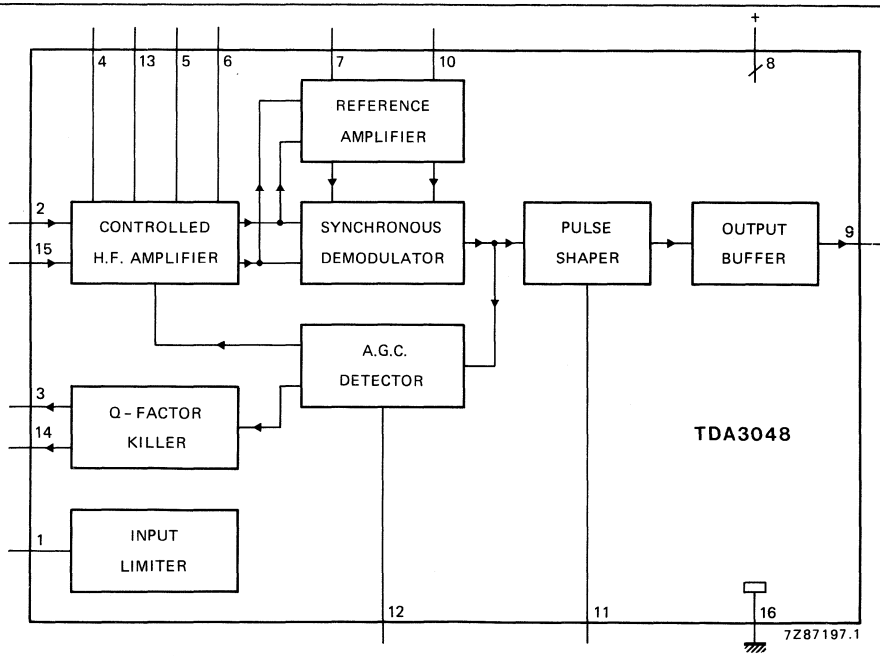


Fig. 1 Block diagram of TDA3048.

PACKAGE OUTLINES

TDA3048P: 16-lead DIL; plastic (SOT38).
TDA3048T: 16-lead mini-pack; plastic (SO16L; SOT162A).

FUNCTIONAL DESCRIPTION

General

The circuit operates from a 5 V supply and has a current consumption of 2 mA. The output is a current source which can drive or suppress a current of $> 75\ \mu A$ with a voltage swing of 4,5 V. The Q-killer circuit eliminates distortion of the output pulses due to the decay of the tuned input circuit at high input voltages. The input circuit is protected against signals of > 600 mV by an input limiter. The typical input is an AM signal at a frequency of 36 kHz. Figures 3 and 4 show the circuit diagrams for the application of narrow-band and wide-band receivers respectively. Circuit description of the eight sections shown in Fig. 1 are given below.

Controlled h.f. amplifier

The input signal is amplified by the gain-controlled amplifier. This circuit comprises three d.c. amplifier stages connected in cascade. The overall gain of the circuit is approximately 83 dB and the gain control range is in the order of 66 dB. Gain control is initially active in the second amplifier stage and is transferred to the first stage as limiting in the second stage occurs, thus maintaining optimum signal-to-noise ratio. Offset voltages in the d.c. coupled amplifier are minimized by two negative feedback loops; these also allow the circuit to have some series resistance of the decoupling capacitor. The output signal of the amplifier is applied to the reference amplifier and to the synchronous demodulator inputs.

Reference amplifier

The reference amplifier amplifies and limits the input signal. The voltage gain is approximately 0 dB. The output signal of this amplifier is applied to the synchronous demodulator.

Synchronous demodulator

In the synchronous demodulator the input signal and reference signal are multiplied. The demodulator output current is 25 μA peak-to-peak. The output signal of the demodulator is fed to the input of the a.g.c. detector and to the input of the pulse-shaper circuit.

A.G.C. detector

The a.g.c. detector comprises two n-p-n transistors operating as a differential pair. The top level of the output signal from the synchronous demodulator is detected by the a.g.c. circuit. Noise pulses are integrated by an internal capacitor. The output signal is amplified and applied to the first and second stages of the amplifier and to the Q-factor killer circuit.

Pulse-shaper

The pulse-shaper comprises two n-p-n transistors operating as a differential pair connected in parallel with the a.g.c. differential pair. The slicing level of the pulse shaper is lower than the slicing level of the a.g.c. detector. The output of the pulse-shaper is determined by the voltage of the capacitor connected to pin 11, which is applied directly to the output buffer.

Output buffer

The voltage of the pulse-shaper capacitor is fed to the base of the first transistor of a differential pair. To obtain a correct RC-5 code, a hysteresis circuit protects the output against spikes. The output at pin 9 is active *low*.

Q-factor killer

Figure 3 shows the Q-factor killer in the narrow-band application. In this application it is necessary to decrease the Q-factor of the input selectivity particularly when large input signals occur at pins 2 and 15. In the narrow-band application the output of the Q-factor killer can be directly coupled to the input; pin 3 to pin 2 and pin 14 to pin 15.

Input limiter

In the narrow-band application high voltage peaks can occur on the input of the selectivity circuit. The input limiter limits these voltage peaks to approximately 0,7 V. Limiting is 0,9 V max. at I_1 = 3 mA.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 8)	$V_P = V_{8-16}$	max.	13,2 V
Output current pulse shaper (pin 11)	I_{11}	max.	10 mA
Voltages between pins*			
pins 2 and 15	V_{2-15}	max.	4,5 V
pins 4 and 13	V_{4-13}	max.	4,5 V
pins 5 and 6	V_{5-6}	max.	4,5 V
pins 7 and 10	V_{7-10}	max.	4,5 V
pins 9 and 11	V_{9-11}	max.	4,5 V
Storage temperature range	T_{stg}		−65 to + 150 °C
Operating ambient temperature range	T_{amb}		−25 to + 125 °C

* All pins except pin 11 are short-circuit protected.

CHARACTERISTICS

$V_P = V_{8-16} = 5$ V; $T_{amb} = 25$ °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 8)					
Supply voltage	$V_P = V_{8-16}$	4,65	5,0	5,35	V
Supply current	$I_P = I_8$	1,2	2,1	3,0	mA
Controlled h.f. amplifier (pins 2 and 15)					
Minimum input signal (peak-to-peak value)					
at f = 36 kHz (note 1)	$V_{2-15(p-p)}$	–	15	25	μV
at f = 36 kHz (note 2)	$V_{2-15(p-p)}$	–	–	5	μV
A.G.C. control range (without Q-killing)		60	66	–	dB
Input signal for correct operation (peak-to-peak value; note 3)	$V_{2-15(p-p)}$	0,03	–	200	mV
Q-killing inactive ($I_3 = I_{14} < 0{,}5$ μA) (peak-to-peak value)	$V_{2-15(p-p)}$	–	–	140	μV
Q-killing active ($I_{14} = I_3$ = max.) (peak-to-peak value)	$V_{2-15(p-p)}$	28	–	–	mV
Q-killing range			see Fig. 2		
Inputs					
Input voltage (pin 2)	V_{2-16}	2,25	2,45	2,65	V
Input voltage (pin 15)	V_{15-16}	2,25	2,45	2,65	V
Input resistance (pin 2)	R_{2-15}	10	15	20	kΩ
Input capacitance (pin 2)	C_{2-15}	–	3	–	pF
Input limiting (pin 1) at I_1 = 3 mA	V_{1-16}	–	0,8	0,9	V
Outputs					
Output voltage *high* (pin 9) at $-I_9 = 75$ μA	$-V_{9-8}$	–	0,1	0,5	V
Output voltage *low* (pin 9) at $I_9 = 75$ μA	V_{9-16}	–	0,1	0,5	V
Output current; output voltage *low*					
$-V_{9-8} = 4{,}5$ V	I_9	75	120	–	μA
$-V_{9-8} = 3{,}0$ V	I_9	75	130	–	μA
$-V_{9-8} = 1{,}0$ V	I_9	75	140	–	μA
Output current; output voltage *high*					
$-V_{9-8} = 0{,}5$ V	$-I_9$	75	120	–	μA
Output resistance between pins 7 and 10	R_{7-10}	3,1	4,7	6,2	kΩ

Notes

1. Voltage pin 9 is *low*; $I_9 = 75$ μA.
2. Voltage pin 9 remains *high*.
3. Undistorted output pulse with 100% AM input.

parameter	symbol	min.	typ.	max.	unit
Pulse shaper (pin 11)					
Trigger level in positive direction (voltage pin 9 changes from *high* to *low*	V_{11-16}	3,75	3,9	4,05	V
Trigger level in negative direction (voltage pin 9 changes from *low* to *high*	V_{11-16}	3,4	3,55	3,7	V
Hysteresis of trigger levels	ΔV_{11-16}	0,25	0,35	0,45	V
A.G.C. detector (pin 12)					
A.G.C. capacitor charge current	$-I_{12}$	3,4	5,0	6,6	μA
A.G.C. capacitor discharge current	I_{12}	67	100	133	μA
Q-factor killer (pins 3 and 14)					
Output current (pin 3) at $V_{12-16} = 2$ V	$-I_3$	2,5	7,5	20	μA
Output current (pin 14) at $V_{12-16} = 2$ V	$-I_{14}$	2,5	7,5	20	μA

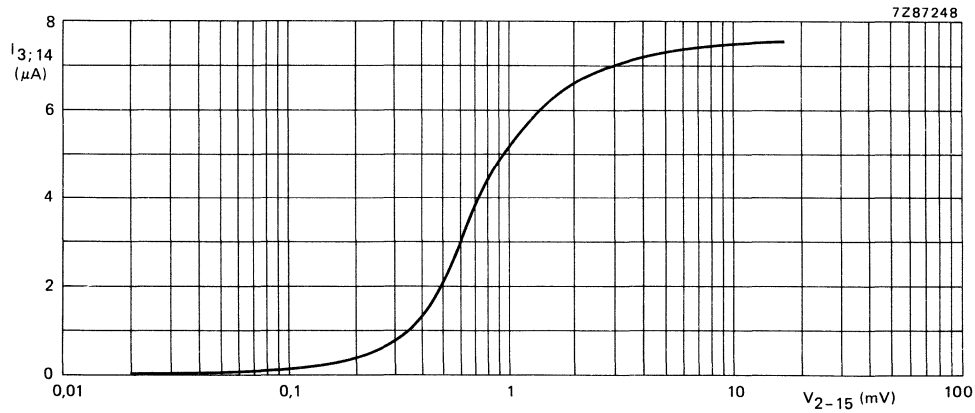
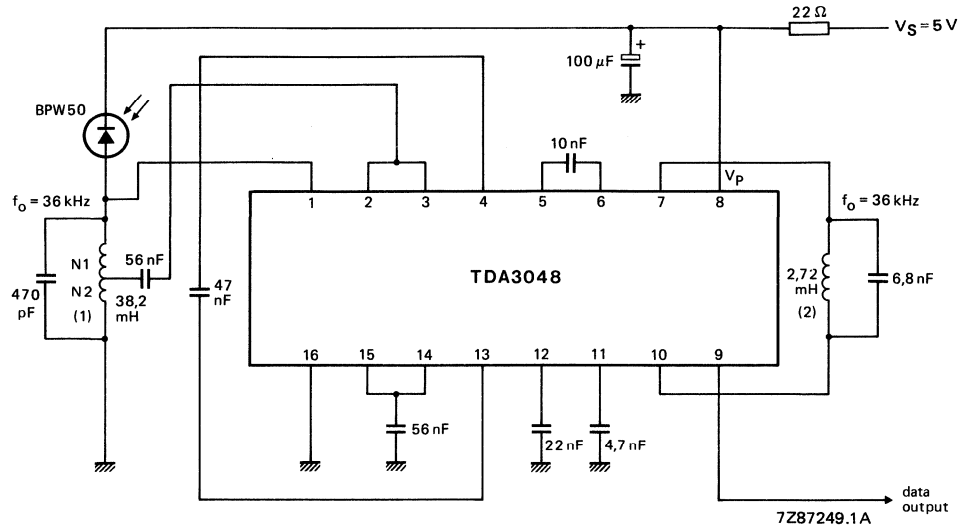


Fig. 2 Typical Q-factor killer current (pins 3 and 14) as a function of the peak-to-peak input voltage (V_{2-15}); $I_{3,14}$ is measured to ground, $V_{2-15(p-p)}$ is a symmetrical square wave. Measured in Fig. 4; $V_P = 5$ V.

APPLICATION INFORMATION



(1) N1 = 3,21
N2 = 1
Q = 16

(2) Q = 6

Fig. 3 Narrow-band receiver using TDA3048.

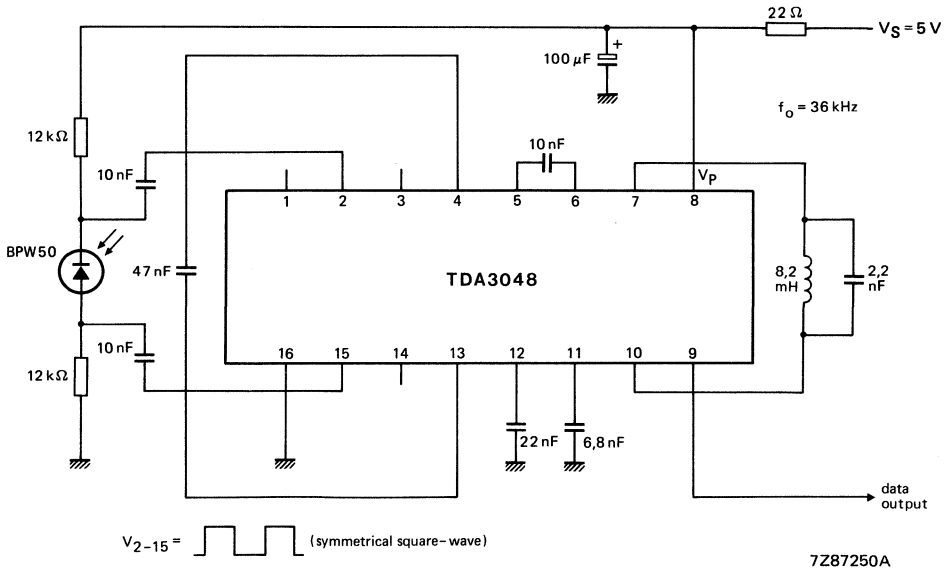


Fig. 4 Wide-band receiver with TDA3048.
For better sensitivity both 12 kΩ resistors may have a higher value.

VIDEO CONTROL COMBINATION

The TDA3501 is a monolithic integrated circuit performing the control functions in a PAL/SECAM decoder which additionally comprises the integrated circuits TDA3510 (PAL decoder) and/or TDA3520 (SECAM decoder).
The required input signals are: luminance and colour difference −(R-Y) and −(B-Y), while linear RGB signals can be inserted from an external source.
RGB signals are provided at the output to drive the video output stages.
The TDA3501 has the following features:

- capacitive coupling of the input signals
- linear saturation control
- (G-Y) and RGB matrix
- insertion possibility of linear RGB signals, e.g. video text, video games, picture-in-picture, camera or slide-scanner
- equal black level for inserted and matrixed signals by clamping
- 3 identical channels for the RGB signals
- linear contrast and brightness control, operating on both the inserted and matrixed RGB signals
- horizontal and vertical blanking (black and ultra-black respectively) and black-level clamping obtained via a 3-level sandcastle pulse
- differential amplifiers with feedback-inputs for stabilization of the RGB output stages
- 2 d.c. gain controls for the green and blue output signals (white point adjustment)
- beam current limiting possibility

QUICK REFERENCE DATA

Supply voltage	$V_{6\text{-}24}$	typ.	12 V
Supply current	I_6	typ.	100 mA
Luminance input signal (peak-to-peak value)	$V_{15\text{-}24(p\text{-}p)}$	typ.	0,45 V
Luminance input resistance	$R_{15\text{-}24}$	typ.	12 kΩ
Colour difference input signals (peak-to-peak values)			
−(B-Y)	$V_{18\text{-}24(p\text{-}p)}$	typ.	1,33 V
−(R-Y)	$V_{17\text{-}24(p\text{-}p)}$	typ.	1,05 V
Inserted RGB signals (peak-to-peak values)	$V_{12,13,14\text{-}24(p\text{-}p)}$	typ.	1 V
Three-level sandcastle pulse detector	$V_{10\text{-}24}$	typ.	2,5/4,5/8,0 V
Control voltage ranges			
brightness	$V_{20\text{-}24}$		1 to 3 V
contrast	$V_{19\text{-}24}$		2 to 4 V
saturation	$V_{16\text{-}24}$		2,1 to 4 V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

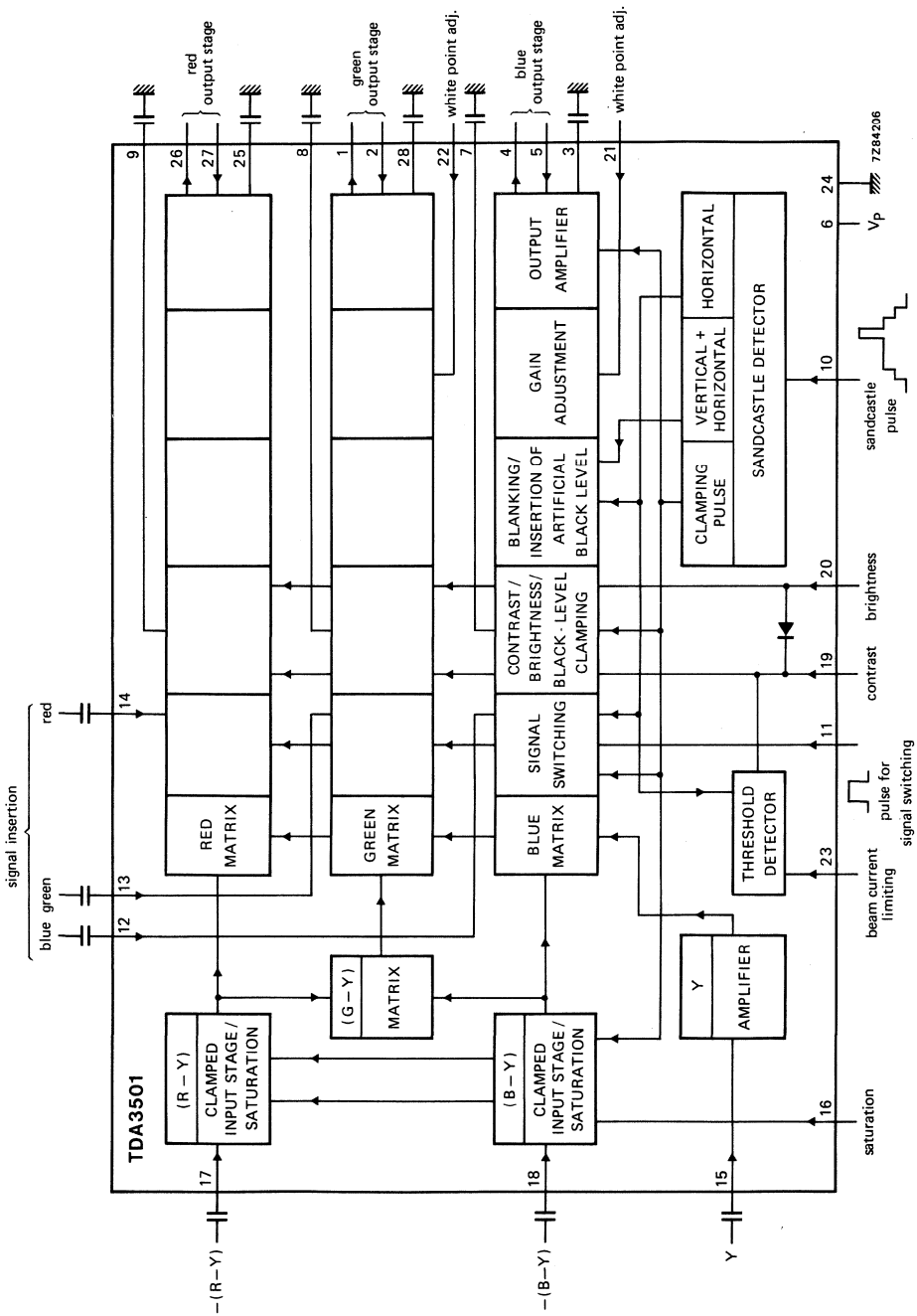


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			min.	max.	
Supply voltage	$V_P = V_{6-24}$		–	13,2	V
Voltages with respect to pin 24					
pins 1,4,26	$V_{1,4,26-24}$		½V_P	V_P + 1	V
pins 2,5,27	$V_{2,5,27-24}$		0	V_P	V
pin 10	V_{10-24}		0	V_P	V
pin 11	V_{11-24}		–0,5	3	V
pins 16,19,20	$V_{16,19,20-24}$		0	½V_P	V
pins 21,22	$V_{21,22-24}$		0	V_P	V
pin 23	V_{23-24}		0	V_P	V
pins 3,25,28; 7,8,9; 12,13,14; 15,17,18	no external d.c. voltage				
Current at pin 20	I_{20}	max.		5	mA
Total power dissipation	P_{tot}	max.		1,7	W
Storage temperature	T_{stg}			–25 to + 125	°C
Operating ambient temperature	T_{amb}			0 to + 70	°C

CHARACTERISTICS

Supply voltage range	V_P		10,8 to 13,2	V
The following characteristics are measured in Fig. 2; V_P = 12 V; T_{amb} = 25 °C; $V_{18-24(p-p)}$ = 1,33 V; $V_{17-24(p-p)}$ = 1,05 V; $V_{15-24(p-p)}$ = 0,45 V; $V_{12,13,14-24(p-p)}$ = 1 V; unless otherwise specified				
Current consumption	I_6	typ.	100	mA
Colour difference inputs				
–(B-Y) input signal (peak-to-peak value)*	$V_{18-24(p-p)}$		1,33	V
–(R-Y) input signal (peak-to-peak value)*	$V_{17-24(p-p)}$		1,05	V
Internal resistance of colour difference sources		<	200	Ω
Input resistance	$R_{17,18-24}$	>	100	kΩ
Internal d.c. voltage due to clamping	$V_{17,18-24}$	typ.	4,2	V
Saturation control				
control voltage range for a change of saturation from –20 dB to + 6 dB	V_{16-24}		2,1 to 4	V
control voltage for attenuation > 40 dB	V_{16-24}	<	1,8	V
nominal saturation (6 dB below max.)	V_{16-24}	typ.	3	V
input current	I_{16}	<	20	μA

* For saturated colour bar with 75% of maximum amplitude.

CHARACTERISTICS (continued)

(G-Y) matrix

Matrixed according the equation	$V_{(G-Y)} = -0{,}51\ V_{(R-Y)} - 0{,}19\ V_{(B-Y)}$		

Luminance amplifier

Input signal (peak-to-peak)	$V_{15\text{-}24(p\text{-}p)}$		0,45 V
Input resistance	$R_{15\text{-}24}$	typ.	12 kΩ
Internal d.c. voltage	$V_{15\text{-}24}$	typ.	2,7 V

RGB channels

Signal switching input voltage for insertion			
on level	$V_{11\text{-}24}$		0,9 to 1,5 V
off level	$V_{11\text{-}24}$		−0,5 to + 0,3 V
Input current	I_{11}		−100 to + 200 μA
Signal insertion			
external RGB input signal (peak-to-peak value)*	$V_{12,13,14\text{-}24(p\text{-}p)}$		1 V
internal d.c. voltage due to clamping	$V_{12,13,14\text{-}24}$	typ.	3,5 V
input current	$I_{12,13,14}$	<	5 μA
Contrast control			
control voltage range for a change of contrast from −17 dB to + 3 dB	$V_{19\text{-}24}$		2 to 4 V
nominal contrast (3 dB below max.)	$V_{19\text{-}24}$	typ.	3,4 V
control voltage for −6 dB	$V_{19\text{-}24}$	typ.	2,7 V
input current at $V_{23\text{-}24} \geqslant 6$ V	I_{19}	<	2,5 μA
Beam current limiting			
internal d.c. voltage	$V_{23\text{-}24}$	typ.	6 V
input resistance	$R_{23\text{-}24}$	typ.	10 kΩ
input current contrast control			
$V_{23\text{-}24} = 5{,}8$ V	I_{19}	typ.	0,7 mA
$V_{23\text{-}24} = 5{,}7$ V	I_{19}	typ.	10 mA
$V_{23\text{-}24} = 5{,}6$ V	I_{19}	typ.	16 mA
Brightness control			
control voltage range	$V_{20\text{-}24}$		1 to 3 V
nominal brightness voltage	$V_{20\text{-}24}$		2 V
input current	I_{20}	<	10 μA
control voltage for nominal black level which equals the inserted artificial black level	$V_{20\text{-}24}$	typ.	2 V
change of black level in the control range related to the nominal luminance signal (black-white)		typ.	± 50 %

* During the clamping time (see sandcastle detector Fig. 1), the inserted RGB signals are clamped to the same black level as the internal RGB signals. For proper clamping, the internal resistance of the external signal sources should be < 200 Ω.

Internal signal limiting*				
signal limiting for nominal luminance (black to white = 100%)				
black		typ.	−25	%
white		typ.	125	%
White point adjustment				
A.C. voltage gain **				
at $V_{21,22\text{-}24}$ = 6 V			100	%
at $V_{21,22\text{-}24}$ = 0 V		<	60	%
at $V_{21,22\text{-}24}$ = 12 V		>	140	%
Input resistance	$R_{21,22\text{-}24}$	typ.	20	kΩ
Differential output amplifier				
Feedback inputs (pins 2,5,27)				
d.c. voltage during clamping	$V_{2,5,27\text{-}24}$	5,79 to 5,95		V
voltage difference between the feedback inputs	ΔV	<	80	mV
input resistance	$R_{2,5,27\text{-}24}$	>	100	kΩ
Output amplifiers (pins 1,4,26) transconductance	$\frac{\Delta I_1}{\Delta V_{2\text{-}24}} = \frac{\Delta I_4}{\Delta V_{5\text{-}24}} = \frac{\Delta I_{26}}{\Delta V_{27\text{-}24}}$	typ.	20	mA/V
integrated load resistance	$R_{1,4,26\text{-}24}$	typ.	610	Ω
output current (peak value) at $V_{1,4,26\text{-}24}$ = 8,2 V	$\pm I_{1,4,26\ m}$	typ.	5	mA
Gain data				
At nominal contrast, saturation and white point adjustment				
Voltage gain between Y-input (pin 15) and feedback inputs (pins 2,5,27)	$G_{2,5,27\text{-}15}$	typ.	10	dB
Frequency response (0 to 5 MHz)	$d_{2,5,27\text{-}15}$	<	3	dB
Voltage gain between colour difference inputs (pins 17 and 18) and feedback inputs (pin 5 and 27)	$G_{5\text{-}18} = G_{27\text{-}17}$	typ.	0	dB
Frequency response (0 to 2 MHz)	$d_{5\text{-}18} = d_{27\text{-}17}$	<	3	dB
Voltage gain between signal display inputs (pins 12,13,14) and feedback inputs (pins 2,5,27)	$G_{2\text{-}13} = G_{5\text{-}12} = G_{27\text{-}14}$	typ.	0	dB
Frequency response (0 to 5 MHz)	$d_{2\text{-}13} = d_{5\text{-}12} = d_{27\text{-}14}$	<	3	dB

* Brightness, contrast and saturation control in nominal position.

** With input pins 21 and 22 not connected an internal bias voltage of 6 V is supplied.

CHARACTERISTICS (continued)

Sandcastle detector

There are 3 internal thresholds (proportional to V_P) the following amplitudes are required for separating the various pulses:

horizontal and vertical blanking pulses (note 1)	V_{10-24}	$>$	2 V
		$<$	3 V
horizontal pulse (note 2)	V_{10-24}	$>$	4 V
		$<$	5 V
clamping pulse (note 3)	V_{10-24}	$>$	7,5 V
d.c. voltage for artificial black level (note 4) (scan and flyback)	V_{10-24}	$>$	7,5 V
no keying	V_{10-24}	$<$	1 V
Input current	$-I_{10}$	$<$	100 μA

Notes

1. Blanking to ultra-black (−20%).
2. Insertion of artificial black level.
3. Pulse duration $>$ 3,5 μs.
4. This function will also be obtained by leaving pin 10 open.

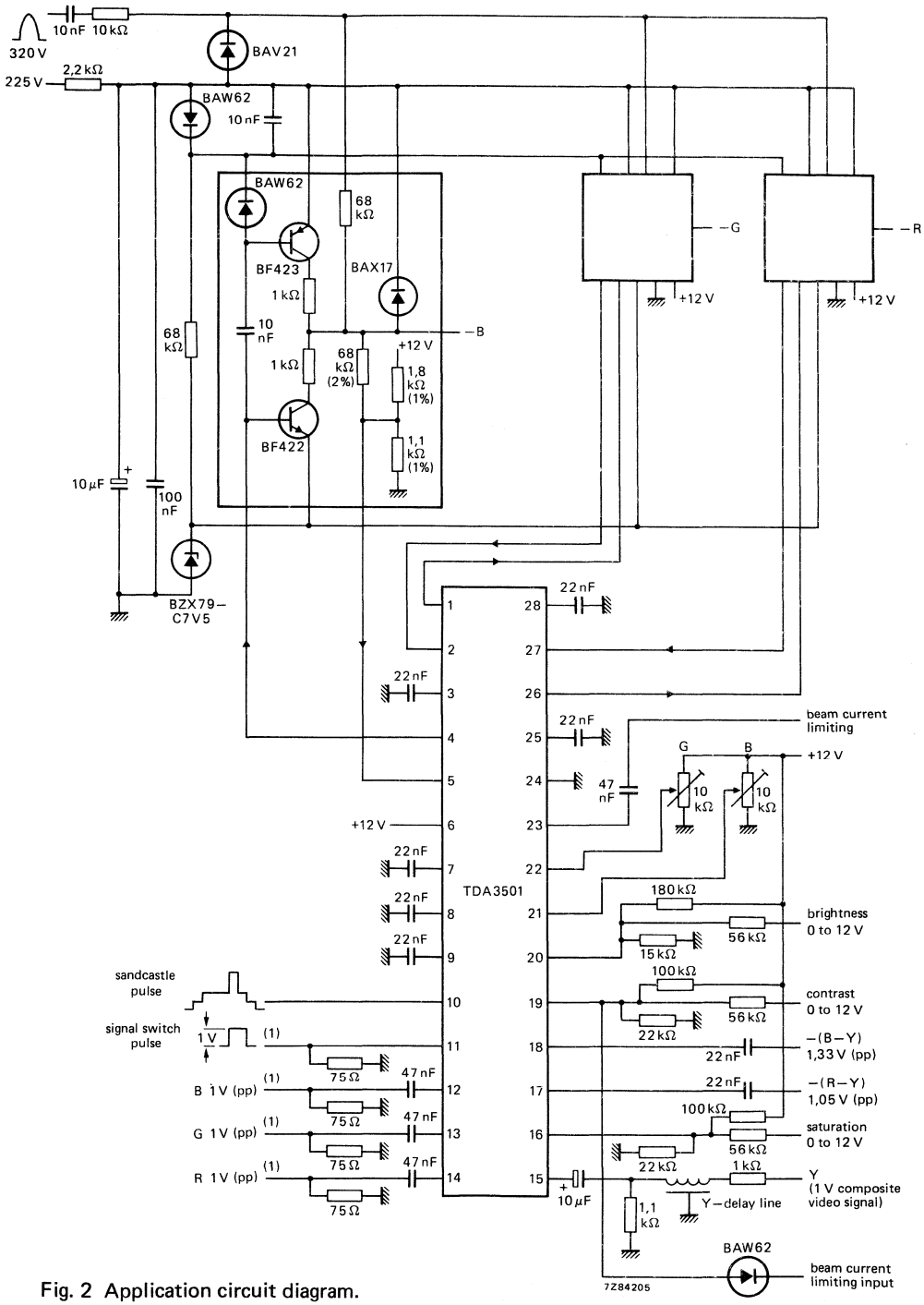


Fig. 2 Application circuit diagram.

VIDEO CONTROL COMBINATION CIRCUIT

WITH AUTOMATIC CUT-OFF CONTROL

GENERAL DESCRIPTION

The TDA3505 and TDA3506 are monolithic integrated circuits which perform video control functions in a PAL/SECAM decoder. The TDA3505 is for negative colour difference signals −(R-Y), −(B-Y) and the TDA3506 is for positive colour difference signals +(R-Y), +(B-Y).

The required input signals are: luminance and colour difference (negative or positive) and a 3-level sandcastle pulse for control purposes. Linear RGB signals can be inserted from an external source. RGB output signals are available for driving the video output stages. The circuits provide automatic cut-off control of the picture tube.

Features

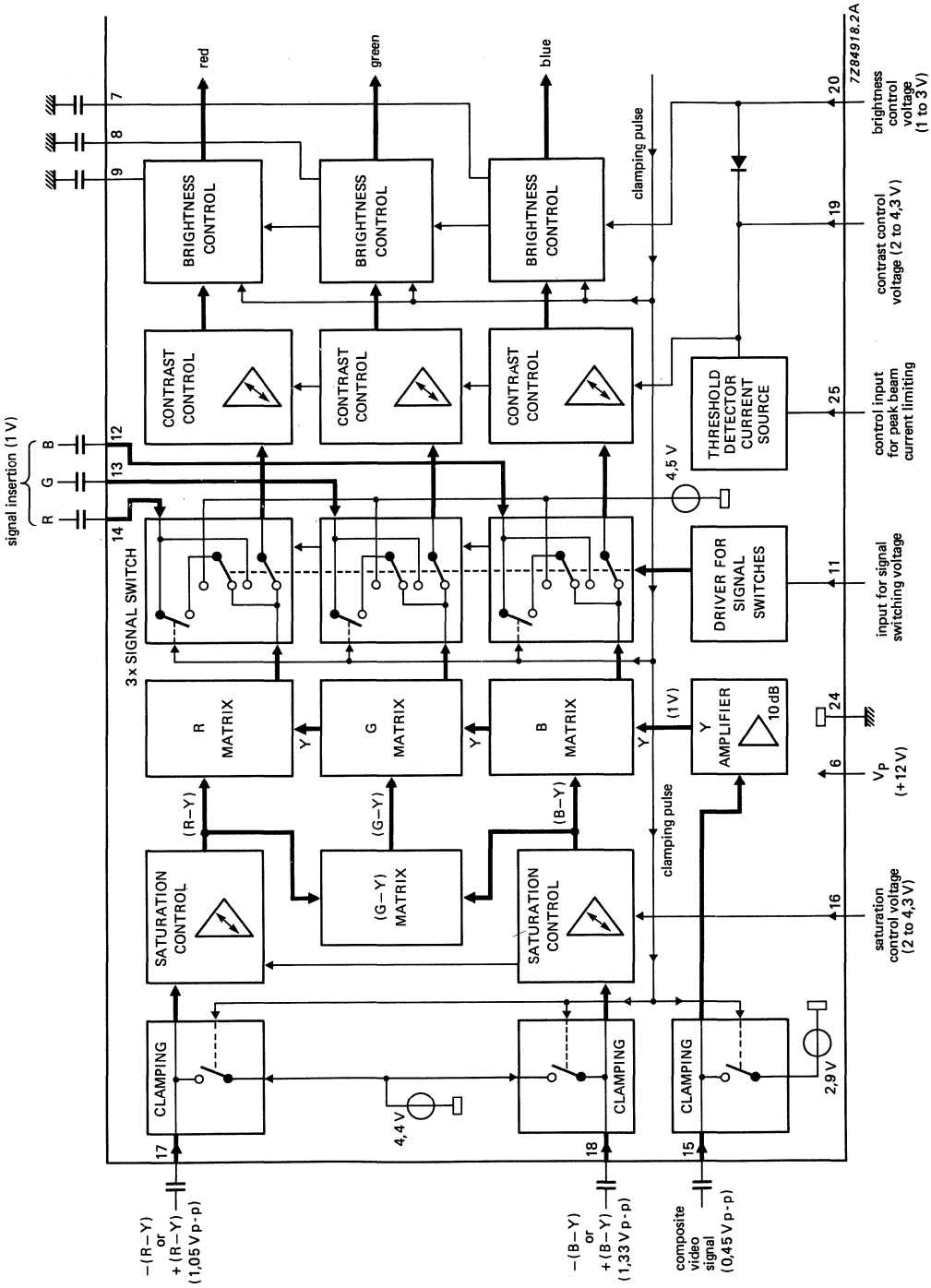
- Capacitive coupling of the colour difference and luminance input signals with black level clamping in the input stages
- Linear saturation control acting on the colour difference signals
- (G-Y) and RGB matrix
- Linear transmission of inserted signals
- Equal black levels for inserted and matrixed signals
- 3 identical channels for the RGB signals
- Linear contrast and brightness controls, operating on both the inserted and matrixed RGB signals
- Peak beam current limiting input
- Clamping, horizontal and vertical blanking of the three input signals controlled by a 3-level sandcastle pulse
- 3 DC gain controls for the RGB output signals (white point adjustment)
- Emitter-follower outputs for driving the RGB output stages
- Input for automatic cut-off control with compensation for leakage current of the picture tube

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 6)		$V_P = V_{6-24}$	–	12	–	V
Supply current		$I_P = I_6$	–	95	–	mA
Composite video input signal (peak-to-peak value)		$V_{15-24(p-p)}$	–	0,45	–	V
Colour difference input signals (peak-to-peak value)						
−(B-Y) or +(B-Y) respectively		$V_{18-24(p-p)}$	–	1,33	–	V
−(R-Y) or +(R-Y) respectively		$V_{17-24(p-p)}$	–	1,05	–	V
Inserted RGB signals (black-to-white value)		$V_{12, 13, 14-24}$	–	1,0	–	V
Three-level sandcastle pulse		V_{10-24}	–	2,5	–	V
			–	4,5	–	V
			–	8,0	–	V
Control voltage ranges						
brightness		V_{20-24}	1,0	–	3,0	V
contrast		V_{19-24}	2,0	–	4,3	V
saturation		V_{16-24}	2,0	–	4,3	V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).



Note Colour difference inputs are negative for TDA3505 or positive for TDA3506.

Fig. 1a Part of block diagram; continued in Fig. 1b.

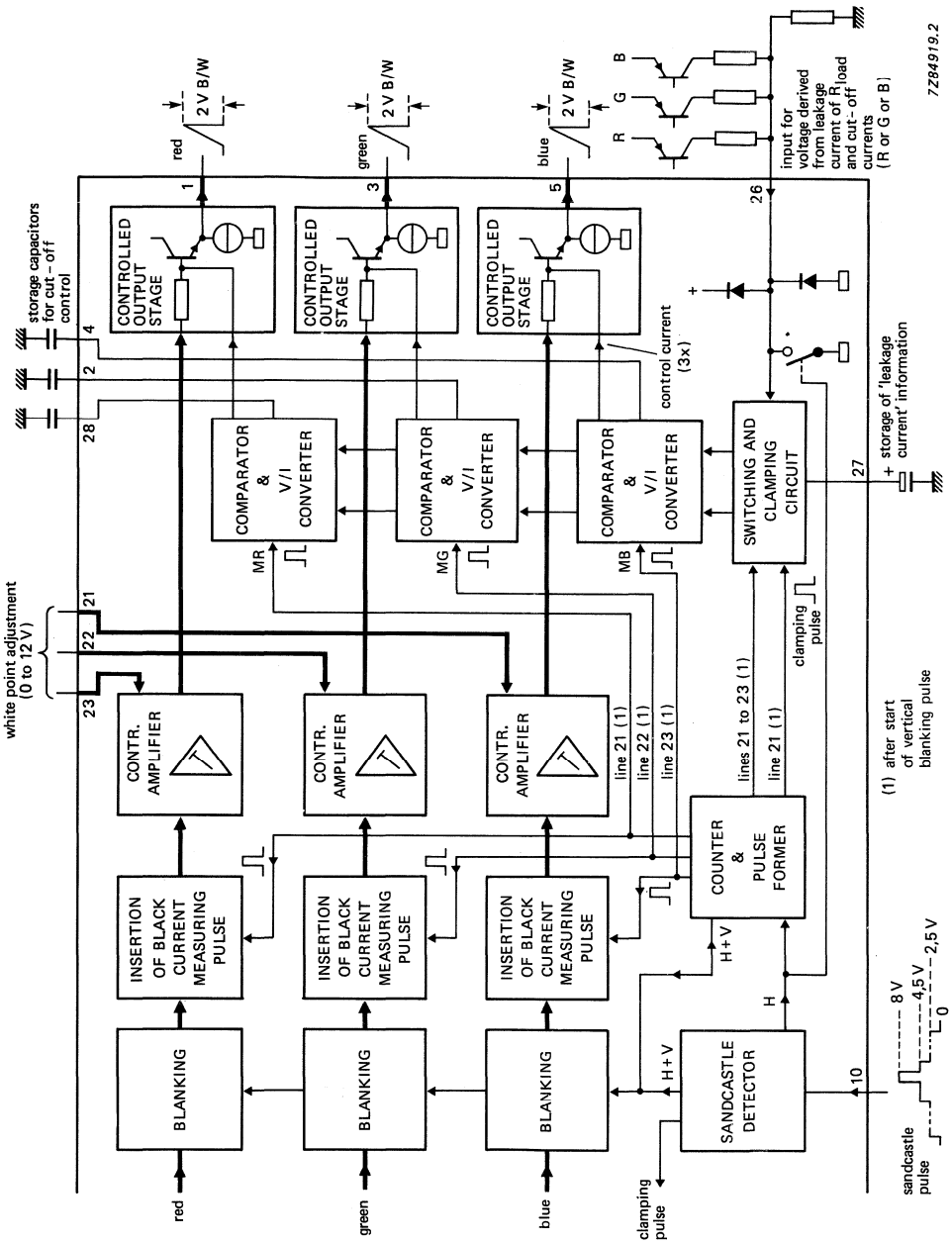


Fig. 1b Part of block diagram; continued from Fig. 1a.

PINNING

pin	description
1	red output
2	green storage capacitor for cut-off control
3	green output
4	blue storage capacitor for cut-off control
5	blue output
6	positive supply voltage (+12 V)
7	blue storage for brightness
8	green storage for brightness
9	red storage for brightness
10	sandcastle pulse input
11	fast switch for RGB inputs
12	blue input (external signal)
13	green input (external signal)
14	red input (external signal)
15	luminance input
16	saturation control input
17	colour difference input −(R-Y) or +(R-Y) respectively
18	colour difference input −(B-Y) or +(B-Y) respectively
19	contrast control input
20	brightness control input
21	white point adjustment, blue
22	white point adjustment, green
23	white point adjustment, red
24	ground (0 V)
25	control input for peak beam current limiting
26	automatic cut-off control input
27	storage capacitor for leakage current
28	red storage capacitor for cut-off control

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 6)	$V_P = V_{6-24}$	–	13,2	V
Voltage ranges				
at pins 10, 21, 22, 23, 25, 26	V_{n-24}	0	V_P	V
at pin 11	V_{11-24}	−0,5	3,0	V
at pins 16, 19, 20	$V_{16, 19, 20-24}$	0	$0{,}5V_P$	V
at pins 1, 2, 3, 4, 5, 7, 8, 9, 12, 13, 14, 15, 17, 18, 27, 28	no external DC voltage			
Currents				
at pins 1, 3, 5	$-I_{1, 3, 5}$	–	3	mA
at pin 19	I_{19}	–	10	mA
at pin 20	I_{20}	–	5	mA
at pin 25	$-I_{25}$	–	5	mA
Total power dissipation	P_{tot}	–	1,7	W
Storage temperature range	T_{stg}	−25	+150	°C
Operating ambient temperature range	T_{amb}	0	+70	°C

CHARACTERISTICS

$V_P = V_{6-24}$ = 12,0 V; $V_{12, 13, 14(p-p)}$ = 1,0 V; $V_{15-24(p-p)}$ = 0,45 V; $V_{17-24(p-p)}$ = 1,05 V; $V_{18-24(p-p)}$ = 1,33 V; T_{amb} = 25 °C; measured in Fig. 2; nominal settings of brightness, contrast, saturation and white point adjustment; all voltages are referred to pin 24; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply (pin 6)						
Supply voltage		$V_P = V_6$	10,8	12,0	13,2	V
Supply current		I_P	–	95	125*	mA
Colour difference inputs (pins 17, 18)						
(R-Y) input signal (pin 17) (peak-to-peak value)	for saturated colour bar with 75% of maximum amplitude	$V_{17(p-p)}$	–	1,05	1,48	V
(B-Y) input signal (pin 18) (peak-to-peak value)	for saturated colour bar with 75% of maximum amplitude	$V_{18(p-p)}$	–	1,33	1,88	V
Input current during scanning		$I_{17, 18}$	–	–	1,0	μA
Input resistance		$R_{17, 18-24}$	1,0	–	–	MΩ
Internal DC voltage due to clamping	note 1	$V_{17, 18}$	3,8	4,4	4,8	V
Saturation control (pin 16)						
Control voltage for maximum saturation	note 1	V_{16}	4,0	4,2	4,4	V
Control voltage for nominal saturation	6 dB below max. note 1	V_{16}	2,9	3,1	3,3	V
Control voltage for –26 dB saturation referred to maximum	note 1	V_{16}	1,9	2,1	2,3	V
Minimum saturation	V_{16} = 1,8 V	d	46	50	–	dB
Input current		I_{16}	–	–	20	μA
(G-Y) matrix						
Matrixed according to the equation $V_{(G-Y)} = -0{,}51\ V_{(R-Y)} - 0{,}19\ V_{(B-Y)}$						
Luminance input (pin 15)						
Composite video input signal (peak-to-peak value)		$V_{15(p-p)}$	–	450	630	mV
Input resistance		R_{15-24}	100	–	–	kΩ

* < 110 mA after warm-up.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Luminance input (continued)						
Input capacitance		$C_{15\text{-}24}$	–	–	5	pF
Input current during scanning		I_{15}	–	–	1	μA
Linearity	nominal settings	m	0,85	–	–	
Internal DC voltage due to clamping	note 1	V_{15}	2,5	2,9	3,3	V
RGB channels						
Signal switching input (pin 11)						
Normal state; no insertion		V_{11}	0	–	0,4	V
Level for insertion-on		V_{11}	0,9	–	3,0	V
Input capacitance		$C_{11\text{-}24}$	–	–	10	pF
Input current	V_{11} = 0 to 3 V	I_{11}	−100	–	+450	μA
Signal insertion (pins 12, 13, 14)						
External RGB input signals (black-to-white value)		$V_{12, 13, 14}$	–	1,0	1,4	V
Input current during scanning		$I_{12, 13, 14}$	–	–	1,0	μA
Internal DC voltage due to clamping	notes 1, 2	$V_{12, 13, 14}$	4,0	4,5	5,0	V
Contrast control (pin 19)	note 1					
Control voltage for maximum contrast		V_{19}	4,0	4,2	4,4	V
Control voltage for nominal contrast	3 dB below max.	V_{19}	3,4	3,6	3,8	V
Control voltage for −10 dB below max.		V_{19}	2,6	2,8	3,0	V
Minimum contrast referred to max.	V_{19} = 2 V	d	18	21	29	dB
Input current	$V_{25} > 6$ V	I_{19}	–	–	2	μA
Difference between RGB channels	contrast −10 dB below max.		–	–	0,6	dB
Peak beam current limiting (pin 25)						
Internal DC bias voltage	note 1	V_{25}	5,3	5,5	5,7	V
Input resistance		$R_{25\text{-}24}$	–	10	–	kΩ
Input current at contrast control input	V_{25} = 4,5 V	I_{19}	10	20	34	mA

parameter	conditions	symbol	min.	typ.	max.	unit
Brightness control (pin 20)	note 1					
Control voltage range		V_{20}	1	–	3	V
Input current		$-I_{20}$	–	–	10	μA
Change of black level in the control range related to the luminance signal (black/white)	$\Delta V_{20} = 1$ V		–	±50	–	%
Tracking			95	–	–	%
Internal signal limiting (RGB)						
Signal limiting referred to nominal luminance and nominal black level						
black			–	–25	–	%
white			115	120	125	%
White point adjustment (pins 21, 22, 23)	note 1					
AC voltage gain	note 3					
$V_{21, 22, 23} = 5{,}5$ V		G_V	–	100	–	%
$V_{21, 22, 23} = 0$ V		G_V	–35	–40	–	%
$V_{21, 22, 23} = 12$ V		G_V	+35	+40	–	%
Input resistance		$R_{21,22,23\text{-}24}$	–	20	–	kΩ
RGB outputs (emitter follower) (pins 1, 3, 5)						
Output voltage; black-to-white positive		$V_{1, 3, 5}$	1,5	2,0	2,5	V
Black level without automatic cut-off control	note 1; $V_{28,2,4} = 10$ V	$V_{1, 3, 5}$	6,1	6,9	7,7	V
Difference in black level between RGB channels due to variation of contrast control		$\Delta V_{1, 3, 5}$	–	–	10	mV
Cut-off control range	note 1	$V_{1, 3, 5}$	4,0	4,6	–	V
Internal current source		$I_{1, 3, 5}$	2,0	3,0	–	mA

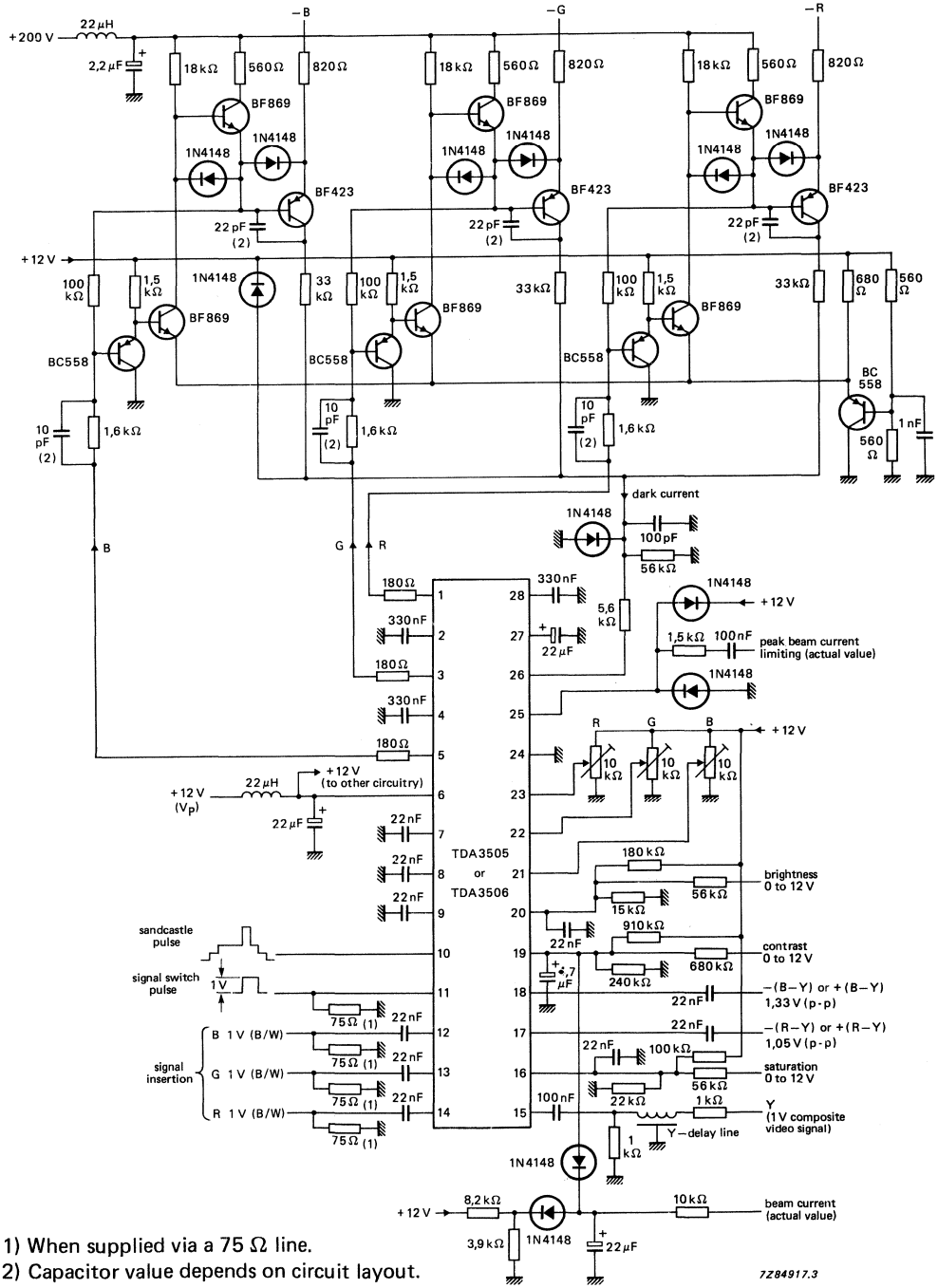
CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Automatic cut-off control (pin 26)	notes 1, 4					
Input voltage range		V_{26}	0	–	6,5	V
Voltage difference between cut-off current measurement (note 5) and leakage current measurement (note 6)		V_{26}	0,5	0,64	0,72	V
Input pin 26 switches to ground during horizontal flyback						
Gain data	at nominal brightness, contrast, saturation and white point settings					
Voltage gain with respect to luminance input (pin 15)		$G_{1,3,5\text{-}15}$	14	16	18	dB
Frequency response of luminance path	0 to 5 MHz	$d_{1,3,5\text{-}15}$	–	–	3	dB
Voltage gain with respect to colour difference inputs (pins 17 and 18)		$G_{5\text{-}18}$ $G_{1\text{-}17}$	3	6	9	dB
Frequency response of colour difference paths	0 to 2 MHz	$d_{5\text{-}18}$ $d_{1\text{-}17}$	–	–	3	dB
Voltage gain with respect to inserted signals		$G_{1\text{-}14}$ $G_{3\text{-}13}$ $G_{5\text{-}12}$	4	6	8	dB
Frequency response of inserted signal paths	0 to 10 MHz	$d_{1\text{-}14}$ $d_{3\text{-}13}$ $d_{5\text{-}12}$	–	–	3	dB
Rise and fall times of RGB output signals (pins 1, 3, 5)		t_r, t_f	–	40	–	ns
Difference in transit times between R, G and B channels		$\Delta t_{1,3,5}$	–	0	15	ns
Delay time between signal switching and signal insertion		t_d	–25	–	+25	ns
Difference in gain between normal mode and signal insertion mode		$\Delta G_{1,3,5}$	–	–	10	%

parameter	conditions	symbol	min.	typ.	max.	unit
Sandcastle pulse detector (pin 10)	note 7					
Levels for separating the following pulses:						
horizontal and vertical blanking pulses	note 8	V_{10}	1,0	1,5	2,0	V
required pulses (H+V)		V_{10}	2,1	2,5	2,9	V
horizontal pulses		V_{10}	3,0	3,5	4,0	V
required pulses (H)		V_{10}	4,1	4,5	5,0	V
clamping pulses	note 9	V_{10}	6,5	7,0	7,5	V
required pulses		V_{10}	7,6	–	12,0	V
no keying		V_{10}	–	–	1,0	V
Input current		$-I_{10}$	–	–	110	μA

Notes to the characteristics

1. Values are proportional to the supply voltage.
2. When $V_{11\text{-}24} < 0{,}4$ V during clamping time - the black levels of the inserted RGB signals are clamped on the black levels of the internal RGB signals.
   When $V_{11\text{-}24} > 0{,}9$ V during clamping time - the black levels of the inserted RGB signals are clamped on an internal DC voltage (correct clamping of the external RGB signals is possible only when they are synchronous with the sandcastle pulse).
3. When pins 21, 22 and 23 are not connected, an internal bias voltage of 5,5 V is supplied.
4. Automatic cut-off control measurement occurs in the following lines after start of the vertical blanking pulse:
   line 20: measurement of leakage current (R + G + B)
   line 21: measurement of red cut-off current
   line 22: measurement of green cut-off current
   line 23: measurement of blue cut-off current
5. Black level of the measured channel is nominal; the other two channels are blanked to ultra-black.
6. All three channels blanked to ultra-black.
   The cut-off control cycle occurs when the vertical blanking part of the sandcastle pulse contains more than 3 line pulses.
   The internal blanking continues until the end of the last measured line.
   The vertical blanking pulse is not allowed to contain more than 34 line pulses, otherwise another control cycle begins.
7. The sandcastle pulse is compared with three internal thresholds (proportional to Vp) and the given levels separate the various pulses.
8. Blanked to ultra-black (−25%).
9. Pulse duration $\geqslant 3{,}5$ μs.



(1) When supplied via a 75 Ω line.
(2) Capacitor value depends on circuit layout.

Fig. 2 Typical application circuit diagram using TDA3505 or TDA3506; colour difference inputs are negative for TDA3505 or positive for TDA3506.

VIDEO CONTROL COMBINATION CIRCUIT

WITH AUTOMATIC CUT-OFF CONTROL

GENERAL DESCRIPTION

The TDA3507 is a monolithic integrated circuit which performs video control functions in a PAL/SECAM decoder.

The required input signals are: luminance and negative colour difference −(R−Y) and −(B−Y), and a 3-level sandcastle pulse for control purposes. Linear RGB signals can be inserted from an external source. RGB output signals are available for driving the video output stages. This circuit provides automatic cut-off control of the picture tube.

The TDA3507 is the same as the TDA3505 but with RGB channel bandwidths of (typical) 16 MHz and an automatic cut-off cycle that ends in line 15.

Features

- Capacitive coupling of the colour difference and luminance input signals with black level clamping in the input stages
- Linear saturation control acting on the colour difference signals
- (G−Y) and RGB matrix
- Linear transmission of inserted signals
- Equal black levels for inserted and matrixed signals
- 3 identical channels for the RGB signals
- Linear contrast and brightness controls, operating on both the inserted and matrixed RGB signals
- Peak beam current limiting input
- Clamping, horizontal and vertical blanking of the three input signals controlled by a 3-level sandcastle pulse
- 3 DC gain controls for the RGB output signals (white point adjustment)
- Emitter-follower outputs for driving the RGB output stages
- Input for automatic cut-off control with compensation for leakage current of the picture tube

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 6)		$V_P = V_{6-24}$	–	12	–	V
Supply current		$I_P = I_6$	–	100	–	mA
Composite video input signal (peak-to-peak value)		$V_{15-24(p-p)}$	–	0,45	–	V
Colour difference input signals (peak-to-peak value)						
–(B–Y)		$V_{18-24(p-p)}$	–	1,33	–	V
–(R–Y)		$V_{17-24(p-p)}$	–	1,05	–	V
Inserted RGB signals (black-to-white value)		$V_{12,13,14-24}$	–	1,0	–	V
Three-level sandcastle pulse		V_{10-24}	–	2,5	–	V
			–	4,5	–	V
			–	8,0	–	V
Control voltage ranges						
brightness		V_{20-24}	1,0	–	3,0	V
contrast		V_{19-24}	2,0	–	4,3	V
saturation		V_{16-24}	2,0	–	4,3	V

DEVELOPMENT DATA

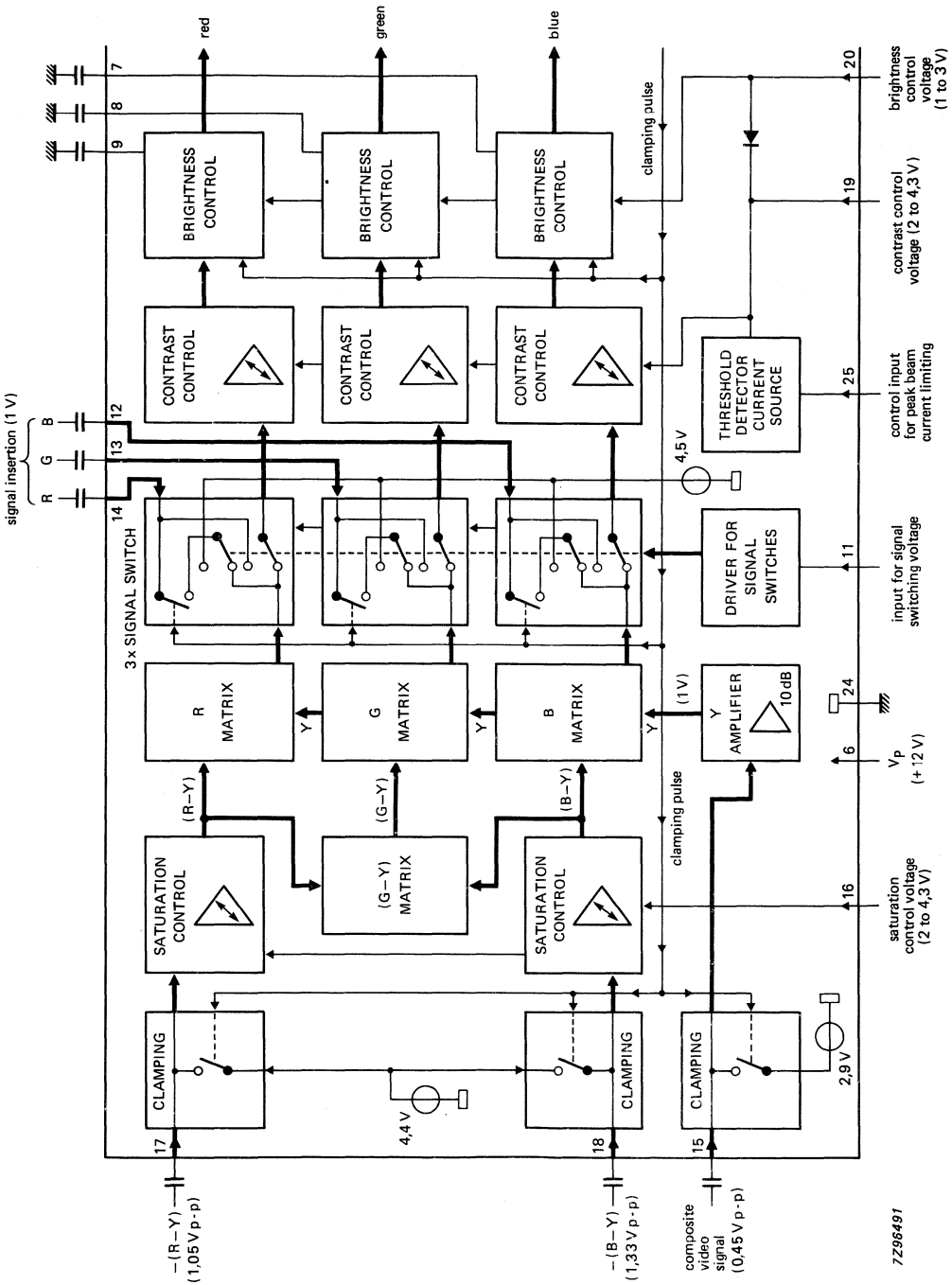


Fig. 1a Part of block diagram, continued in Fig. 1b.

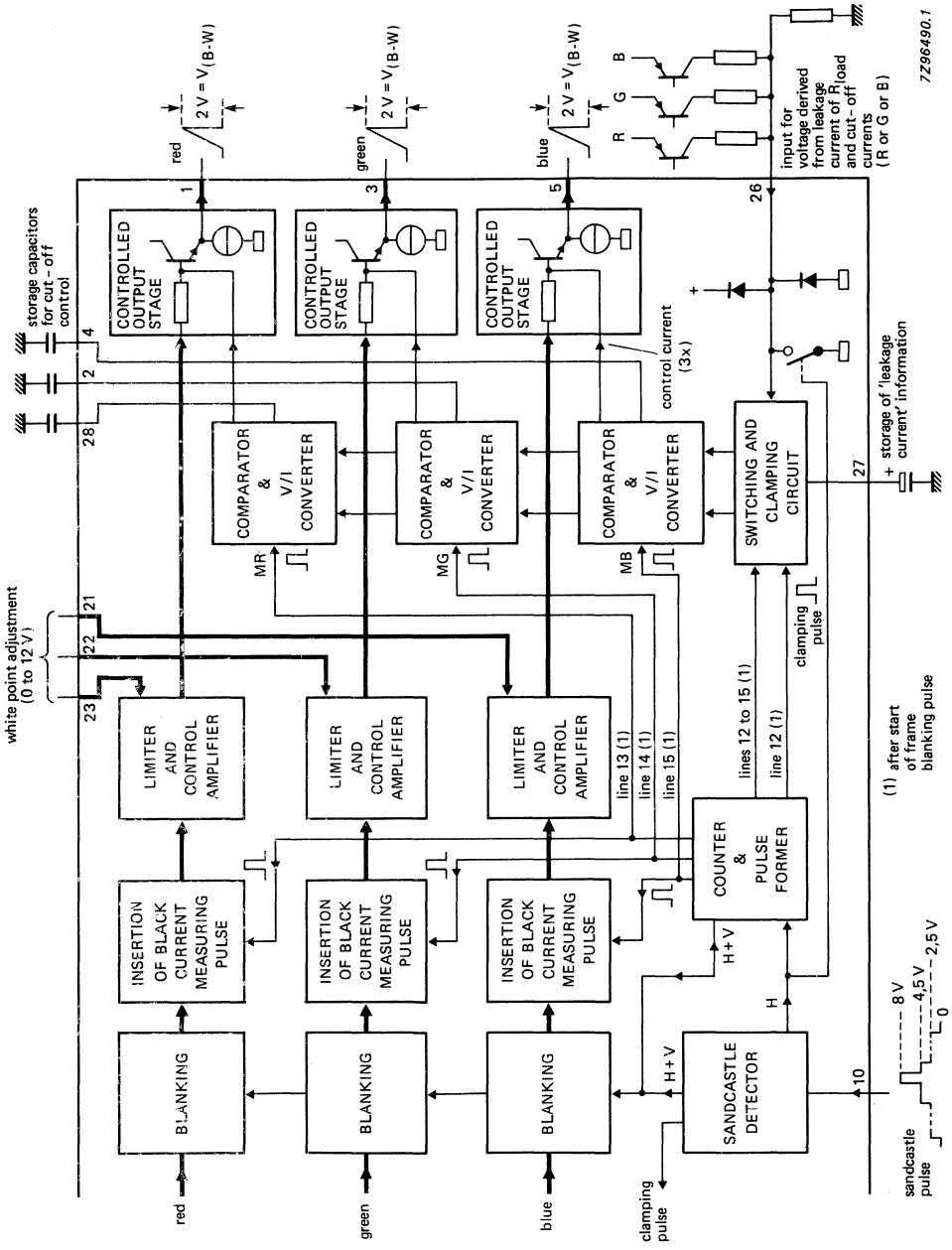


Fig. 1b Part of block diagram, continued from Fig. 1a.

DEVELOPMENT DATA

PINNING

pin	description
1	red output
2	green storage capacitor for cut-off control
3	green output
4	blue storage capacitor for cut-off control
5	blue output
6	positive supply voltage (+12 V)
7	blue storage for brightness
8	green storage for brightness
9	red storage for brightness
10	sandcastle pulse input
11	fast switch for RGB inputs
12	blue input (external signal)
13	green input (external signal)
14	red input (external signal)
15	luminance input
16	saturation control input
17	−(R−Y) colour difference input
18	−(B−Y) colour difference input
19	contrast control input
20	brightness control input
21	white point adjustment, blue
22	white point adjustment, green
23	white point adjustment, red
24	ground (0 V)
25	control input for peak beam current limiting
26	automatic cut-off control input
27	storage capacitor for leakage current
28	red storage capacitor for cut-off control

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 6)	$V_P = V_{6-24}$	–	13,2	V
Voltage ranges				
at pins 10, 21, 22, 23, 25, 26	V_{n-24}	0	V_P	V
at pin 11	V_{11-24}	−0,5	3,0	V
at pins 16, 19, 20	$V_{16,19,20-24}$	0	0,5V_P	V
at pins 1, 2, 3, 4, 5, 7, 8, 9, 12, 13, 14, 15, 17, 18, 27, 28	no external DC voltage			
Currents				
at pins 1, 3, 5	$-I_{1,3,5}$	–	3	mA
at pin 19	I_{19}	–	10	mA
at pin 20	I_{20}	–	5	mA
at pin 25	$-I_{25}$	–	5	mA
Total power dissipation	P_{tot}	–	1,7	W
Storage temperature range	T_{stg}	−25	+150	°C
Operating ambient temperature range	T_{amb}	0	+70	°C

CHARACTERISTICS

$V_P = V_{6-24} = 12{,}0$ V; $V_{12,13,14(p-p)} = 1{,}0$ V; $V_{15-24(p-p)} = 0{,}45$ V; $V_{17-24(p-p)} = 1{,}05$ V; $V_{18-24(p-p)} = 1{,}33$ V; $T_{amb} = 25\ ^{o}C$; measured in Fig. 2; nominal settings of brightness, contrast, saturation and white point adjustment; all voltages are referred to pin 24; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply (pin 6)						
Supply voltage		$V_P = V_6$	10,8	12,0	13,2	V
Supply current		I_P	–	100	130*	mA
Colour difference inputs (pins 17, 18)						
–(R–Y) input signal (pin 17) (peak-to-peak value)	for saturated colour bar with 75% of maximum amplitude	$V_{17(p-p)}$	–	1,05	1,48	V
–(B–Y) input signal (pin 18) (peak-to-peak value)	for saturated colour bar with 75% of maximum amplitude	$V_{18(p-p)}$	–	1,33	1,88	V
Input current during scanning		$I_{17,18}$	–	–	1,0	μA
Input resistance		$R_{17,18-24}$	1,0	–	–	MΩ
Internal DC voltage due to clamping	note 1	$V_{17,18}$	3,8	4,4	4,8	V
Saturation control (pin 16)						
Control voltage for maximum saturation	note 1	V_{16}	4,0	4,2	4,4	V
Control voltage for nominal saturation	6 dB below max. note 1	V_{16}	2,9	3,1	3,3	V
Control voltage for –26 dB saturation referred to maximum	note 1	V_{16}	1,9	2,1	2,3	V
Minimum saturation	$V_{16} = 1{,}8$ V	d	46	50	–	dB
Input current		I_{16}	–	–	20	μA
(G–Y) matrix						
Matrixed according to the equation $V_{(G-Y)} = -0{,}51\ V_{(R-Y)} - 0{,}19\ V_{(B-Y)}$						
Luminance input (pin 15)						
Composite video input signal (peak-to-peak value)		$V_{15(p-p)}$	–	450	630	mV
Input resistance		R_{15-24}	100	–	–	kΩ
Input capacitance		C_{15-24}	–	–	5	pF

* < 115 mA after warm-up

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Luminance input (continued)						
Input current during scanning		I_{15}	–	–	1	μA
Linearity	nominal settings	m	0,85	–	–	
Internal DC voltage due to clamping	note 1	V_{15}	2,5	2,9	3,3	V
RGB channels						
Signal switching input (pin 11)						
Normal state; no insertion		V_{11}	0	–	0,4	V
Level for insertion-on		V_{11}	0,9	–	3,0	V
Input capacitance		$C_{11\text{-}24}$	–	–	10	pF
Input current	V_{11} = 0 to 3 V	I_{11}	−100	–	+450	μA
Signal insertion (pins 12, 13, 14)						
External RGB input signals (black-to-white value)		$V_{12,13,14}$	–	1,0	1,4	V
Input current during scanning		$I_{12,13,14}$	–	–	1,0	μA
Internal DC voltage due to clamping	notes 1, 2	$V_{12,13,14}$	4,0	4,5	5,0	V
Contrast control (pin 19)	note 1					
Control voltage for maximum contrast		V_{19}	4,0	4,2	4,4	V
Control voltage for nominal contrast	3 dB below max.	V_{19}	3,4	3,6	3,8	V
Control voltage for −10 dB below max.		V_{19}	2,6	2,8	3,0	V
Minimum contrast referred to max.	V_{19} = 2 V	d	18	21	29	dB
Input current	$V_{25} > 6$ V	I_{19}	–	–	2	μA
Difference between RGB channels	contrast −10 dB below max.		–	–	0,6	dB
Peak beam current limiting (pin 25)						
Internal DC bias voltage	note 1	V_{25}	5,3	5,5	5,7	V
Input resistance		$R_{25\text{-}24}$	–	10	–	kΩ
Input current at contrast control input	V_{25} = 4,5 V	I_{19}	10	20	34	mA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Brightness control (pin 20)	note 1					
Control voltage range		V_{20}	1	–	3	V
Input current		$-I_{20}$	–	–	10	μA
Change of black level in the control range related to the luminance signal (black/white)	ΔV_{20} = 1 V		–	±50	–	%
Tracking			95	–	–	%
Internal signal limiting (RGB)						
Signal limiting referred to nominal luminance and nominal black level						
black			–	–25	–	%
white			115	120	125	%
White point adjustment (pins 21, 22, 23)	note 1					
AC voltage gain	note 3					
$V_{21,22,23}$ = 5,5 V		G_V	–	100	–	%
$V_{21,22,23}$ = 0 V		G_V	–35	–40	–	%
$V_{21,22,23}$ = 12 V		G_V	+35	+40	–	%
Input resistance		$R_{21,22,23\text{-}24}$	–	20	–	kΩ
RGB outputs (emitter follower) (pins 1, 3, 5)						
Output voltage; black-to-white positive		$V_{1,3,5}$	1,5	2,0	2,5	V
Black level without automatic cut-off control	note 1; $V_{28,2,4}$ = 10 V	$V_{1,3,5}$	6,1	6,9	7,7	V
Difference in black level between RGB channels due to variation of contrast control		$\Delta V_{1,3,5}$	–	–	10	mV
Cut-off control range	note 1	$V_{1,3,5}$	4,0	4,6	–	V
Internal current source		$I_{1,3,5}$	2,0	3,0	–	mA

parameter	conditions	symbol	min.	typ.	max.	unit
Automatic cut-off control (pin 26)	notes 1,4					
Input voltage range		V_{26}	0	–	6,5	V
Voltage difference between cut-off current measurement (note 5) and leakage current measurement (note 6)		V_{26}	0,5	0,64	0,72	V
Input pin 26 switches to ground during horizontal flyback						
Gain data	at nominal brightness, contrast, saturation and white point settings					
Voltage gain with respect to luminance input (pin 15)		$G_{1,3,5\text{-}15}$	14	16	18	dB
Frequency response of luminance path	0 to 5 MHz	$d_{1,3,5\text{-}15}$	–	–	3	dB
Voltage gain with respect to colour difference inputs (pins 17 and 18)		$G_{5\text{-}18}$ $G_{1\text{-}17}$	3	6	9	dB
Frequency response of colour difference paths	0 to 2 MHz	$d_{5\text{-}18}$ $d_{1\text{-}17}$	–	–	3	dB
Voltage gain with respect to inserted signals		$G_{1\text{-}14}$ $G_{3\text{-}13}$ $G_{5\text{-}12}$	4	6	8	dB
Frequency response of inserted signal paths	0 to 16 MHz	$d_{1\text{-}14}$ $d_{3\text{-}13}$ $d_{5\text{-}12}$	–	3	–	dB
Frequency response of inserted signal paths	0 to 13 MHz	$d_{1\text{-}14}$ $d_{3\text{-}13}$ $d_{5\text{-}12}$	–	–	3	dB
Rise and fall times of RGB output signals (pins 1, 3, 5)		t_r, t_f	–	40	–	ns
Difference in transit times between R, G and B channels		$\Delta t_{1,3,5}$	–	0	15	ns

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Gain data (continued)						
Delay time between signal switching and signal insertion		t_d	−25	–	+25	ns
Difference in gain between normal mode and signal insertion mode		$\Delta G_{1,3,5}$	–	–	10	%
Sandcastle pulse detector (pin 10)	note 7					
Levels for separating the following pulses:						
horizontal and vertical blanking pulses	note 8	V_{10}	1,0	1,5	2,0	V
required pulses (H+V)		V_{10}	2,1	2,5	2,9	V
horizontal pulses		V_{10}	3,0	3,5	4,0	V
required pulses (H)		V_{10}	4,1	4,5	5,0	V
clamping pulses	note 9	V_{10}	6,5	7,0	7,5	V
required pulses		V_{10}	7,6	–	12,0	V
no keying		V_{10}	–	–	1,0	V
Input current		$-I_{10}$	–	–	110	μA

Notes to the characteristics

1. Values are proportional to the supply voltage.
2. When $V_{11\text{-}24} < 0{,}4$ V during clamping time – the black levels of the inserted RGB signals are clamped on the black levels of the internal RGB signals.

   When $V_{11\text{-}24} > 0{,}9$ V during clamping time – the black levels of the inserted RGB signals are clamped on an internal DC voltage (correct clamping of the external RGB signals is possible only when they are synchronous with the sandcastle pulse).
3. When pins 21, 22 and 23 are not connected, an internal bias voltage of 5,5 V is supplied.
4. Automatic cut-off control measurement occurs in the following lines after start of the vertical blanking pulse:

   line 12: measurement of leakage current (R + G + B)
   line 13: measurement of red cut-off current
   line 14: measurement of green cut-off current
   line 15: measurement of blue cut-off current
5. Black level of the measured channel is nominal; the other two channels are blanked to ultra-black.
6. All three channels blanked to ultra-black.

   The cut-off control cycle occurs when the vertical blanking part of the sandcastle pulse contains more than 3 line pulses.

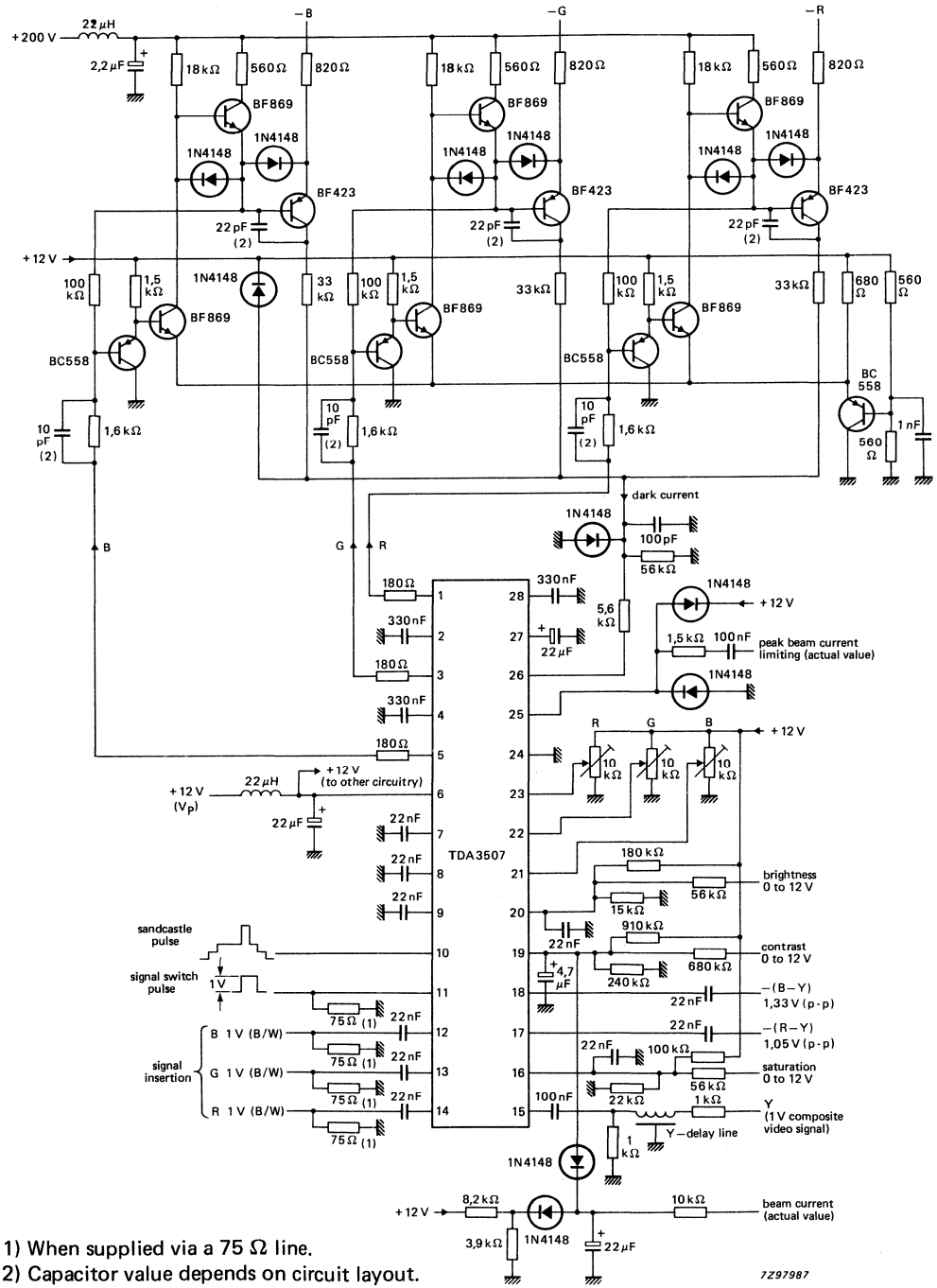
   The internal blanking continues until the end of the last measured line.

   The vertical blanking pulse is not allowed to contain more than 34 line pulses, otherwise another control cycle begins.

7. The sandcastle pulse is compared with three internal thresholds (proportional to Vp) and the given levels separate the various pulses.
8. Blanked to ultra-black (−25%).
9. Pulse duration $\geqslant 3{,}5\ \mu s$.

DEVELOPMENT DATA

APPLICATION INFORMATION



(1) When supplied via a 75 Ω line.
(2) Capacitor value depends on circuit layout.

Fig. 2 Typical application circuit diagram using the TDA3507.

PAL DECODER

The TDA3510 is a monolithic integrated colour decoder for the PAL standard.
The circuit incorporates the following functions:

Chrominance part

- Controlled chrominance amplifier
- Chrominance output stage with automatic standard switch for driving the 64 μs delay line
- Blanking circuit for the colour burst signal

Reference voltage and control voltage part

- 8,8 MHz reference oscillator with divider stage to obtain both the 4,4 MHz reference signals
- Gated phase comparison for an optimum noise ratio
- Circuit for obtaining the chrominance control voltage and a reference voltage
- Circuit for generating the colour killer signal and the identification signal

Demodulator part

- Two synchronous demodulators for the (B-Y) and (R-Y) signals
- PAL flip-flop and PAL switch
- Flyback blanking incorporated in the synchronous demodulators
- (R-Y) and (B-Y) signal output stages, which are controlled by the colour killer with switchable d.c. voltage levels

QUICK REFERENCE DATA

Supply voltage	$V_P = V_{9-24}$	typ.	12 V
Supply current	I_9	typ.	58 mA
Chrominance input signal (peak-to-peak value)	$V_{1-24(p-p)}$		10 to 200 mV
Sandcastle pulse			
burst gating level	V_{20-24}	>	7,5 V
blanking level	V_{20-24}	>	1,8 V
Colour difference output signals			
peak-to-peak values			
−(R-Y) signal	$V_{11-24(p-p)}$	typ.	1,05 V ± 3 dB
−(B-Y) signal	$V_{10-24(p-p)}$	typ.	1,33 V ± 3 dB

PACKAGE OUTLINE

24-lead DIL; plastic (SOT101A).

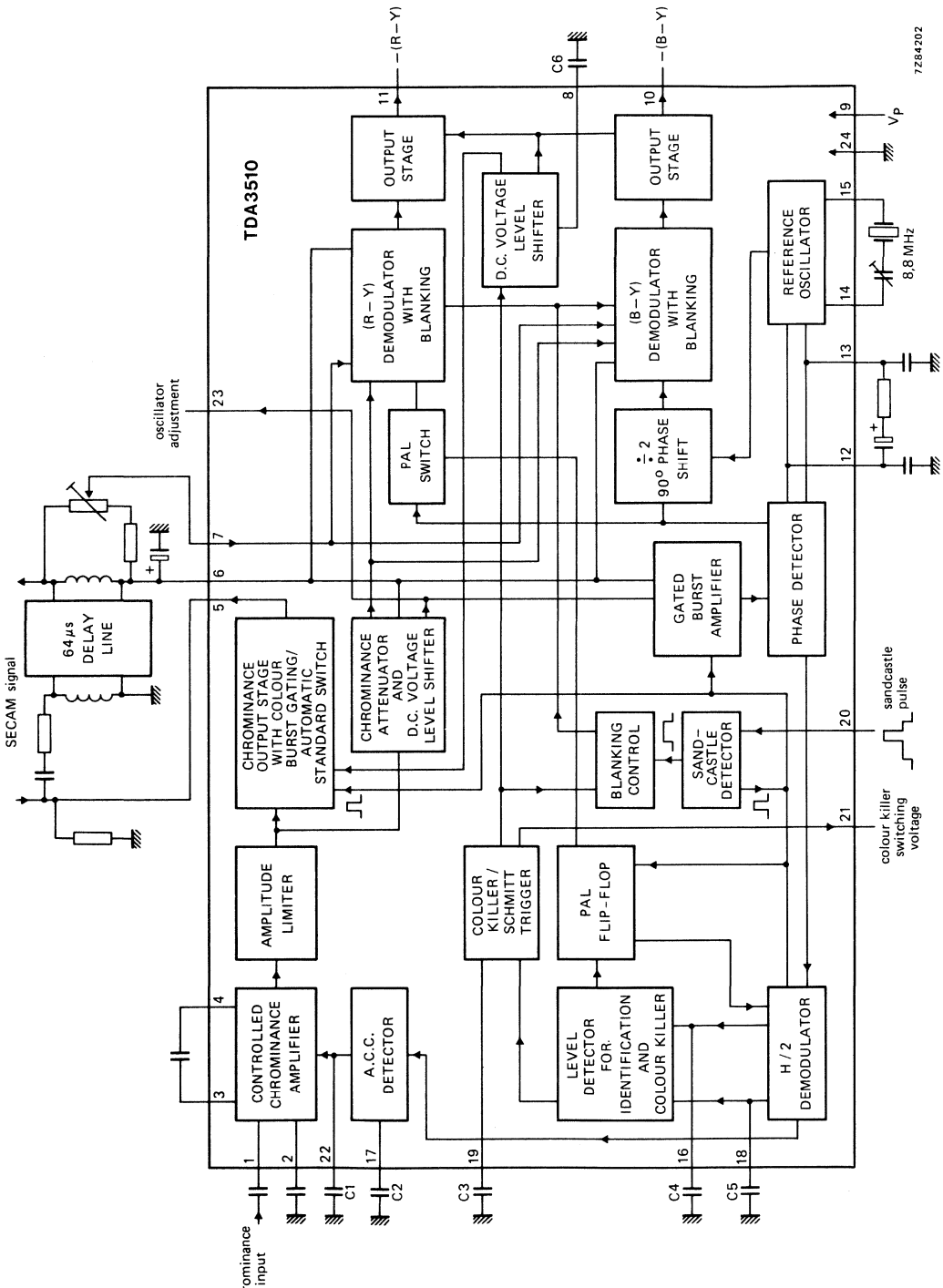


Fig. 1 Block diagram; for external capacitors see next page.

External capacitors in Fig. 1

capacitor	pins	
C1	22 – 24	filter capacitor for control voltage
C2	17 – 24	time constant for control voltage
C3	19 – 24	time constant for colour ON
C4	16 – 24	identification signal and colour OFF time constant
C5	18 – 24	load capacitor for the reference voltage
C6	8 – 24	time constant for the rise or fall time of the d.c. voltage level of the colour difference signal

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	$V_P = V_{9-24}$	10,8 to 13,2		V
Currents				
at pin 5	$-I_5$	max.	10	mA
at pins 10 and 11	$-I_{10}, -I_{11}$	max.	1	mA
at pin 21	I_{21}	max.	10	mA
Total power dissipation	P_{tot}	max.	1,1	W
Storage temperature	T_{stg}	−20 to + 125		°C
Operating ambient temperature	T_{amb}	0 to + 70		°C

CHARACTERISTICS

$V_P = 12$ V; $T_{amb} = 25$ °C

Supply current	I_9	typ.	58	mA
Chrominance part				
Chrominance signal is asymmetric (pins 1, 2)				
Input voltage range (peak-to-peak value)	$V_{1-24(p-p)}$	10 to 200		mV
Nominal input voltage (peak-to-peak value) with 75% colour bar signal	$V_{1-24(p-p)}$	typ.	100	mV
Input impedance	$\lvert Z_i \rvert$	typ.	3,3	kΩ
Colour ON				
chrominance output voltage (peak-to-peak value) with 75% colour bar signal	$V_{5-24(p-p)}$	typ.	2	V
d.c. voltage at chrominance output	V_{5-24}	typ.	8	V
Colour OFF				
chrominance suppression		>	56	dB
d.c. voltage at chrominance output	V_{5-24}	typ.	4	V

CHARACTERISTICS (continued)

Reference voltage and control voltage part

Oscillator (8,8 MHz)			
Gain	$G_{14\text{-}15}$	>	8 dB
Input resistance	$R_{15\text{-}24}$	typ.	270 Ω
Output resistance	$R_{14\text{-}24}$	<	200 Ω
Catching range	Δf	typ.	500 Hz
Sandcastle pulse (pin 20)			
Burst gating level	$V_{20\text{-}24}$	>	7,5 V
Blanking level	$V_{20\text{-}24}$	>	1,8 V
Colour switching voltage (open collector)			
Maximum output current	I_{21max}	typ.	10 mA
Colour ON	$V_{21\text{-}24}$	typ.	V_P
Colour OFF	$V_{21\text{-}24}$	<	0,5 V
Reference output voltage	$V_{18\text{-}24}$	typ.	5,5 V
Colour killer voltages			
colour OFF at	$V_{18\text{-}16}$	typ.	0 V
or at	$V_{19\text{-}24}$	>	6 V
colour ON at	$V_{18\text{-}16}$	typ.	1,5 V
or at	$V_{19\text{-}24}$	<	4 V
Colour unkill delay; depends on C3	t_d	typ.	20 ms/μF
Identification ON	$V_{16\text{-}18}$	<	200 mV

Demodulator part

Delayed chrominance input signal (peak-to-peak value) with 75% colour bar signal	$V_{7\text{-}24(p\text{-}p)}$	typ.	250 mV
Colour difference output signals (peak-to-peak values)			
−(R-Y) signal	$V_{11\text{-}24(p\text{-}p)}$	typ.	1,05 V ± 3 dB
−(B-Y) signal	$V_{10\text{-}24(p\text{-}p)}$	typ.	1,33 V ± 3 dB
Ratio of colour difference output signals (R-Y)/(B-Y)	$\frac{V_{11\text{-}24}}{V_{10\text{-}24}}$	typ.	0,79 ± 10 %
D.C. voltage at colour difference outputs			
at colour ON	$V_{10;\,11\text{-}24}$	typ.	8 V
at colour OFF	$V_{10;\,11\text{-}24}$	typ.	4 V
Signal attenuation at colour OFF		>	60 dB
Residual 4,4 MHz signal	$V_{10;\,11\text{-}24}$	<	20 mV
H/2 ripple at (R-Y) output (peak-to-peak value) without input signal	$V_{11\text{-}24(p\text{-}p)}$	<	10 mV

PAL DECODER

The TDA3561A is a decoder for the PAL colour television standard. It combines all functions required for the identification and demodulation of PAL signals. Furthermore it contains a luminance amplifier, an RGB-matrix and amplifier. These amplifiers supply output signals up to 5 V peak-to-peak (picture information) enabling direct drive of the discrete output stages. The circuit also contains separate inputs for data insertion, analogue as well as digital, which can be used for text display systems (e.g. (Teletext/ broadcast antiope), channel number display, etc. Additional to the TDA3560, the circuit includes the following features:

- The peak white limiter is only active during the time that the 9,3 V level at the output is exceeded. The start of the limiting function is delayed by one line period. This avoids peak white limiting by test patterns which have abrupt transitions from colour to white signals.
- The brightness control is obtained by inserting a variable pulse in the luminance channel. Therefore the ratio of brightness variation and signal amplitude at the three outputs will be identical and independent of the difference in gain of the three channels. Thus discolouring due to adjustment of contrast and brightness is avoided.
- Improved suppression of the internal RGB signals when the device is switched to external signals, and vice versa.
- Non-synchronized external RGB signals do not disturb the black level of the internal signals.
- Improved suppression of the residual 4,4 MHz signal in the RGB output stages.
- Cascoded stages in the demodulators and burst phase detector minimize the radiation of the colour demodulator inputs.
- High current capability of the RGB outputs and the chrominance output.

QUICK REFERENCE DATA

Supply voltage	V_{1-27}	type.	12	V
Supply current	I_1	typ.	85	mA
Luminance input signal (peak-to-peak value)	$V_{10-27(p-p)}$	typ.	0,45	V
Chrominance input signal (peak-to-peak value)	$V_{3-27(p-p)}$	55 to	1100	mV
Data input signals (peak-to-peak value)	$V_{13,15,17-27(p-p)}$	typ.	1	V
RGB output signals at nominal contrast and saturation (peak-to-peak value)	$V_{12,14,16-27(p-p)}$	typ.	5,25	V
Contrast control range		typ.	20	dB
Saturation control range		min.	50	dB
Input voltage for data insertion	V_{9-27}	min.	0,9	V
Blanking input voltage	V_{8-27}	typ.	1,5	V
Burst gating and black-level gating input voltage	V_{8-27}	typ.	7	V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

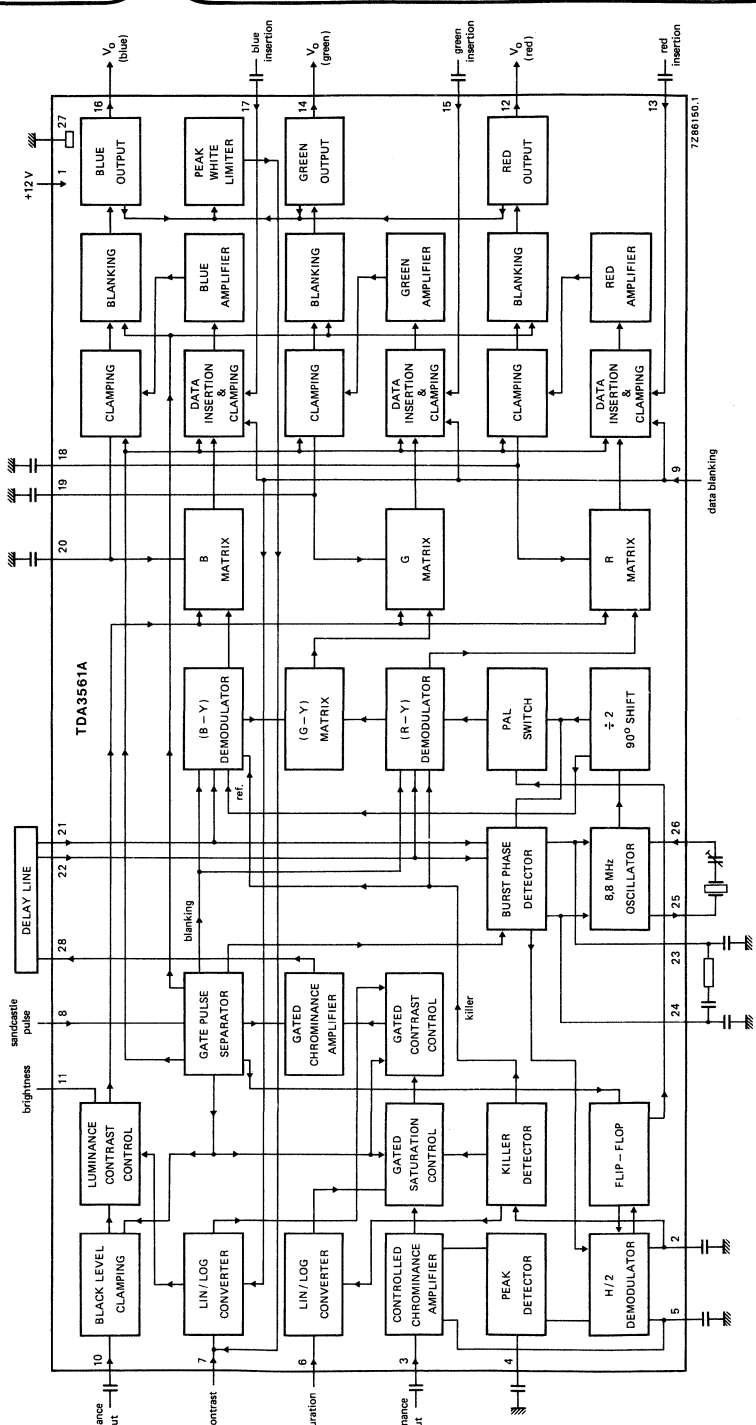


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_P = V_{1-27}$	max.	13,2	V
Total power dissipation; see also Fig. 2	P_{tot}	max.	1,7	W
Storage temperature range	T_{stg}		−25 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 65	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	50	K/W

CHARACTERISTICS

$V_P = V_{1-27} = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified

Supply voltage	$V_P = V_{1-27}$	typ.	12	V
			8 to 13,2	V
Supply current		typ.	85	mA
		<	115	mA
Total power dissipation	P_{tot}	typ.	1,0	W
		<	1,4	W
Luminance input (pin 10)				
Input voltage (peak-to-peak value); note 1	$V_{10-27(p-p)}$	typ.	0,45	V
Input level before clipping	V_{10-27}	<	2	V
Input current; input level 2 V, clamp not active	I_{10}	typ.	0,15	μA
		<	1	μA
Contrast control range (see Fig. 3)			−17 to + 3	dB
Control voltage for 40 dB attenuation	V_{7-27}	typ.	1,2	V
Input current contrast control at $V_{7-27} = 3$ V	I_7	<	10	μA
Chrominance amplifier				
Input voltage (peak-to-peak value); note 2	$V_{3-27(p-p)}$	typ.	550	mV
			55 to 1100	mV
Input impedance	$\lvert Z_{3-27}\rvert$	typ.	9	kΩ
			6 to 12	kΩ
Input capacitance	C_{3-27}	typ.	4	pF
		<	6	pF
A.C.C. control range		>	30	dB
Change of the burst signal at the output over the whole control range		<	1,5	dB
Gain at nominal contrast/saturation pin 3 to pin 28; note 3		>	32	dB
Output signal (peak-to-peak value) at nominal contrast/saturation; burst signal: 0,5 V peak to peak	$V_{28-27(p-p)}$	typ.	1,7	V
Maximum output voltage (peak-to-peak value) $R_L = 2$ kΩ	$V_{28-27(p-p)}$	typ.	4,0	V

CHARACTERISTICS (continued)

Chrominance amplifier (continued)

Distortion of chrominance amplifier at $V_{28\text{-}27(p\text{-}p)}$ = 2 V up to $V_{3\text{-}27(p\text{-}p)}$ = 1 V	d	typ. <	1,5 5	% %
Frequency response between 0 and 5 MHz			−2	dB
Saturation control range (see Fig. 4)		>	50	dB
Input current saturation control at $V_{6\text{-}27}$ = 3 V	I_6	<	15	μA
Tracking between luminance and chrominance with contrast control over a range of 10 dB		<	2	dB
Cross-coupling between luminance and chrominance amplifier; note 10		<	−46	dB
Signal-to-noise ratio at nominal input signal; note 11	S/N	>	56	dB
Phase shift between burst and chrominance at nominal contrast/saturation	$\Delta\varphi$	<	± 5°	
Output impedance of chrominance amplifier	$\lvert Z_{28\text{-}27}\rvert$	typ.	25	Ω
Maximum output current	I_{28}	<	15	mA

Reference part

Phase locked loop:				
– catching range; note 4		> typ.	500 700	Hz Hz
– phase shift; note 5		<	5°	
Oscillator:				
– temperature coefficient of oscillator frequency; note 4		typ.	−1,5	Hz/K
– frequency deviation for V_P changing from 10 to 13,2 V; note 4		typ.	40	Hz
– input resistance (pin 26)	$R_{26\text{-}27}$	typ. 260 to 420	340	Ω Ω
– input capacitance (pin 26)	$C_{26\text{-}27}$	<	10	pF
– output resistance (pin 25)	$R_{25\text{-}27}$	typ. 100 to 200	150	Ω Ω
– output voltage (peak-to-peak value; pin 25)	$V_{25\text{-}27(p\text{-}p)}$	typ.	700	mV
A.C.C. generation:				
– reference voltage (pin 4)	$V_{4\text{-}27}$	typ.	4,9	V
– control voltage at nominal input signal (pin 2)	$V_{2\text{-}27}$	typ.	5,1	V
– control voltage without chrominance input (pin 2)	$V_{2\text{-}27}$	typ.	2,65	V
– colour-off voltage (pin 2)	$V_{2\text{-}27}$	typ.	3,15	V
– colour-on voltage (pin 2)	$V_{2\text{-}27}$	typ.	3,4	V
– identification-on voltage (pin 2)	$V_{2\text{-}27}$	typ.	1,9	V
– change in burst amplitude with supply voltage (± 10%)		proportional		
– change in burst amplitude with temperature		typ. <	0,1 0,25	%/K %/K
– voltage at pin 5 at nominal input signal	$V_{5\text{-}27}$	typ.	5	V

Demodulator part

Input burst signal amplitude (peak-to-peak value) between pins 21 and 22; note 6	$V_{21\text{-}22(p\text{-}p)}$	typ.	100 mV
Input impedance between pins 21 and 22	$\lvert Z_{21\text{-}22}\rvert$	typ.	2 kΩ
Ratio of demodulated signals for equal input signals at pins 21 and 22 (B−Y)/(R−Y)	$\frac{V_{16\text{-}27}}{V_{12\text{-}27}}$	typ.	1,78 ± 10%
(G−Y)/(R−Y); no (B−Y) signal	$\frac{V_{14\text{-}27}}{V_{12\text{-}27}}$	typ.	−0,51 ± 10%
(G−Y)/(B−Y); no (R−Y) signal	$\frac{V_{14\text{-}27}}{V_{16\text{-}27}}$	typ.	−0,19 ± 25%
Frequency response between 0 and 1 MHz			−3 dB
Cross talk between colour demodulated signals		>	40 dB
Phase difference between (R−Y) signal and (R−Y) reference signal		<	5°
Phase difference between (R−Y) and (B−Y) reference signals		typ.	90° 85 to 95°

R.G.B. matrix and amplifiers

Output voltage (peak-to-peak value) at nominal luminance/contrast (black to white); note 3	$V_{12,14,16\text{-}27(p\text{-}p)}$	typ.	5,4 V 4,5 to 6,3 V
Output voltage (peak-to-peak value) of the RED channel at nominal contrast/saturation and no luminance signal at the input, (R−Y) signal	$V_{12\text{-}27(p\text{-}p)}$	typ.	5,25 V 3,7 to 6,7 V
Maximum peak white level; note 7		typ.	9,3 V 9,0 to 9,6 V
Maximum output current	$I_{12,14,16}$	<	15 mA
Black level at the output for a brightness control voltage of 2 V	$V_{12,14,16\text{-}27}$	typ.	2,6 V
Difference in black level between the three channels at an output level of 3 V; note 8	ΔV	<	200 mV
Black level shift with vision contents		<	40 mV
Brightness control voltage range	see Fig. 5		
Input current brightness control	I_{11}	<	50 μA
Variation of black level with temperature	ΔV	typ. <	0,35 mV/K 1,0 mV/K
Variation of black level with contrast control	ΔV	typ. <	10 mV 200 mV
Relative spread between the R, G and B output signals		<	10 %
Relative black-level variation between the three channels during variation of contrast and supply voltage		typ. <	0 mV 20 mV

CHARACTERISTICS (continued)

RGB matrix and amplifier (continued)

Differential black-level drift over a temperature range of 40 °C		typ. <	0 mV 20 mV
Blanking level at the RGB outputs		typ. 1,9 to 2,3	2,1 V V
Difference in blanking level of the three channels		typ.	0 mV
Differential blanking level drift over a temperature range of 40 °C		typ.	0 mV
Tracking of output black level with supply voltage	$\frac{\Delta V_{bl}}{V_{bl}} \times \frac{V_P}{\Delta V_P}$	typ.	1,1
Signal-to-noise ratio of output signals; note 11	S/N	>	62 dB
Residual 4,4 MHz signal at RGB outputs (peak-to-peak value)		typ. <	40 mV 150 mV
Residual 8,8 MHz signal and higher harmonics at the RGB outputs (peak-to-peak value)		typ. <	75 mV 150 mV
Output impedance of RGB outputs	$\lvert Z_{12,14,16-27} \rvert$	typ.	50 Ω
Frequency response of total luminance and RGB amplifier circuits for f = 0 to 5 MHz		<	−3 dB

Signal insertion (pins 13,15 and 17)

Input signals (peak-to-peak value) for an RGB output voltage of 5 V peak-to-peak	$V_{13,15,17-27(p-p)}$	typ. 0,85 to 1,1	1 V V
Difference between the black levels of the RGB signals and the inserted signals at the output; note 9	ΔV	<	260 mV
Output rise time	t_r	typ. <	40 ns 80 ns
Differential delay time for the three channels	t_d	typ. <	0 ns 40 ns
Input current	$I_{13,15,17}$	<	10 μA

Data blanking (pin 9)

Input voltage for no data insertion	V_{9-27}	<	0,4 V
Input voltage for data insertion	V_{9-27}	>	0,9 V
Maximum input voltage	V_{9-27}	<	3 V
Delay of data blanking	t_d	<	20 ns
Input current	I_9	<	35 μA
Input impedance	$\lvert Z_{9-27} \rvert$	typ.	10 kΩ
Suppression of the internal RGB signals when $V_{9-27} > 0,9$ V		>	46 dB

Sandcastle input (pin 8)

Level at which the RGB blanking is activated	$V_{8\text{-}27}$	typ.	1,5 V 1 to 2 V
Level at which burst gating and clamping pulse are separated	$V_{8\text{-}27}$	typ.	7,0 V 6,5 to 7,5 V
Delay between black level clamping and burst gating pulse	t_d	typ.	0,4 μs
Input current for:			
$V_{8\text{-}27}$ = 0 to 1 V	$-I_8$	<	1 mA
$V_{8\text{-}27}$ = 1 to 8,5 V	I_8	typ.	20 μA
$V_{8\text{-}27}$ = 8,5 to 12 V	I_8	<	2 mA

Notes to the characteristics

1. Signal with the negative-going sync; amplitude includes sync pulse amplitude.
2. Indicated is a signal for a colour bar with 75% saturation, so chrominance to burst ratio is 2,2 : 1.
3. Nominal contrast is specified as the maximum contrast −3 dB and nominal saturation as the maximum saturation −6 dB.
4. All frequency variations are referred to the 4,4 MHz carrier frequency.
5. For ± 400 Hz deviation of the oscillator frequency.
6. These signal amplitudes are determined by the a.c.c. circuit of the reference part.
7. When this level is exceeded, the amplitude of the output signal is reduced via a discharge of the capacitor at pin 7 (contrast control). The start of the peak white limiting action has a delay of one line period.
8. The variation of the black level depends directly on the gain of each channel during brightness control in the three channels. As a consequence, the black levels at the outputs (for output levels above or below 3 V) can have a difference which exceeds 200 mV. Because the amplitude and the black level change with brightness control have a direct relationship, no discolouring can occur, caused by adjustment of contrast and brightness.
9. This difference occurs when the source impedance of the data signal inputs is 150 Ω and the black level clamp pulse duration is 4 μs (sandcastle pulse). A lower difference is obtained when the impedance is lower.
10. Cross-coupling is measured under the following condition. Input signals nominal, contrast and saturation such that nominal output signals are obtained. The signals at the output at which no signal should be available must be compared with the nominal output signal at that output.
11. The signal-to-noise ratio is specified as peak-to-peak signal with respect to r.m.s. noise.

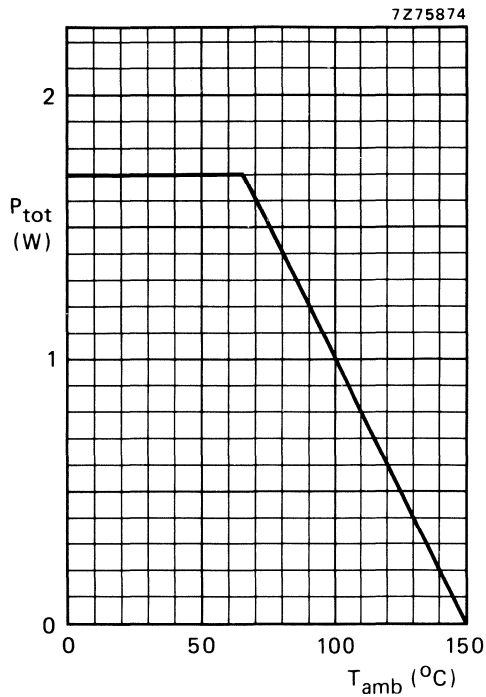


Fig. 2 Power derating curve.

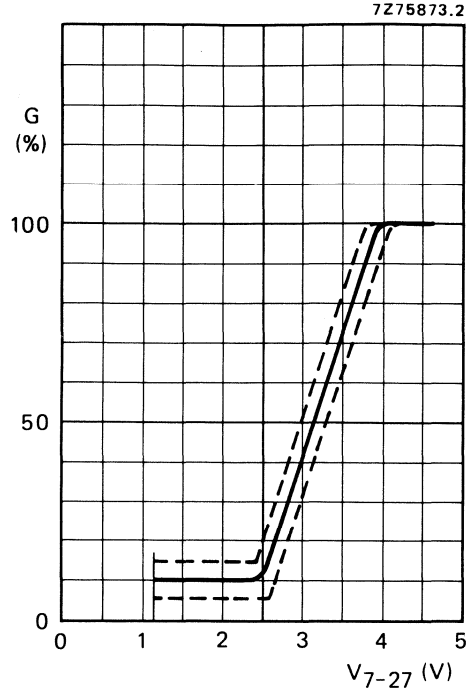


Fig. 3 Contrast control voltage range.

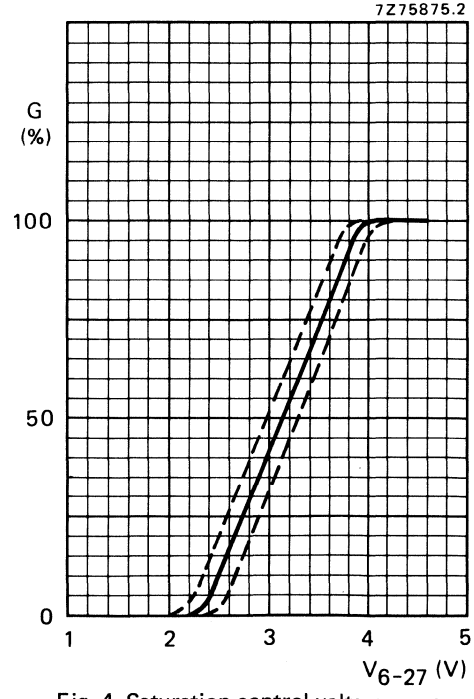


Fig. 4 Saturation control voltage range.

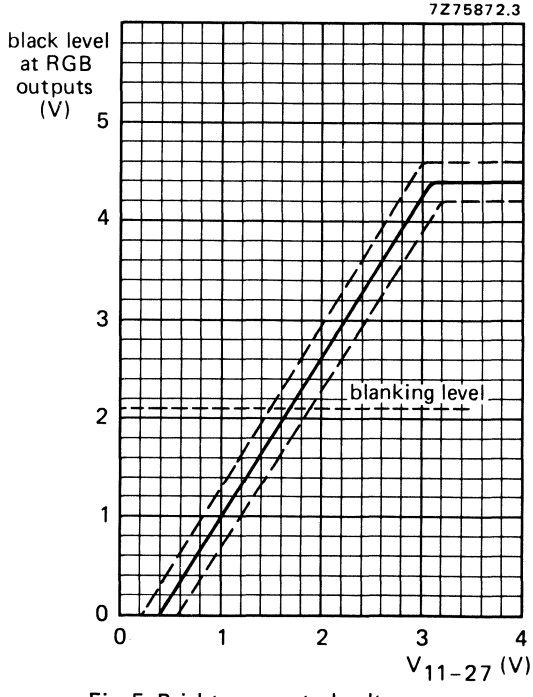


Fig. 5 Brightness control voltage range.

APPLICATION INFORMATION

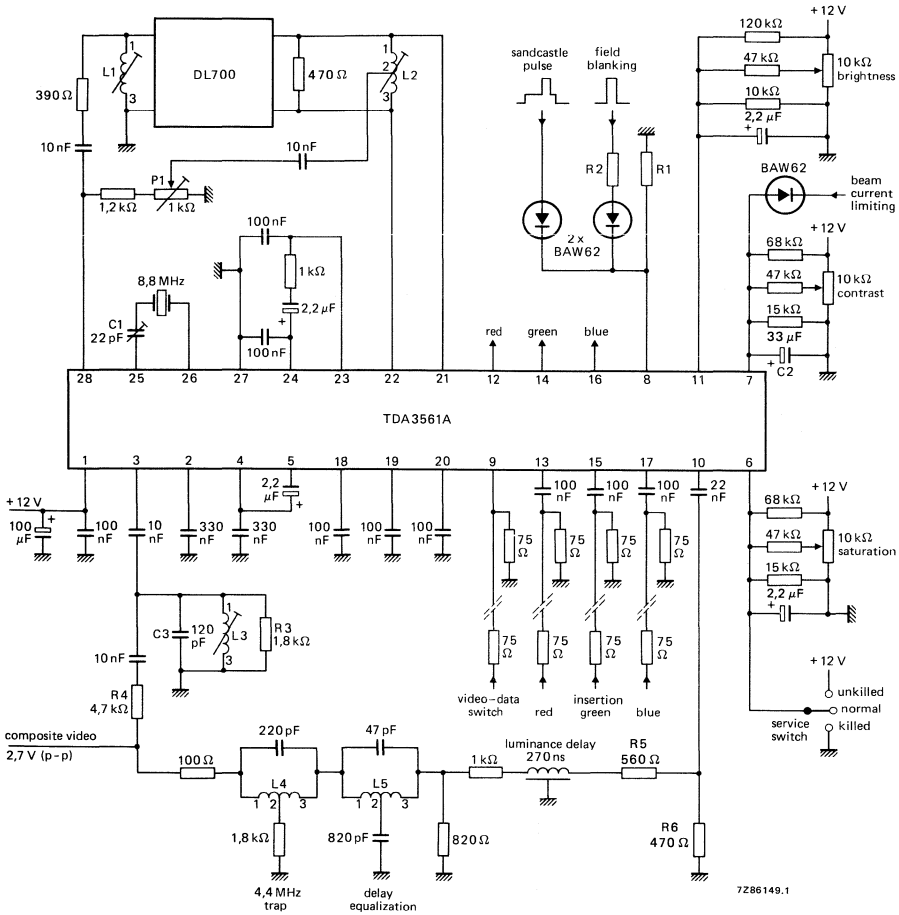


Fig. 6 Application circuit.

Adjustments (see Fig. 6)

C1	8,8 MHz oscillator	
L1	phase delay line	= 10,7 μH
L2	nominal value	= 10,7 μH
L3	4,4 MHz chrominance input filter	= 10,7 μH = L1
L4	4,4 MHz trap in luminance signal line	= 5,6 μH
L5	delay equalization	= 66,1 μH
P1	amplitude of direct chroma singal	
R1 R2	field blanking $\frac{R1}{R1 + R2}$ x field blanking amplitude 2,0 V to 6,5 V.	

For a video input voltage of 1 V peak-to-peak: R3 can be omitted; R4 = 1 kΩ; R5 must be short-circuited; R6 = 1 kΩ.

APPLICATION INFORMATION

The function is described against the corresponding pin number.

1. + 12 V power supply

The circuit gives good operation in a supply voltage range between 8 and 13,2 V provided that the supply voltage for the controls is equal to the supply voltage for the TDA3561A. All signal and control levels have a linear dependency on the supply voltage. The current taken by the device at 12 V is typically 85 mA. It is linearly dependent on the supply voltage.

2. Control voltage for identification

This pin requires a detection capacitor of about 330 nF for correct operation. The voltages available under various signal conditions are given in the specification.

3. Chrominance input

The chroma signal must be a.c.-coupled to the input. Its amplitude must be between 55 mV and 1100 mV peak-to-peak (25 mV to 500 mV peak-to-peak burst signal). All figures for the chroma signals are based on a colour bar signal with 75% saturation, that is the burst-to-chroma ratio of the input signal is 1 : 2,25.

4. Reference voltage A.C.C. detector

This pin must be decoupled by a capacitor of about 330 nF. The voltage at this pin is 4,9 V.

5. Control voltage A.C.C.

The A.C.C. is obtained by synchronous detection of the burst signal followed by a peak detector. A good noise immunity is obtained in this way and an increase of the colour for weak input signals is prevented. The recommended capacitor value at this pin is 2,2 μF.

6. Saturation control

The saturation control range is in excess of 50 dB. The control voltage range is 2 to 4 V. Saturation control is a linear function of the control voltage.

When the colour killer is active, the saturation control voltage is reduced to a low level if the resistance of the external saturation control network is sufficiently high. Then the chroma amplifier supplies no signal to the demodulator. Colour switch-on can be delayed by proper choice of the time constant for the saturation control setting circuit.

When the saturation control pin is connected to the power supply the colour killer circuit is overruled so that the colour signal is visible on the screen. In this way it is possible to adjust the oscillator frequency without using a frequency counter (see also pins 25 and 26).

7. Contrast control

The contrast control range is 20 dB for a control voltage change from + 2 to + 4 V. Contrast control is a linear function of the control voltage. The output signal is suppressed when the control voltage is 1 V or less. If one or more output signals surpasses the level of 9 V the peak white limiter circuit becomes active and reduces the output signals via the contrast control by discharging C2 via an internal current sink.

8. Sandcastle and field blanking input

The output signals are blanked if the amplitude of the input pulse is between 2 and 6,5 V. The burst gate and clamping circuits are activated if the input pulse exceeds a level of 7,5 V.
The higher part of the sandcastle pulse should start just after the sync pulse to prevent clamping of video signal on the sync pulse. The width should be about 4 μs for proper A.C.C. operation.

9. Video-data switching

The insertion circuit is activated by means of this input by an input pulse between 1 V and 2 V. In that condition, the internal RGB signals are switched off and the inserted signals are supplied to the output amplifiers. If only normal operation is wanted this pin should be connected to the negative supply. The switching times are very short ($<$ 20 ns) to avoid coloured edges of the inserted signals on the screen.

10. Luminance signal input

The input signal should have a peak-to-peak amplitude of 0,45 V (peak white to sync) to obtain a black-white output signal of 5 V at nominal contrast. It must be a.c.-coupled to the input by a capacitor of about 22 nF. The signal is clamped at the input to an internal reference voltage.
A 1 kΩ luminance delay line can be applied because the luminance input impedance is made very high. Consequently the charging and discharging currents of the coupling capacitor are very small and do not influence the signal level at the input noticeably. Additionally the coupling capacitor value may be small.

11. Brightness control

The black level of the RGB outputs can be set by the voltage on this pin (see Fig. 5). The black level can be set higher than 4 V however the available output signal amplitude is reduced (see pin 7). Brightness control also operates on the black level of the inserted signals.

12, 14, 16. RGB outputs

The output circuits for red, green and blue are identical. Output signals are 5,25 V (R, G and B) at nominal input signals and control settings. The black levels of the three outputs have the same value. The blanking level at the outputs is 2,1 V. The peak white level is limited to 9,3 V. When this level exceeded the output signal amplitude is reduced via the contrast control (see pin 7).

13, 15, 17. Inputs for external RGB signals

The external signals must be a.c.-coupled to the inputs via a coupling capacitor of about 100 nF. Source impedance should not exceed 150 Ω. The input signal required for a 5 V peak-to-peak output signal is 1 V peak -to-peak. At the RGB outputs the black level of the inserted signal is identical to that of normal RGB signals. When these inputs are not used the coupling capacitors have to be connected to the negative supply.

18, 19, 20. Black level clamp capacitors

The black level clamp capacitors for the three channels are connected to these pins. The value of each capacitor should be about 100 nF.

21, 22. Inputs (B-Y) and (R-Y) demodulators

The input signal is automatically fixed to the required level by means of the burst phase detector and A.C.C. generator which are connected to pin 21 and pin 22. As the burst (applied differentially to those pins) is kept constant by the A.C.C., the colour difference signals automatically have the correct value.

APPLICATION INFORMATION (continued)

23, 24. Burst phase detector outputs

At these pins the output of the burst phase detector is filtered and controls the reference oscillator. An adequate catching range is obtained with the time constants given in the application circuit (see Fig. 6).

25, 26. Reference oscillator

The frequency of the oscillator is adjusted by the variable capacitor C1. For frequency adjustment interconnect pin 21 and pin 22. The frequency can be measured by connecting a suitable frequency counter to pin 25.

28. Output of the chroma amplifier

Both burst and chroma signals are available at the output. The burst-to-chroma ratio at the output is identical to that at the input for nominal control settings. The burst signal is not affected by the controls. The amplitude of the input signal to the demodulator is kept constant by the A.C.C. Therefore the output signal at pin 28 will depend on the signal loss in the delay line.

PAL DECODER

GENERAL DESCRIPTION

The TDA3565 PAL decoder contains all the functions required for PAL signal decoding and colour matrixing and is contained within an 18-pin package. The oscillator, a.c.c. detector and burst phase detector each have single-pin outputs and the coupling capacitor for the luminance input at pin 8 doubles as a storage capacitor for the black level clamping circuit. Black level clamping of the three colour channels is performed using feedback proportional to the red channel black level. This feedback (variable with the brightness control) controls the input level of the luminance amplifier and therefore the clamping levels of all three colour signal outputs.

QUICK REFERENCE DATA

Supply voltage	$V_p = V_{1-17}$	typ.	12 V
Supply current	$I_P = I_1$	typ.	85 mA
Luminance input signal (peak-to-peak value)	$V_{8-17(p-p)}$	typ.	0,45 V
Chrominance input signal (peak-to-peak value)	$V_{3-17(p-p)}$	typ.	550 mV
RGB output signal amplitudes (peak-to-peak value) at nominal luminance and contrast	$V_{10,11,12-17(p-p)}$	typ.	5 V
Contrast control range			−17 to +3 dB
Saturation control range		>	50 dB
A.C.C. control range		>	30 dB
Level at which RGB blanking is activated	V_{7-17}	typ.	1,5 V
Level at which burst gate/clamping pulse are separated	V_{7-17}	typ.	7 V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

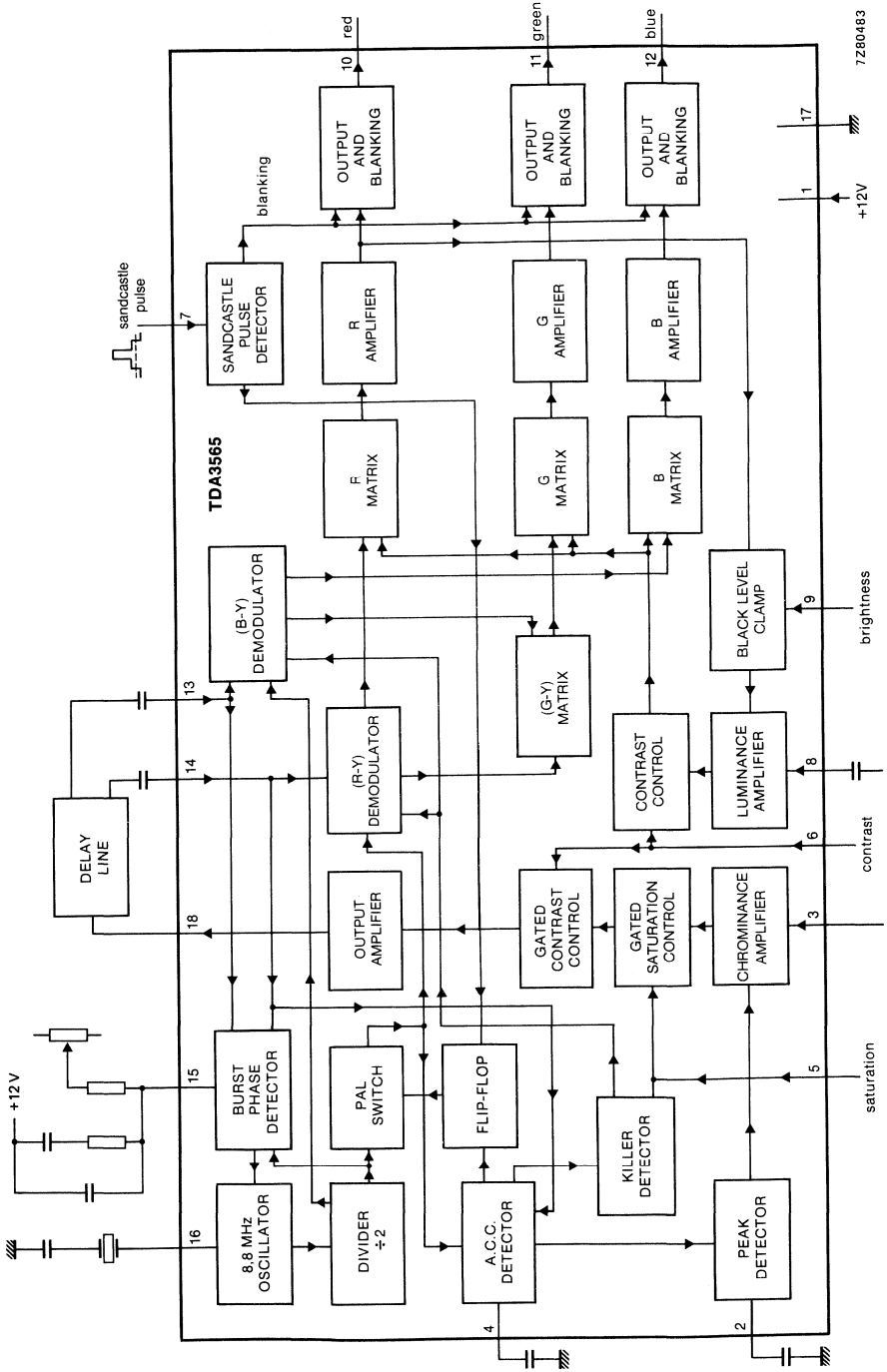


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 1)	$V_P = V_{1-17}$	max.	13,2	V
Total power dissipation	P_{tot}	max.	1,7	W
Operating ambient temperature range	T_{amb}		−25 to +65	°C
Storage temperature range	T_{stg}		−25 to +150	°C

THERMAL RESISTANCE

From junction to ambient (in free air)	$R_{th\ j-a}$	max.	50	K/W

CHARACTERISTICS

$V_P = V_{1-17} = 12$ V; $T_{amb} = 25$ °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 1)					
Supply voltage	V_{1-17}	9,0	12,0	13,2	V
Supply current	I_1	–	85	–	mA
Total power dissipation	P_{tot}	–	1,0	–	W
Luminance amplifier					
Input signal amplitude (note 1) (peak-to-peak value)	$V_{8-17(p-p)}$	–	0,45	–	V
Input level before clipping occurs *	$V_{8-17(p-p)}$	–	–	0,7	V
Input current at $V_{8-17} = 2$ V; clamp not active	I_8	–	0,15	1,0	μA
Contrast control range (Fig. 2)		–	−17 to +3	–	dB
Input current when peak white limiter is active ($V_{6-17} = 2{,}5$ V)	I_8	–	5,5	–	mA
Input resistance $V_{6-17} > 6$ V	R_i	1,4	2,0	2,6	kΩ
Chrominance amplifier					
Input signal amplitude (note 2)	$V_{3-17(p-p)}$	55	550	1100	mV
Minimum burst signal amplitude within the control range (peak-peak)		30	–	–	mV
Input impedance	Z_{3-17}	–	8,0	–	kΩ
Input capacitance	C_{3-17}	–	4,0	6,0	pF
A.C.C. control range		30	–	–	dB
Change of burst signal at output over whole a.c.c. control range		–	–	1	dB
Amplification pin 3 to pin 18 at nominal contrast/saturation (note 3)		32	–	–	dB

* At nominal contrast and nominal brightness.

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Chrominance amplifier (continued)					
Chroma to burst ratio (note 3)		–	3,8	–	dB
Max. output voltage range (pin 18) R_L = 2 kΩ		4,0	4,5	–	V
Chrominance amplifier distortion at $V_{8\text{-}17(p\text{-}p)}$ = 2 V (output) up to $V_{3\text{-}17(p\text{-}p)}$ = 1 V (input)	$d_{8\text{-}3}$	–	3,0	5,0	%
Frequency response between 0 and 5 MHz		–	–	–2	dB
Saturation control range (Fig. 3)		50	–	–	dB
Saturation control input current at $V_{5\text{-}17} < 6$ V	I_5	–	1	20	μA
Input impedance for V_5 between 6 and 10 V	Z_i	1,4	2,0	2,6	kΩ
Input impedance when colour killer is active	Z_i	1,4	2,0	2,6	kΩ
Input impedance for $V_5 > 10$ V (adjustment procedure)	Z_i	0,7	1,0	1,3	kΩ
Tracking between luminance and chrominance over 10 dB of contrast control range		–	–	2	dB
Cross coupling between luminance and chrominance amplifiers (note 4)		–	–	–46	dB
Signal-to-noise ratio at nominal input signal (note 5)	S/N	56	–	–	dB
Burst phase shift with respect to chrominance at nominal contrast/saturation (note 3)	$\Delta\varphi$	–	–	±5	deg
Chrominance amplifier output impedance	$Z_{18\text{-}17}$	–	25	–	Ω
Output current (pin 18)	I_{18}	–	–	10	mA
Reference part					
Phase-locked loop					
Catching range	Δf	500	700	–	Hz
Phase shift for ± 400 Hz deviation of oscillator frequency	$\Delta\varphi$	–	–	5	deg
Oscillator					
Temperature coefficient of oscillator frequency	TC_{osc}	–	2	3	Hz/K
Frequency deviation when supply voltage changes from 10 to 13,2 V	Δf_{osc}	–	200	300	Hz

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Input resistance	$R_{16\text{-}17}$	250	290	330	Ω
Input capacitance	$C_{16\text{-}17}$	–	–	10	pF
A.C.C. generation					
Voltage with nominal input signal	$V_{4\text{-}17}$	–	5,0	–	V
Voltage without chrominance input	$V_{4\text{-}17}$	–	2,5	–	V
Colour-off voltage	$V_{4\text{-}17}$	–	3,2	–	V
Colour-on voltage	$V_{4\text{-}17}$	–	3,5	–	V
Identification-on voltage	$V_{4\text{-}17}$	–	2,5	–	V
Pin 2 voltage at nominal input signal	$V_{2\text{-}17}$	–	5,1	–	V
Demodulator part					
Burst signal amplitude (peak-to-peak value) at pins 13 and 14 (note 6)	$V_{13\text{-}17(p\text{-}p)}$ $V_{14\text{-}17(p\text{-}p)}$	–	80	–	mV
Input impedance of pins 13 or 14 to pin 17	$Z_{13,\,14\text{-}17}$	–	1,0	–	kΩ
Ratios of demodulated signals with equal signal inputs to pins 13 and 14 and no luminance input signal:					
(B-Y)/(R-Y)	$\frac{V_{12\text{-}17}}{V_{10\text{-}17}}$	–	1,78±10%	–	
(G-Y)/(R-Y) (no (B-Y) signal)	$\frac{V_{11\text{-}17}}{V_{10\text{-}17}}$	–	−0,51±10%	–	
(G-Y)/(B-Y) (no (R-Y) signal)	$\frac{V_{11\text{-}17}}{V_{12\text{-}17}}$	–	−0,19±10%	–	
Frequency response between 0 and 1 MHz		–	–	−3	dB
Separation of colour difference channels		40	–	–	dB
Phase difference between (R-Y) signal and (R-Y) reference signal	$\Delta\varphi$	–	–	5	deg
Phase difference between (R-Y) and (B-Y) reference signals	$\Delta\varphi$	85	90	95	deg
RGB matrix and amplifiers					
Output signal amplitudes (peak-to-peak value) at nominal luminance signal and contrast inputs (black-white) (note 3)	$V_{10\text{-}17(p\text{-}p)}$ $V_{11\text{-}17(p\text{-}p)}$ $V_{12\text{-}17(p\text{-}p)}$	4,5	5,0	5,5	V
Red channel output amplitude (peak-to-peak value) at nominal contrast/saturation (note 3) and no luminance signal to (R-Y)	$V_{10\text{-}17(p\text{-}p)}$	3,7	5,25	7,4	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Maximum peak white level (note 7)		9,0	9,3	9,6	V
Maximum output current	$I_{10,11,12}$	–	–	15	mA
Red channel black level output when brightness control V_{9-17} = 2 V	V_{10-17}	–	2,7	–	V
Difference between black levels in R, G and B outputs		–	–	600	mV
Black level shift with picture content		–	–	40	mV
Brightness control voltage range	V_{9-17}		see Fig. 3		
Brightness control input current at V_{9-17} = 2 V	I_9	–	–	–50	μA
Variation of black level with temperature		–	+0,35	1,0	mV/K
Variation of black level with contrast control		–	10	100	mV
Relative spread between the three channel outputs		–	–	10	%
Relative variation in black level between the three channels during normal variations of contrast and supply voltage		–	0	20	mV
Differential drift of black level over a temperature range of 40 °C		–	0	20	mV
Blanking level at the three channel outputs		1,9	2,1	2,3	V
Difference in blanking level of the three channel outputs		–	0	–	mV
Differential drift of blanking levels over a temperature range of 40 °C		–	0	–	mV
Tracking of output black levels with variation of supply voltage	$\frac{\Delta V_{bl}}{V_{bl}} \times \frac{V_P}{\Delta V_P}$	–	1,1	–	
Signal-to-noise ratio of output signals (note 5)	S/N	62	–	–	dB
Residual 4,4 MHz component in output signals (peak-to-peak value)		–	25	50	mV
Residual 8,8 MHz and higher harmonic components in output signals (peak-to-peak value)		–	25	50	mV
Output impedance	$Z_{10,11,12-17}$	–	50	–	Ω
Frequency response of total luminance/RGB amplifier circuits for 0 to 5 MHz		–	–	–3	dB

parameter	symbol	min.	typ.	max.	unit
Sandcastle pulse detector					
Level at which RGB blanking is activated	V_{7-17}	1,0	1,5	2,0	V
Level at which burst gate and clamping pulse are separated	V_{7-17}	6,5	7,0	7,5	V
Delay between black level clamping and burst gating pulse		–	0,4	–	μs
Input current at:					
V_{7-17} = 0 to 1 V	I_7	–	–	−1	mA
V_{7-17} = 1 to 8,5 V	I_7	–	20	40	μA
V_{7-17} = 8,5 to 12 V	I_7	–	–	2	mA

Notes to the characteristics

1. Signal with negative-going sync pulse, amplitude includes sync pulse amplitude.
2. The signal indicated is for a colour bar with 75% saturation, so the chroma burst ratio of 2,2 : 1.
3. Nominal contrast is defined as (maximum contrast −3 dB) and nominal saturation is (maximum saturation −12 dB).
4. Cross coupling is measured under the following condition; input signals nominal and contrast/saturation such that nominal output signals are obtained. The signals at the output at which no signal should be available must be compared with the nominal signal at that output.
5. The signal-to-noise ratio is specified as peak-to-peak signal with respect to r.m.s. noise.
6. These signal amplitudes are determined by the a.c.c. circuit of the reference part.
7. When this level is exceeded the amplitude of the output signal is reduced via a discharge of the capacitor at pin 6 (contrast control). The discharge current is 5,5 mA.

DEVELOPMENT DATA

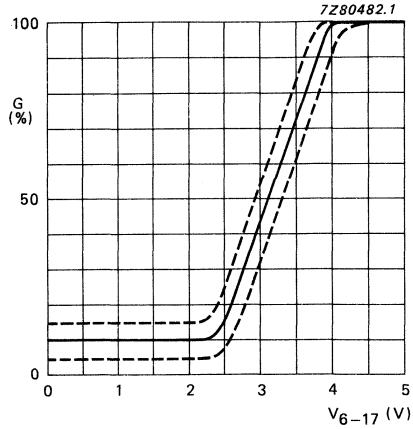


Fig. 2 Luminance contrast control voltage range.

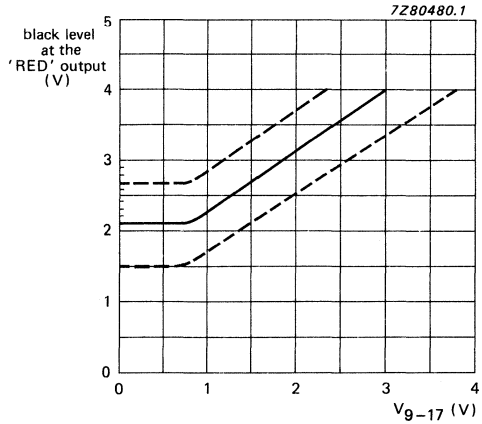


Fig. 3 Brightness control voltage range.

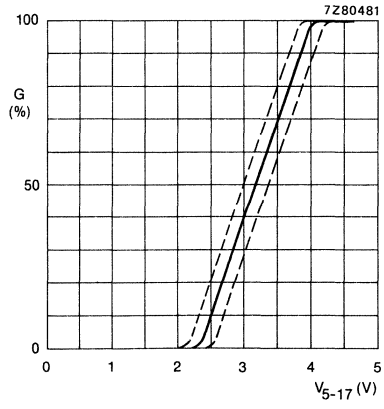


Fig. 4 Saturation control voltage range.

APPLICATION INFORMATION

DEVELOPMENT DATA

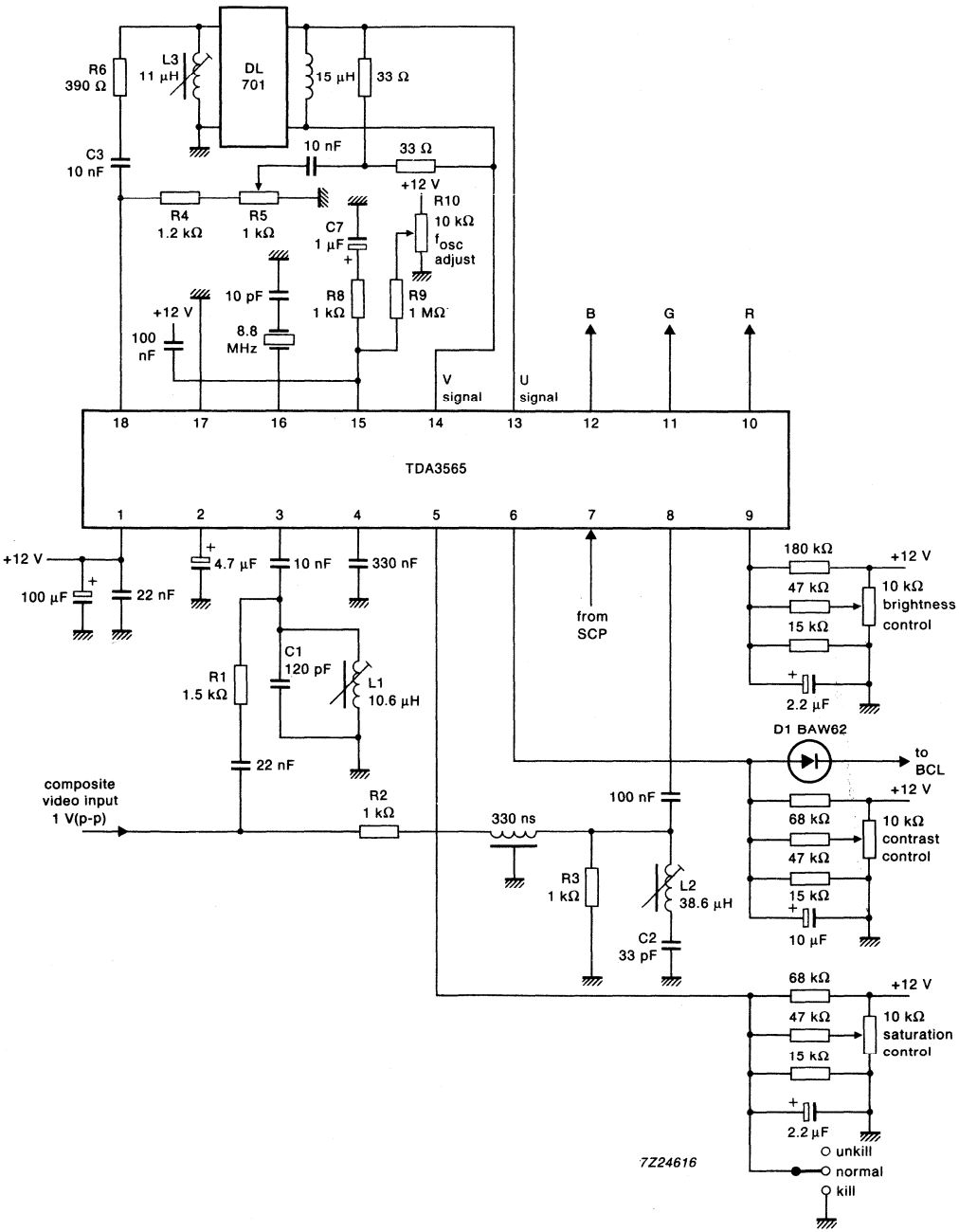


Fig. 5 Application diagram

PAL/NTSC DECODER

GENERAL DESCRIPTION

The TDA3566 is a monolithic integrated decoder for the PAL and/or NTSC colour television standards. It combines all functions required for the identification and demodulation of PAL/NTSC signals. Furthermore it contains a luminance amplifier, an RGB-matrix and amplifier. These amplifiers supply output signals up to 4 V peak-to-peak (picture information) enabling direct drive of the discrete output stages. The circuit also contains separate inputs for data insertion, analogue as well as digital, which can be used for text display systems (e.g. Teletext/broadcast antiope), channel number display, etc.

Features

- A black-current stabilizer which controls the black-currents of the three electron-guns to a level low enough to omit the black-level adjustment
- Contrast control of inserted RGB signals
- No black-level disturbance when non-synchronized external RGB signals are available on the inputs
- NTSC capability with hue control

QUICK REFERENCE DATA

Supply voltage (pin 1)	$V_P = V_{1-27}$	typ.	12 V
Supply current (pin 1)	$I_P = I_1$	typ.	80 mA
Luminance amplifier (pin 8)			
Input voltage (peak-to-peak value)	$V_{8-27(p-p)}$	typ.	450 mV
Contrast control range		typ.	20 dB
Chrominance amplifier (pin 4)			
Input voltage range (peak-to-peak value)	$V_{4-27(p-p)}$	40 to	1100 mV
Saturation control range		min.	50 dB
RGB matrix and amplifiers			
Output voltage at nominal luminance and contrast (peak-to-peak value)	$V_{13, 15, 17-27(p-p)}$	typ.	4 V
Data insertion			
Input signals (peak-to-peak value)	$V_{12, 14, 16-27(p-p)}$	typ.	1 V
Data blanking (pin 9)			
Input voltage for data insertion	V_{9-27}	min.	0,9 V
Sandcastle input (pin 7)			
Blanking input voltage	V_{7-27}	typ.	1,5 V
Burst gating and clamping input voltage	V_{7-27}	typ.	7 V

PACKAGE OUTLINE

28-lead DIL; plastic, with internal heat spreader (SOT117).

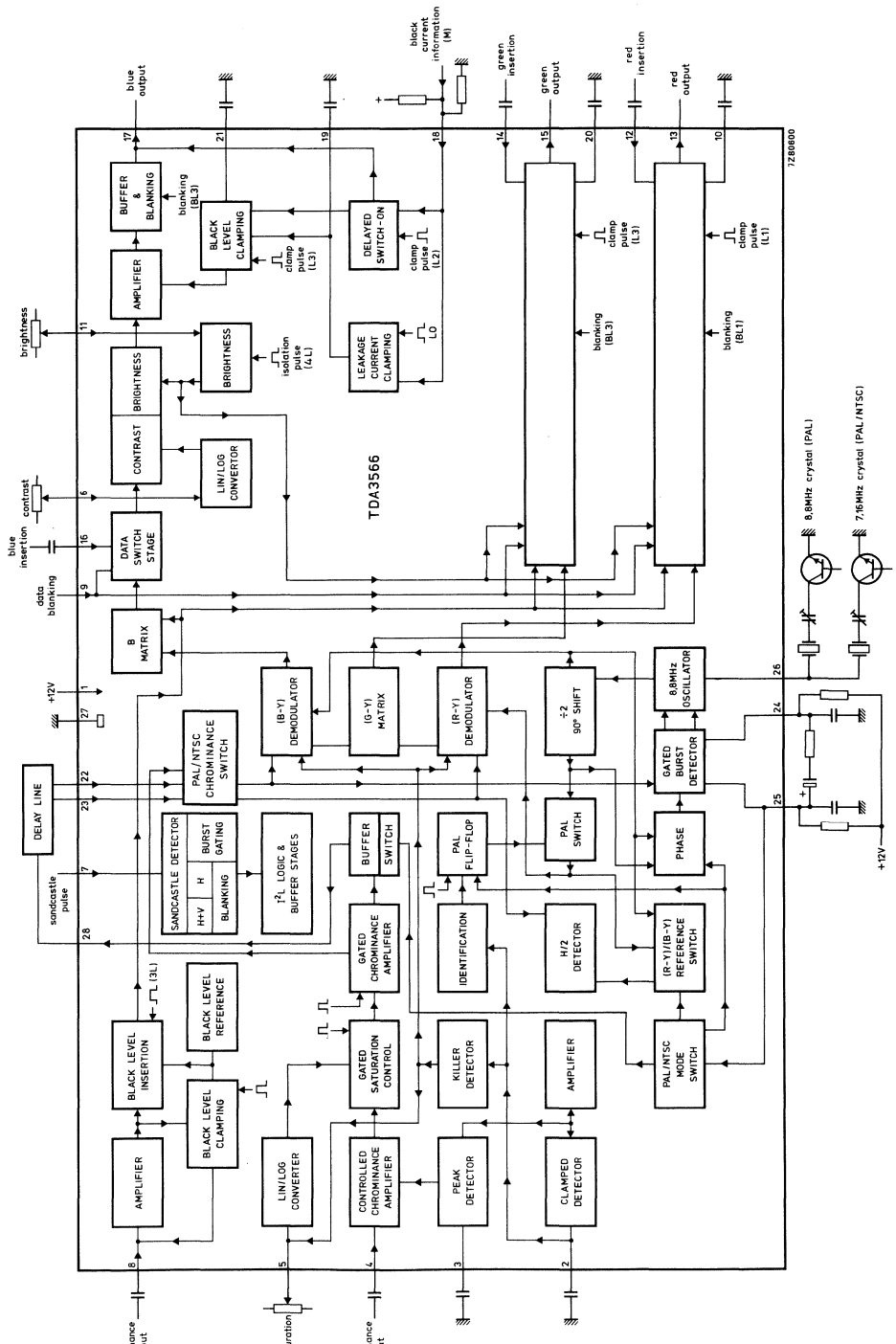


Fig. 1 Block diagram; for explanation of pulse mnemonics see Fig. 6.

FUNCTIONAL DESCRIPTION

The TDA3566 is a further development of the TDA3562A. It has the same pinning and almost the same application. The differences between the TDA3562A and the TDA3566 are as follows:

- The NTSC-application has largely been simplified. In the case of NTSC the chroma signal is now internally coupled to the demodulators, ACC and phase detectors. The chroma output signal (pin 28) is suppressed in this case. It follows that the external switches and filters which are needed for the TDA3562A are not needed for the TDA3566.
  Furthermore there is no difference between the amplitude of the colour output signals in the PAL or NTSC mode. The PAL/NTSC-switch and the hue control of the TDA3566 and the TDA3562A are identical.
- The switch-on and the switch-off behaviour of the TDA3566 has been improved. This has been obtained by suppressing the output signals during the switch-on and switch-off periods.
- The clamp capacitors connected to the pins 10, 20 and 21 can be reduced to 100 nF for the TDA3566. The clamp capacitors also receive a pre-bias voltage to avoid coloured background during switch-on.
- The crystal oscillator circuit has been changed to prevent parasitic oscillations on the third overtone of the crystal. This has the consequence that optimal tuning capacitance must be reduced to 10 pF.

Luminance amplifier

The luminance amplifier is voltage driven and requires an input signal of 450 mV peak-to-peak (positive video). The luminance delay line must be connected between the i.f. amplifier and the decoder. The input signal is a.c. coupled to the input (pin 8). After amplification, the black level at the output of the preamplifier is clamped to a fixed d.c. level by the black level clamping circuit. During three line periods after vertical blanking, the luminance signal is blanked out and the black level reference voltage is inserted by a switching circuit. This black level reference voltage is controlled via pin 11 (brightness). At the same time the RGB signals are clamped. Noise and residual signals have no influence during clamping thus simple internal clamping circuitry is used.

Chrominance amplifiers

The chrominance amplifier has an asymmetrical input. The input signal must be a.c. coupled (pin 4) and have a minimum amplitude of 40 mV peak-to-peak. The gain control stage has a control range in excess of 30 dB, the maximum input signal must not exceed 1,1 V peak-to-peak, otherwise clipping of the input signal will occur. Form the gain control stage the chrominance signal is fed to the saturation control stage. Saturation is linear controlled via pin 5. The control voltage range is 2 to 4 V, the input impedance is high and the saturation control range is in excess of 50 dB. The burst signal is not affected by saturation control. The signal is then fed to a gated amplifier which has a 12 dB higher gain during the chrominance signal. As a result the signal at the output (pin 28) has a burst to chrominance ratio which is 6 dB lower than that of the input signal when the saturation control is set at −6 dB. The chrominance output signal is fed to the delay line and, after matrixing, is applied to the demodulator input pins (pins 22 and 23). These signals are fed to the burst phase detector.
In the case of NTSC the chroma signal is internally coupled to the demodulators, ACC and phase detector.

FUNCTIONAL DESCRIPTION (continued)

Oscillator and identification circuit

The burst phase detector is gated with the narrow part of the sandcastle pulse (pin 7). In the detector the (R-Y) and (B-Y) signals are added to provide the composite burst signal again. This composite signal is compared with the oscillator signal divided-by-2 ((R-Y) reference signal). The control voltage is available at pins 24 and 25, and is also applied to the 8,8 MHz oscillator. The 4,4 MHz signal is obtained via the divide-by-2 circuit, which generates both the (B-Y) and (R-Y) reference signals and provides a 90° phase shift between them.
The flip-flop is driven by pulses obtained from the sandcastle detector. For the identification of the phase at PAL mode, the (R-Y) reference signal coming from the PAL switch, is compared to the vertical signal (R-Y) of the PAL delay line. This is carried out in the H/2 detector, which is gated during burst. When the phase is incorrect, the flip-flop gets a reset from the identification circuit. When the phase is correct, the output voltage of the H/2 detector is directly related to the burst amplitude so that this voltage can be used for the a.c.c. To avoid 'blooming-up' of the picture under weak input signal conditions the a.c.c. voltage is generated by peak detection of the H/2 detector output signal.

The killer and identification circuits get their information from a gated output signal of the H/2 detector. Killing is obtained via the saturation control stage and the demodulators to obtain good suppression. The time constant of the saturation control (pin 5) provides a delayed switch-on after killing.
Adjustment of the oscillator is achieved by variation of the burst phase detector load resistance between pins 24 and 25 (see Fig. 7). With this application the trimmer capacitor in series with the 8,8 MHz crystal (pin 26) can be replaced by a fixed value capacitor to compensate for unbalance of the phase detector.

Demodulator

The (R-Y) and (B-Y) demodulators are driven by the colour difference signals from the delay-line matrix circuit and the reference signals from the 8,8 MHz divider circuit. The (R-Y) reference signal is fed via the PAL-switch. The output signals are fed to the R and B matrix circuits and to the (G-Y) matrix to provide the (G-Y) signal which is applied to the G-matrix. The demodulation circuits are killed and blanked by by-passing the input signals.

NTSC mode

The NTSC mode is switched on when the voltage at the burst phase detector outputs (pins 24 and 25) is adjusted below 9 V. To ensure reliable application the phase detector load resistors are external. When the TDA3566 is used only for PAL these two 33 kΩ resistors must be connected to + 12 V (see Fig. 7). For PAL/NTSC application the value of each resistor must be reduced to 10 kΩ and connected to the slider of a potentiometer (see Fig. 8). The switching transistor brings the voltage at pins 24 and 25 below 9 V which switches the circuit to the NTSC mode. The position of the PAL flip-flop ensures that the correct phase of the (R-Y) reference signal is supplied to the (R-Y) demodulator. The drive to the H/2 detector is now provided by the (B-Y) reference signal. (In the PAL mode it is driven by the (R-Y) reference signal.)
Hue control is realized by changing the phase of the reference drive to the burst phase detector. This is achieved by varying the voltage at pins 24 and 25 between 7,5 V and 8,5 V, nominal position 8,0 V. The hue control characteristic is shown in Fig. 5.

RGB matrix and amplifiers

The three matrix and amplifier circuits are identical and only one circuit will be described.
The luminance and the colour difference signals are added in the matrix circuit to obtain the colour signal, which is then fed to the contrast control stage. The contrast control voltage is supplied to pin 6 (high-input impedance). The control range is + 3 dB to −17 dB nominal. The relationship between the control voltage and the gain is linear (see Fig. 2).
During the 3-line period after blanking a pulse is inserted at the output of the contrast control stage. The amplitude of this pulse is varied by a control voltage at pin 11. This applies a variable offset to the normal black level, thus providing brightness control. The brightness control range is 1 V to 3 V.

While this offset level is present, the 'black-current' input impedance (pin 18) is high and the internal clamp circuit is activated. The clamp circuit then compares the reference voltage at pin 19 with the voltage developed across the external resistor network R_A and R_B (pin 18) which is provided by picture tube beam current. The output of the comparator is stored in capacitors connected from pins 10, 20 and 21 to ground which controls the black level at the output. The reference voltage is composed by the resistor divider network and the leakage current of the picture tube into this bleeder. During vertical blanking, this voltage is stored in the capacitor connected to pin 19, which ensures that the leakage current of the CRT does not influence the black current measurement.
The RGB output signals can never exceed a level of 10 V. When the signal tends to exceed this level the output signal is clipped. The black level at the outputs (pins 13, 15 and 17) will be about 3 V. This level depends on the spread of the guns of the picture tube. If a beam current stabilizer is not used it is possible to stabilize the black levels at the outputs, which in this application must be connected to the black current measuring input (pin 18) via a resistor network.

DEVELOPMENT DATA

Data insertion

Each colour amplifier has a separate input for data insertion. A 1 V peak-to-peak input signal provides a 4 V peak-to-peak output signal. To avoid the 'black-level' of the inserted signal differing from the black level of the normal video signal, the data is clamped to the black level of the luminance signal. Therefore a.c. coupling is required for the data inputs.
To avoid a disturbance of the blanking level due to the clamping circuit, the source impedance of the driver circuit must not exceed 150 Ω.
The data insertion circuit is activated by the data blanking input (pin 9). When the voltage at this pin exceeds a level of 0,9 V, the RGB matrix circuits are switched off and the data amplifiers are switched on. To avoid coloured edges, the data blanking switching time is short.
The amplitude of the data output signals is controlled by the contrast control at pin 6. The black level is equal to the video black level and can be varied between 2 and 4 V (nominal condition) by the brightness control voltage at pin 11.
Non-synchronized data signals do not disturb the black level of the internal signals.

Blanking of RGB and data signals

Both the RGB and data signals can be blanked via the sandcastle input (pin 7). A slicing level of 1,5 V is used for this blanking function, so that the wide part of the sandcastle pulse is separated from the remainder of the pulse. During blanking a level of + 1 V is available at the output.
To prevent parasitic oscillations on the third overtone of the crystal the optimal tuning capacitance should be 10 pF.

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Supply voltage (pin 1)	$V_P = V_{1-27}$	max.	13,2 V
Total power dissipation	P_{tot}	max.	1,7 W
Storage temperature range	T_{stg}	−25 to	+ 150 °C
Operating ambient temperature range	T_{amb}	−25 to	+ 70 °C

THERMAL RESISTANCE

From junction to ambient (in free air)	$R_{th\ j-a}$	=	40 K/W

CHARACTERISTICS

$V_P = V_{1-27} = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 1)					
Supply voltage	$V_P = V_{1-27}$	10,8	12	13,2	V
Supply current	$I_P = I_1$	–	80	110	mA
Total power dissipation	P_{tot}	–	0,95	1,3	W
Luminance amplifier (pin 8)					
Input voltage (note 1) (peak-to-peak value)	$V_{8-27(p-p)}$	–	0,45	0,63	V
Input level before clipping	V_{8-27}	–	–	1.4	V
Input current	I_8	–	0,1	1	μA
Contrast control range (see Fig. 2)		−15	–	+ 5	dB
Input current contrast control	I_7	–	–	15	μA
Chrominance amplifier (pin 4)					
Input voltage (note 2) (peak-to-peak value)	$V_{4-27(p-p)}$	40	390	1100	mV
Input impedance (pin 4)	$\lvert Z_{4-27} \rvert$	–	10	–	kΩ
Input capacitance	C_{4-27}	–	–	6,5	pF
A.C.C. control range		30	–	–	dB
Change of the burst signal at the output over the whole control range	ΔV	–	–	1	dB
Gain at nominal contrast/saturation pin 4 to pin 28 (note 3)	G	34	–	–	dB
Chrominance to burst ratio at nominal saturation (notes 2 and 3) at pin 28		–	12	–	dB
Maximum output voltage range (peak-to-peak value); $R_L = 2$ kΩ	$V_{28-27(p-p)}$	4	5	–	V
Distortion of chrominance amplifier at $V_{28-27(p-p)} = 2$ V (output) up to $V_{4-27(p-p)} = 1$ V (input)	d	–	–	5	%
Frequency response between 0 and 5 MHz	α_{28-4}	–	–	−2	dB
Saturation control range (see Fig. 3)		50	–	–	dB
Input current saturation control (pin 5)	I_5	–	–	20	μA
Cross-coupling between luminance and chrominance amplifier (note 4)		–	–	−46	dB
Signal-to-noise ratio at nominal input signal (note 5)	S/N	56	–	–	dB

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Chrominance amplifier (continued)					
Phase shift between burst and chrominance at nominal contrast/saturation	$\Delta\varphi$	–	–	± 5	deg
Output impedance of chrominance amplifier	$\lvert Z_{28\text{-}27}\rvert$	–	10	–	Ω
Output current	I_{28}	–	–	15	mA
Reference part					
Phase-locked-loop catching range (note 6)	Δf	500	700	–	Hz
phase shift for ± 400 Hz deviation of f_{osc} (note 6)	$\Delta\varphi$	–	–	5	deg
Oscillator					
temperature coefficient of oscillator frequency (note 6)	TC_{osc}	–	−2	−3	Hz/K
frequency variation when supply voltage increases from 10 to 13,2 V (note 6)	Δf_{osc}	–	40	100	Hz
input resistance (pin 26)	$R_{26\text{-}27}$	280	400	520	Ω
input capacitance (pin 26)	$C_{26\text{-}27}$	–	–	10	pF
A.C.C. generation (pin 2)					
→ control voltage at nominal input signal	$V_{2\text{-}27}$	–	4,5	–	V
→ control voltage without chrominance input	$V_{2\text{-}27}$	–	2	–	V
→ colour-off voltage	$V_{2\text{-}27}$	–	2,8	–	V
→ colour-on voltage	$V_{2\text{-}27}$	–	3	–	V
→ identification-on voltage	$V_{2\text{-}27}$	–	1,7	–	V
change in burst amplitude with temperature		–	0,1	0,25	%/K
voltage at pin 3 at nominal input signal	$V_{3\text{-}27}$	–	5,1	–	V
Demodulator part					
Input burst signal amplitude (peak-to-peak value between pins 23 and 27 (note 7)	$V_{23\text{-}27(p\text{-}p)}$	68	80	95	mV
Input impedance between pins 22 or 23 and 27	$\lvert Z_{22\text{-}27/23\text{-}27}\rvert$	0,7	1	1,3	kΩ
Ratio of demodulated signals (note 8)					
(B-Y)/(R-Y)	$\frac{V_{17\text{-}27}}{V_{13\text{-}27}}$	–	1,78 ± 10%	–	
(G-Y)/(R-Y); no (B-Y) signal	$\frac{V_{15\text{-}27}}{V_{13\text{-}27}}$	–	−0,51 ± 10%	–	
(G-Y)/(B-Y); no (R-Y) signal	$\frac{V_{15\text{-}27}}{V_{17\text{-}27}}$	–	−0,19 ± 10%	–	

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Demodulator part (continued)					
Frequency response between 0 and 1 MHz	α_{17}	–	–	–3	dB
Cross-talk between colour difference signals		40	–	–	dB
Phase difference between (R-Y) signal and (R-Y) reference signals	$\Delta\varphi$	–	–	5	deg
Phase difference between (R-Y) signal and (B-Y) reference signals	$\Delta\varphi$	85	90	95	deg
RGB matrix and amplifiers					
Output voltage (peak-to-peak value) at nominal luminance/contrast (black-to-white) (note 3)	$V_{13,15,17\text{-}27(p\text{-}p)}$	3,5	4	4,5	V
Output voltage at pin 13 (peak-to-peak value) at nominal contrast/saturation and no luminance signal to (R-Y)	$V_{13\text{-}27(p\text{-}p)}$	–	4,2	–	V
Maximum peak-white level	$V_{13,15,17\ (m)}$	9,7	10	10,3	V
Available output current (pins 13, 15 17)	$I_{13,15,17}$	10	–	–	mA
Difference between black level and measuring level at the output for a brightness control voltage at pin 11 of 2 V (note 9)	$\Delta V_{13,15,17\text{-}27}$	–	0	–	V
Difference in black level between the three channels without black current stabilization (note 10)	ΔV	–	–	100	mV
Control range of black-current stabilization at V_{b1} = 3 V; $V_{11\text{-}17}$ = 2 V		–	–	± 2	V
Black level shift with vision contents	ΔV	–	–	40	mV
Brightness control voltage range		see Fig. 4			
Brightness control input current	I_{11}	–	–	5	μA
Variation of black level with temperature	$\Delta V/\Delta T$	–	0	–	mV/K
Variation of black level with contrast*	ΔV	–	–	100	mV
Relative spread between the R, G and B output signals		–	–	10	%
Relative black-level variation between the three channels during variation of contrast, brightness and supply voltage (± 10%)*	ΔV	–	0	20	mV
Differential black-level drift over a temperature range of 40 °C	ΔV	–	0	20	mV
Blanking level at the RGB outputs	V_{bl}	–	0,95	1,1	V

* With respect to the measuring pulses.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
RGB matrix and amplifiers (continued)					
Difference in blanking level of the three channels	V_{bl}	–	0	–	mV
Differential drift of the blanking levels over a temperature range of 40 °C	V_{bl}	–	0	10	mV
Tracking of output black level with supply voltage	$\frac{\Delta V_{bl}}{V_{bl}} \times \frac{V_P}{\Delta V_P}$	0,9	1	1,1	
Tracking of contrast control between the three channels over a control range at 10 dB		–	–	0,5	dB
Output signal during the clamp pulse (3L) after switch-on	V_O	7,5	–	–	V
Signal-to-noise ratio of output signals (note 5)	S/N	62	–	–	dB
Residual 4,4 MHz signal at RGB outputs (peak-to-peak value)	$V_{R(p-p)}$	–	–	50	mV
Residual 8,8 MHz signal and higher harmonics at the RGB outputs (peak-to-peak value)	$V_{R(p-p)}$	–	–	150	mV
Output impedance of RGB outputs	$\lvert Z_{13,15,17-27} \rvert$	–	50	–	Ω
Frequency response of total luminance and RGB amplifier circuits for f = 0 to 9 MHz	α	–	−1	−3	dB
Current source of output stage	I_O	2	3	–	mA
Difference of black level at the three outputs at nominal brightness*	ΔV	–	–	10	mV
Tracking of brightness control		–	–	2	%
Signal insertion (pins 12, 14 and 16)					
Input signals (peak-to-peak value) for and RGB output voltage of 3.5 V (peak-to-peak) at nominal contrast	$V_{12,14,16-27(p-p)}$	0,9	1	1,1	V
Difference between the black levels of the RGB signals and the inserted signals at the output (note 11)	ΔV	–	–	100	mV
Output rise time	t_r	–	50	80	ns
Differential delay time for the three channels	t_d	–	0	40	ns
Input current	$I_{12,14,16}$	–	–	10	μA

* With respect to the measuring pulses.

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Data blanking (pin 9)					
Input voltage for no data insertion	$V_{9\text{-}27}$	–	–	0,4	V
Input voltage for data insertion	$V_{9\text{-}27}$	0,9	–	–	V
Maximum input voltage	$V_{9\text{-}27(m)}$	–	–	3	V
Delay of data blanking	t_d	–	–	20	ns
Input resistance	$R_{9\text{-}27}$	7	10	13	kΩ
Suppression of the internal RGB signals when $V_{9\text{-}27} > 0{,}9$ V		46	–	–	dB
Sandcastle input (pin 7)					
Level at which the RGB blanking is activated	$V_{7\text{-}27}$	1	1,5	2	V
Level at which the horizontal pulses are separated	$V_{7\text{-}27}$	3	3,5	4	V
Level at which burst gating and clamping pulse are separated	$V_{7\text{-}27}$	6,5	7,0	7,5	V
Delay between black level clamping and burst gating pulse	t_d	–	0,6	–	µs
Input current					
at $V_{7\text{-}27}$ = 0 to 1 V	$-I_7$	–	–	1	mA
at $V_{7\text{-}27}$ = 1 to 8,5 V	I_7	–	–	50	µA
at $V_{7\text{-}27}$ = 8,5 to 12 V	I_7	–	–	2	mA
Black current stabilization (pin 18)					
Bias voltage (d.c.)	$V_{18\text{-}27}$	3,5	5	7,0	V
Difference between input voltage for 'black' current and leakage current	ΔV	0,35	0,5	0,65	V
Input current during 'black' current	I_{18}	–	–	1	µA
Input current during scan	I_{18}	–	–	10	mA
Internal limiting at pin 10	$V_{18\text{-}27}$	8,5	9	9,5	V
Switching threshold for 'black' current control ON	$V_{18\text{-}27}$	7,6	8	8,4	V
Input resistance during scan	$R_{18\text{-}27}$	1	1,5	2	kΩ
Input current during scan at pins 10, 20 and 21 (d.c.)	$I_{10,\ 20,\ 21}$	–	–	tbf	nA
Maximum charge/discharge current during measuring time		–	1	–	nA
NTSC					
Level at which the PAL/NTSC switch is activated (pins 24 and 25)	$V_{24\text{-}25}$	–	8,8	9,2	V
Average output current (note 12)	$I_{24\,+\,25(AV)}$	75	90	105	µA
Hue control		see Fig. 5			

Notes to the characteristics

1. Signal with the negative-going sync; amplitude includes sync amplitude.
2. Indicated is a signal for a colour bar with 75% saturation; chrominance to burst ratio is 2,2 : 1.
3. Nominal contrast is specified as the maximum contrast −5 dB and nominal saturation as the maximum saturation −6 dB.
4. Cross coupling is measured under the following condition: input signal nominal, contrast and saturation such that nominal output signals are obtained. The signals at the output at which no signal should be available must be compared with the nominal output signal at that output.
5. The signal-to-noise ratio is defined as peak-to-peak signal with respect to r.m.s. noise.
6. All frequency variations are referred to 4,4 MHz carrier frequency.
7. These signal amplitudes are determined by the a.c.c. circuit of the reference part.
8. The demodulators are driven by a chrominance signal of equal amplitude for the (R-Y) and the (B-Y) components. The phase of the (R-Y) chrominance signal equals the phase of the (R-Y) reference signal. This also applies to the (B-Y) signals.
9. This value depends on the gain setting of the RGB output amplifiers and the drift of the picture tube guns. Higher black level values are possible (up to 5 V) but in that application the amplitude of the output signal is reduced.
10. The variation of the black-level during brightness control in the three different channels is directly dependent on the gain of each channel. Discolouration during adjustments of contrast and brightness does not occur because amplitude and the black-level change with brightness control are directly related.
11. This difference occurs when the source impedance of the data signals is 150 Ω and the black level clamp pulse width is 4 μs (sandcastle pulse). For a lower impedance the difference will be lower.
12. The voltage at pins 24 and 25 can be changed by connecting the load resistors (10 kΩ in this application) to the slider bar of the hue control potentiometer (see Fig. 8). When the transistor is switched on, the voltage at pins 24 and 25 is reduced below 9 V, and the circuit is switched to NTSC mode. The width of the burst gate is assumed to be 4 μs typical.

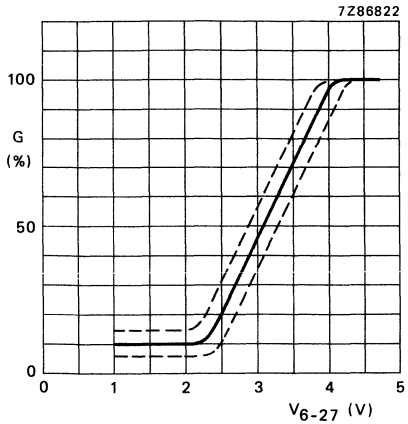


Fig. 2 Contrast control voltage range.

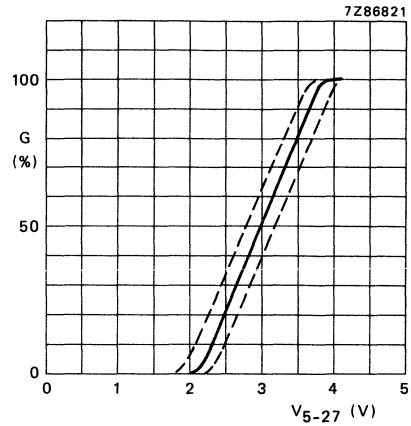


Fig. 3 Saturation control voltage range.

DEVELOPMENT DATA

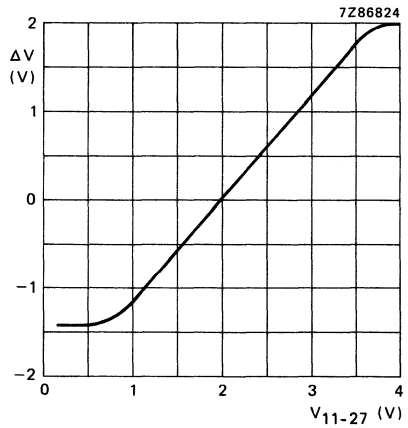


Fig. 4 Difference between black level and measuring level at the RGB outputs (ΔV) as a function of the brightness control input voltage (V_{11-27}).

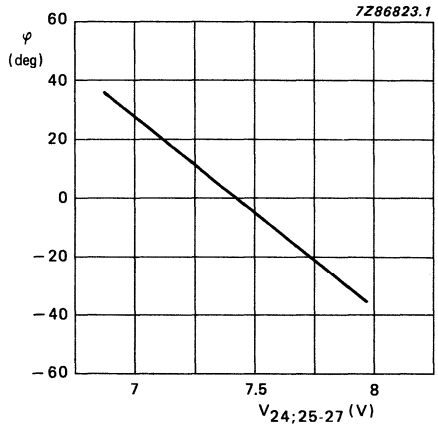


Fig. 5 Hue control voltage range.

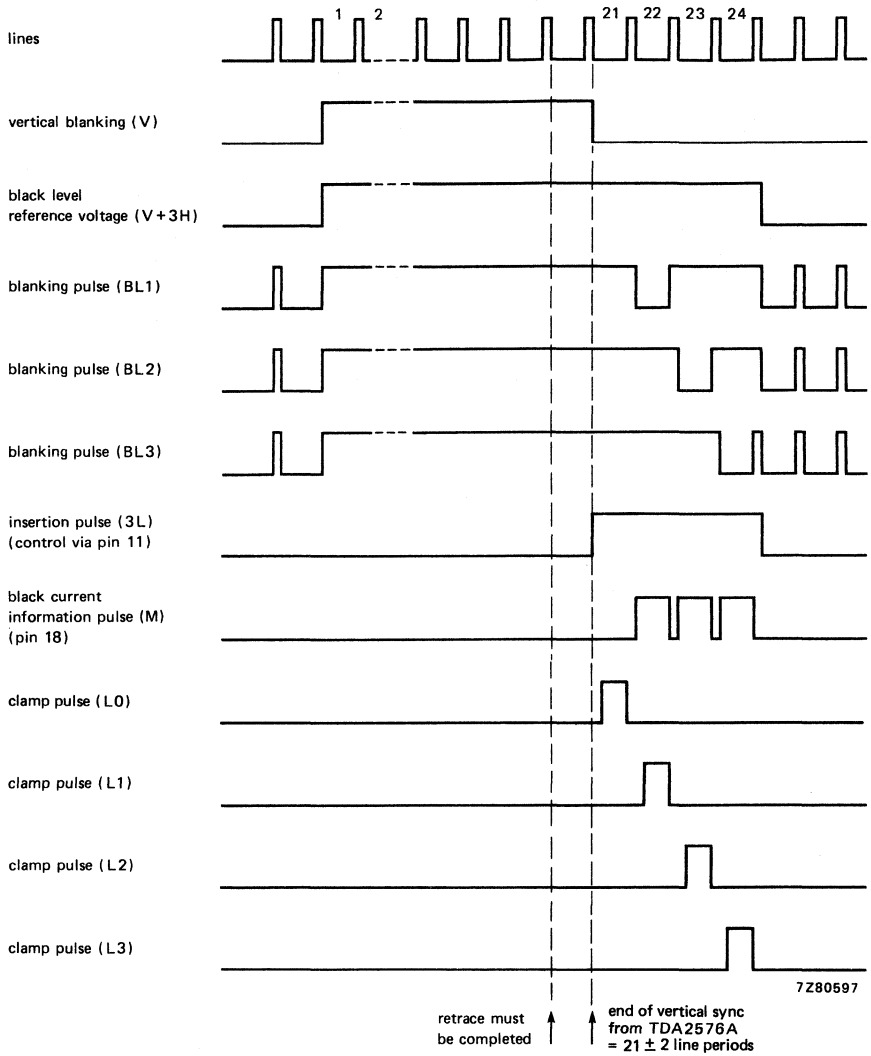


Fig. 6 Timing diagram for black-current stabilizing.

DEVELOPMENT DATA

APPLICATION INFORMATION

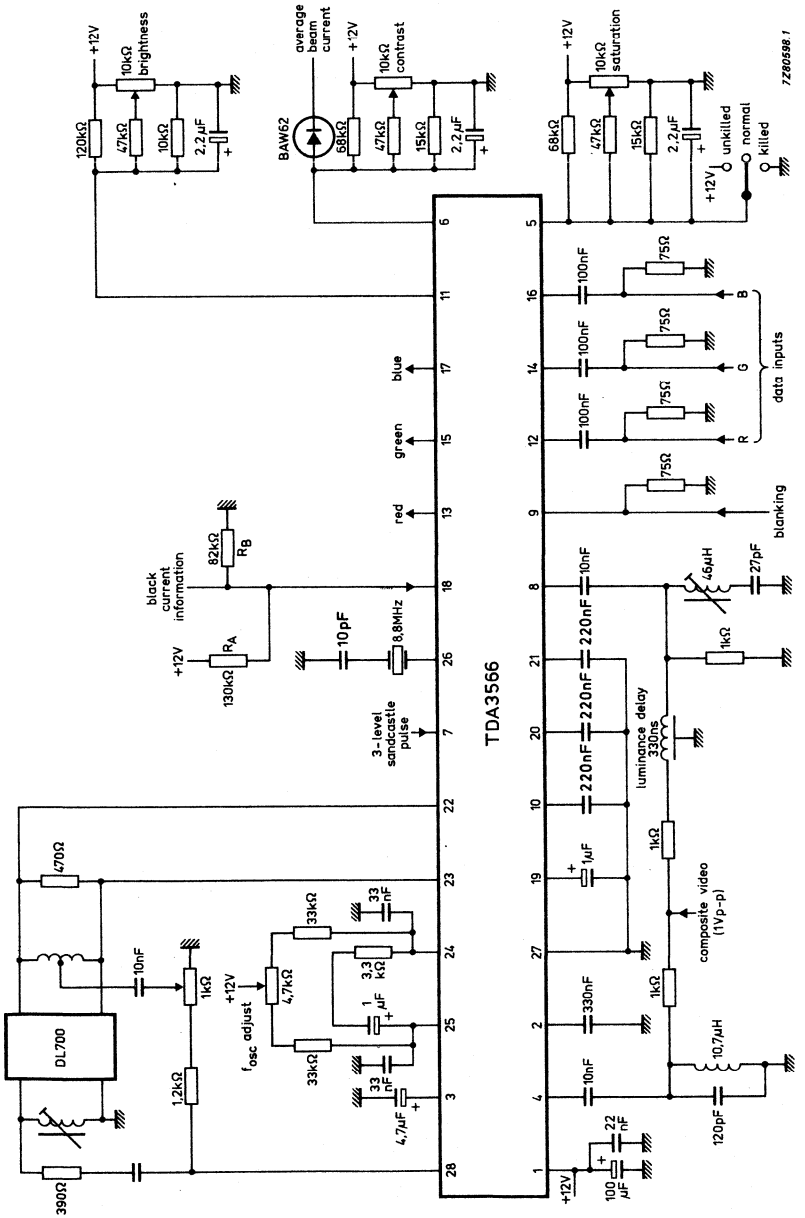


Fig. 7 Application diagram showing the TDA3566 for a PAL decoder.

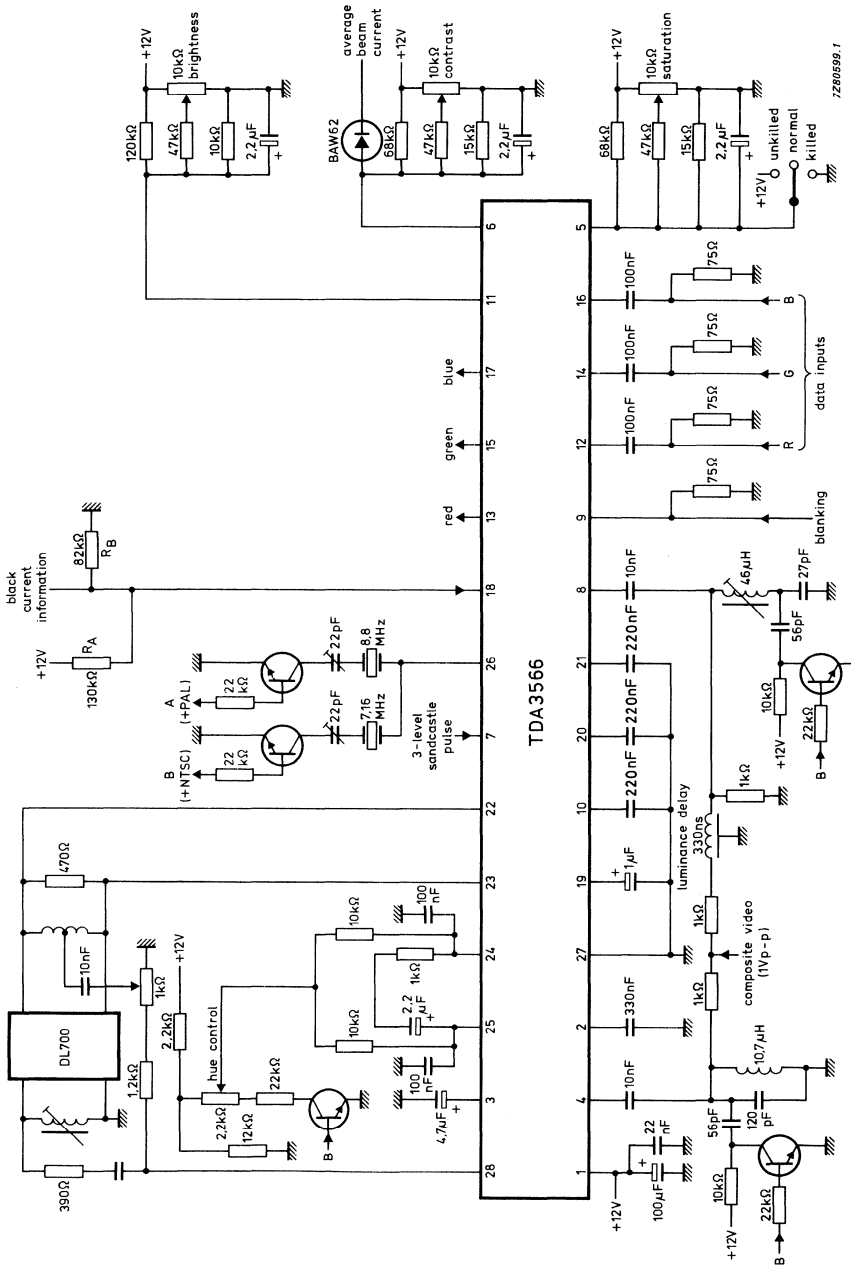


Fig. 8 Application diagram showing the TDA3566 for a PAL/NTSC decoder.

DEVELOPMENT DATA

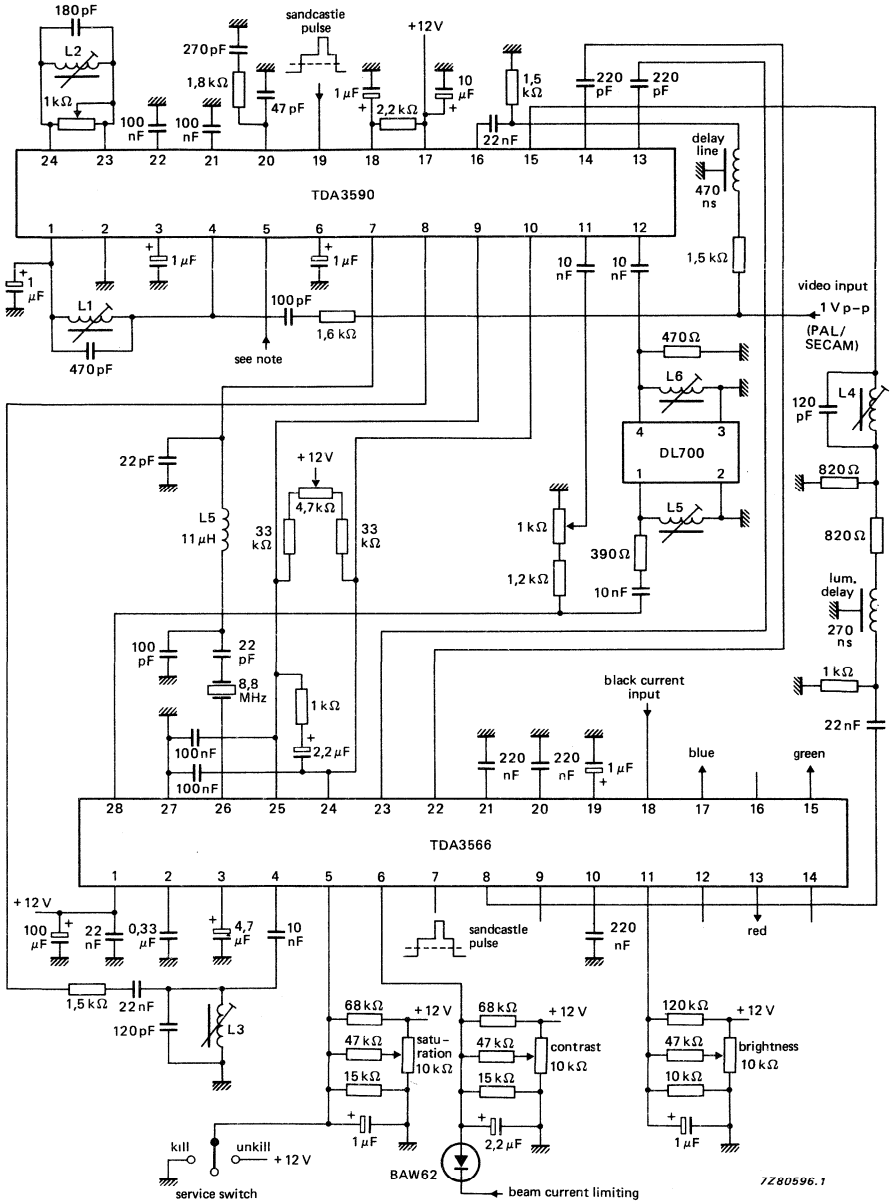


Fig. 9 PAL/SECAM application circuit diagram using the TDA3590 and TDA3566.

Note to pin 5 TDA3590:

$V_{5\text{-}2} < 1$ V; horizontal identification and black level clamping.
$V_{5\text{-}2} > 11$ V; vertical identification and artificial black level.
$V_{5\text{-}2} = 5$ to 7 V; horizontal identification and artificial black level.

NTSC DECODER

GENERAL DESCRIPTION

The TDA3567 is a monolithic integrated decoder for the NTSC colour television standards. It combines all functions required for the demodulation of NTSC signals. Further more it contains a luminance amplifier, an RGB-matrix and amplifier. These amplifiers supply output signals up to 5 V peak-to-peak (picture information) enabling direct drive of the discrete output stages.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 1	$V_P = V_{1-17}$	9	12	13,2	V
Supply current	pin 1	$I_P = I_1$	–	65	–	mA
Luminance input signal	pin 8					
Input voltage (peak-to-peak value)		$V_{8-17(p-p)}$	–	0,45	–	V
Contrast control range			–	20	–	dB
Chrominance amplifier	pin 3					
Input voltage (peak-to-peak value)		$V_{3-17(p-p)}$	–	550	–	mV
Saturation control range			50	–	–	dB
RGB matrix and amplifiers						
Output voltage at nominal luminance input signal and nominal contrast (peak-to-peak value)		$V_{10,11,12-17(p-p)}$	4,0	5,0	6,0	V
Sandcastle input	pin 7					
Blanking input voltage		V_{7-17}	1,0	1,5	2,0	V
Burst gating and clamping input voltage		$V_{7-17(p-p)}$	6,5	7,0	7,5	V

PACKAGE OUTLINE

18-lead DIL; plastic, with internal heatspreader (SOT102).

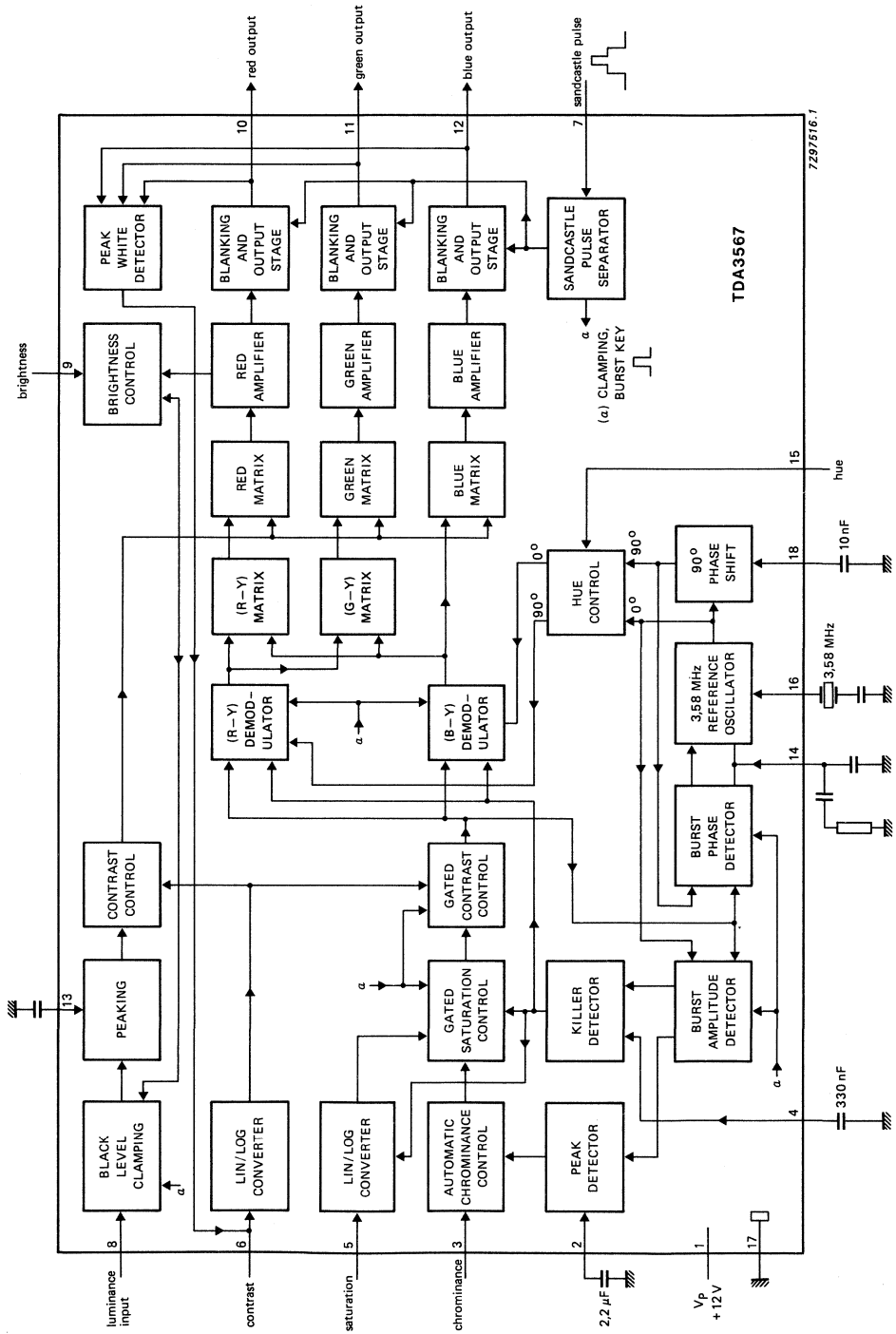


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

Luminance amplifier

The luminance amplifier is voltage driven and requires an input signal of 450 mV peak-to-peak*. The luminance delay line must be connected between the i.f. amplifier and the decoder. The input signal must be a.c. coupled to the input pin 8.

The black level clamp circuit of the RGB amplifiers uses the coupling capacitor as a storage capacitor. After clamping the signal is fed to a peaking stage. The RC network connected to pin 13 is used to define the amount of overshoot.

The peaking stage is followed by a contrast control stage. The control voltage has to be supplied to pin 6. The control voltage range is nominally −17 to + 3 dB. The linear curve of the contrast control voltage is shown in Fig. 2.

Chrominance amplifier

The chrominance amplifier has an asymmetrical input. The input signal at pin 3 must be a.c. coupled, and must have an amplitude of 550 mV peak-to-peak. The gain control stage has a control range in excess of 30 dB, the maximum input signal should not exceed 1,1 V peak-to-peak, otherwise clipping of the input signal will occur. From the gain control stage the chrominance signal is fed to the saturation and contrast control stages. Chrominance and luminance control stages are directly coupled to obtain good tracking. The saturation is linearly controlled via pin 5. The control voltage range is 2 V to 4 V. The impedance is high and the saturation control range is in excess of 50 dB. The burst signal is not affected by contrast or saturation control. After the amplification and control stages the chrominance signal is internally fed to the (R-Y) and (B-Y) demodulators, burst phase and a.c.c. detectors.

Oscillator and a.c.c. circuit

The 3,58 MHz reference oscillator operates at the subcarrier frequency. The crystal must be connected between pin 16 and ground. The oscillator does not require adjustment due to the small spreads of the IC. The free running frequency of the oscillator can be checked by connecting the saturation control (pin 5) to the positive supply line. Then the loop is opened, so that the frequency can be measured. The oscillator has an internal gain limiting stage which controls the gain to unity, so that internal signals are sinusoidal. This prevents the generation of higher harmonics of the subcarrier signals. The burst signal is compared to a 0^{o} reference signal by the burst amplitude detector and is then amplified and fed to a peak detector for a.c.c. and to a sample and hold circuit which drives the colour killer circuit. The reference signal for the burst phase detector is provided by the 90^{o} phase shifted signal. An RC network is used to obtain the required catching range and noise immunity for the output voltage of the burst phase detector.

The hue control is obtained by mixing oscillator signals with a phase of 0^{o} and 90^{o} before they are fed to the (R-Y) and (B-Y) demodulators. The 90^{o} phase shifted signal is provided by a miller integrator (biased by pin 18). As the hue control is independent of the PLL, the control will react without time delay on the control voltage changes.

DEVELOPMENT DATA

* Signal with negative going sync; amplitude includes sync pulse amplitude.

FUNCTIONAL DESCRIPTION (continued)

Demodulator circuits

The demodulators are driven by the amplified and controlled chrominance signals, the reference signals are obtained from the hue control circuit. In nominal hue control position the phase angle of (R-Y) reference signal is 0^o, the phase angle of the (B-Y) reference signal is 90^o.

For flesh tone corrections the demodulated (R-Y) signal is matrixed with the demodulated (B-Y) signal according to the following equations:

$$(R\text{-}Y)_{matrixed} = 1{,}61\ (R\text{-}Y)_{IN} - 0{,}42\ (B\text{-}Y)_{IN}$$

$$(G\text{-}Y)_{matrixed} = 0{,}43\ (R\text{-}Y)_{IN} - 0{,}11\ (B\text{-}Y)_{IN}$$

$$(B\text{-}Y)_{matrixed} = (B\text{-}Y)_{IN}$$

In these equations $(R\text{-}Y)_{IN}$ and $(B\text{-}Y)_{IN}$ indicate the colour difference signal amplitudes, when the chrominance signal is demodulated with a phase difference between the R-Y and B-Y demodulator of 90^o and a gain ratio B-Y/R-Y = 1,78.

RGB matrix circuit and amplifiers

The three matrix and amplifier circuits are identical. The luminance signal and the colour difference signals are added in the matrix circuit to obtain the colour signal.

Output signals are 5 V (peak-to-peak) (black-white) for the following nominal input signals and control settings.

- Luminance 450 mV (peak-to-peak)
- Chrominance 550 mV (peak-to-peak) (burst-to-chrominance ratio of the input 1 : 2.2)
- Contrast −3 dB (maximum)
- Saturation −10 dB (maximum)

The maximum available output voltage is approximately 7 V (peak-to-peak). The black level of the red channel is compared with a variable external reference level (pin 9), which provides the brightness control. The control loop is closed via the luminance input.

The luminance input is varied to control the black level control, therefore the green and blue outputs will follow any variation of the red output. The output of the black control can be varied between 2 V to 4 V. The corresponding brightness control voltage is shown in Fig. 4.

If the output signal surpasses the level of 9 V the peak-white limiter circuit becomes active and reduces the output signal via the contrast control.

Blanking of RGB signals

A slicing level of about 1,5 V is used for this blanking function, so that the wide part of the sandcastle pulse is separated from the rest of the pulse. During blanking a level of + 2 V is available at the output.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 1)	$V_P = V_{1-17}$	max.	13,2 V
Total power dissipation	P_{tot}	max.	1,7 W
Storage temperature range	T_{stg}	−25 to + 150	°C
Operating ambient temperature range	T_{amb}	−25 to + 65	°C

THERMAL RESISTANCE

From junction to ambient (in free air)	$R_{th\ j-a}$	=	50 K/W

CHARACTERISTICS

$V_P = V_{1-17} = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		$V_P = V_{1-17}$	9	12	13,2	V
Supply current		$I_P = I_1$	–	65	–	mA
Total power dissipation		P_{tot}	–	0,78	–	W
Luminance input signal						
Input voltage (peak-to-peak value)	note 1 pin 8	$V_{8-17(p-p)}$	–	450	–	mV
Input voltage level before clipping occurs in the input stage		V_{8-17}	–	–	1	V
Input current		I_8	–	0,15	1,0	μA
Contrast control range	see Fig. 2		−17	–	+ 3	dB
Input current contrast control	for $V_{6-17} < 6$ V	I_7	–	0,5	15	μA
Input current when the peak-white limiter is active	$V_{6-17} = 2,5$ V	I_7	–	5,5	–	mA
Input resistance	$V_{6-17} > 6$ V	R_{7-17}	1,4	2,0	2,6	kΩ
Peaking of luminance signal						
Output impedance	pin 13	$\lvert Z_{13-17} \rvert$	–	200	–	Ω
Ratio of internal/external current when pin 13 is short-circuited			–	3	–	

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Chrominance amplifier						
Input signal amplitude (peak-to-peak value)	note 2 pin 3	$V_{3\text{-}17(p\text{-}p)}$	–	550	–	mV
Input signal amplitude before clipping occurs in the input stage (peak-to-peak value)		$V_{3\text{-}17(p\text{-}p)}$	–	–	1,1	V
Minimum burst signal amplitude within the a.c.c. control range (peak-to-peak)			35	–	–	mV
A.C.C. control range			30	–	–	dB
Change of the burst signal at the output for the complete control range		ΔV	–	–	+ 1	dB
Input impedance	pin 3	$\lvert Z_{3\text{-}17}\rvert$	6	8	10	kΩ
Input capacitance	pin 3	$C_{3\text{-}17}$	–	4	6	pF
Saturation control range	see Fig. 3		50	–	–	dB
Input current saturation control	for $V_{5\text{-}17} > 6$ V	I_5	–	1	20	μA
Input impedance	$V_{5\text{-}17} = 6$ V to 10 V	$\lvert Z_{5\text{-}17}\rvert$	1,4	2,0	2,6	kΩ
Input impedance when the colour killer is active		$\lvert Z_{5\text{-}17}\rvert$	1,4	2,0	2,6	kΩ
Input impedance	for $V_{5\text{-}17} > 10$ V	$\lvert Z_{5\text{-}17}\rvert$	0,7	1,0	1,3	kΩ
Tracking between luminance and chrominance contrast	for 10 dB of control		–	1	2	dB
Cross coupling between luminance and chrominance amplifier	note 4		–	–50	–46	dB
Reference part						
Phase locked loop						
Catching range		Δf	±400	±500	–	Hz
Phase shift for 400 Hz deviation of the carrier frequency		Δ	–	–	5	deg

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator						
Temperature coefficient of oscillator frequency		TC_{osc}	–	1,5	2,5	Hz/K
Frequency deviation	$\Delta V_P = \pm 10\%$	Δf_{osc9}	–	150	250	Hz
Input resistance	pin 16	$R_{16\text{-}17}$	260	360	460	Ω
Input capacitance	pin 16	$C_{22\text{-}17}$	–	–	10	pF
A.C.C. generation						
Voltage at pin 4 nominal input signal		$V_{4\text{-}17}$	–	4,0	–	V
Voltage at pin 4 without burst input		$V_{4\text{-}17}$	–	1,9	–	V
Colour-off voltage		$V_{4\text{-}17}$	–	2,5	–	V
Colour-on voltage		$V_{4\text{-}17}$	–	2,8	–	V
Change in burst amplitude with temperature			–	0,1	–	%/K
Change in burst amplitude with 10% supply voltage change			–	0	–	%/V
Voltage at pin 2 at nominal input signal		$V_{2\text{-}17}$	–	5,0	–	V
Hue control						
Control voltage range			see Fig. 5			
Input current	for $V_{15\text{-}17} < 5$ V	I_{14}	–	0,5	20	μA
Input impedance	for $V_{15\text{-}17} > 5$ V	$\lvert Z_{14\text{-}17}\rvert$	1,5	2,5	3,5	kΩ
Demodulation part						
Ratio of demodulation signals (measured at the various outputs)	note 7					
(R-Y)/(B-Y); no (R-Y) signal		$\frac{V_{10\text{-}17}}{V_{12\text{-}17}}$	–	–0,42	–	
(R-Y)/(B-Y); colour bar signal		$\frac{V_{10\text{-}17}}{V_{12\text{-}17}}$	–	1,4	–	
(G-Y)/(R-Y); no (B-Y) signal		$\frac{V_{11\text{-}17}}{V_{12\text{-}17}}$	–	–0,25	–	
(G-Y)/(B-Y); no (R-Y) signal		$\frac{V_{11\text{-}17}}{V_{12\text{-}17}}$	–	–0,11	–	
Frequency response	0 to 0,7 MHz		–	–	–3	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
RGB matrix and amplifier						
Output signal amplitude	at nominal luminance input signal and nominal contrast (peak-to-peak value) note 3 black-white	$V_{10,11,12-17(p-p)}$	4,0	5,0	6,0	V
Output signal amplitude of the "blue" channel	at nominal contrast and saturation control setting and no luminance signal to the input (B-Y) signal (peak-to-peak value)	$V_{12-17(p-p)}$	–	3,8	–	V
Maximum peak-white level	note 6	$V_{10,11,12-7}$	9,0	9,3	9,6	V
Maximum output current		$I_{10,11,12-17}$	–	–	10	mA
Difference in the black level between the three channels			–	–	600	mV
Black level shift with vision content			–	10	40	mV
Brightness control voltage range			see Fig. 4			
Brightness control input current		I_9	–	–	–50	μA
Black level variation with temperature		V/T	–	0,15	1,0	mV/K
Black level variation with contrast control		ΔV	–	75	200	mV
Relative spread between the three output signals			–	–	10	%
Relative variation in black level between the three channels	during variations of contrast (10 dB), brightness (± 1 V), and supply voltage (± 10%)	ΔV	–	0	20	mV
Differential drift of black level over a temperature range of 40 °C		ΔV	–	0	20	mV
Blanking level at the RGB outputs		V_{b1}	1,95	2,15	2,35	V

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Tracking of output black levels with supply voltage		$\frac{\Delta V_{b1}}{V_{b1}} \times \frac{V_P}{\Delta V_P}$	1,0	1,05	1,1	
Signal-to-noise ratio of output signals	note 5	S/N	62	–	–	dB
Residual 3,58 MHz in RGB outputs (peak-to-peak value)		$V_{R(p\text{-}p)}$	–	50	75	mV
Residual 7,1 MHz and higher harmonics in the RGB outputs (peak-to-peak value)		$V_{R(p\text{-}p)}$	–	50	75	mV
RGB output impedance		$\lvert Z_{10,11,12\text{-}17} \rvert$	–	–	50	
Frequency response of total luminance and RGB amplifier circuits	0 to 5 MHz		–	–	–3	dB
Sandcastle input						
Level at which the RGB blanking is activated		$V_{7\text{-}17}$	1,0	1,5	2,0	V
Level at which burst gate clamping pulses are separated		$V_{7\text{-}17}$	6,5	7,0	7,5	V
Delay between black level clamping and burst gating pulse		t_d	300	375	450	ns
Input currents	$V_{7\text{-}17}$ = 0 to 1 V	I_7	–	–	–1	mA
	$V_{7\text{-}17}$ = 1 to 8,5 V	I_7	–	–20	–40	μA
	$V_{7\text{-}17}$ = 8,5 to 12 V	I_7	–	–	2	mA

Noted to the characteristics

1. Signal with negative going sync; amplitude includes sync pulse amplitude.
2. Indicated is a signal for colour bar with 75% saturation, so the chrominance to burst ratio is 2,2 : 1.
3. Nominal contrast is specified as maximum contrast –3 dB and nominal saturation as maximum saturation –10 dB.
4. Cross coupling is measured under the following condition:
   - input signals nominal;
   - contrast and saturation such that nominal output signals are obtained;
   - the signals at the output at which no signal should be available must be compared with the nominal output signal at that output.
5. The signal-to-noise ratio is specified as peak-to-peak signal with respect to RMS noise.
6. When this level is exceeded the amplifier of the output signal is reduced via a discharge of the capacitor on pin 7 (contrast control). Discharge current is 5,5 mA.
7. These matrixed values are found by measuring the ratio of the various output signals. The values are derived from the matrix equations given in the section 'FUNCTIONAL DESCRIPTION'.

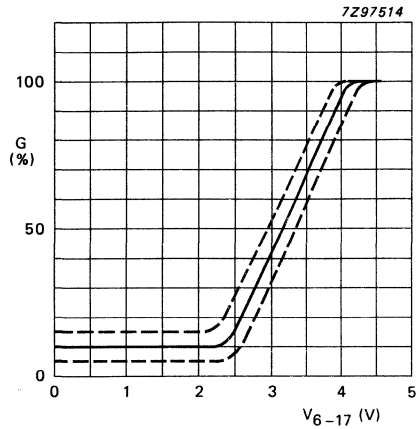


Fig. 2 Contrast control voltage range.

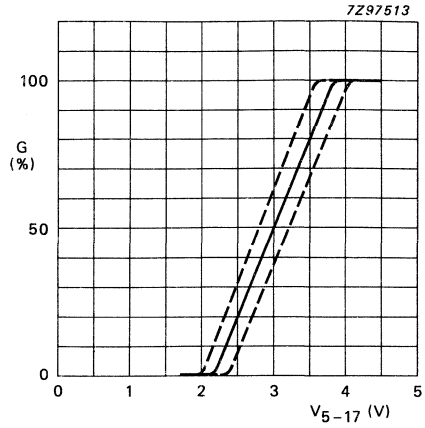


Fig. 3 Saturation control voltage range.

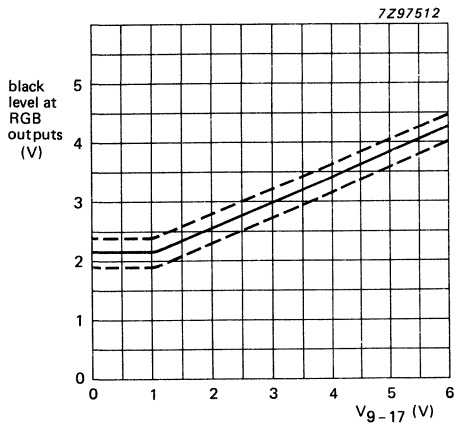


Fig. 4 Brightness control voltage range.

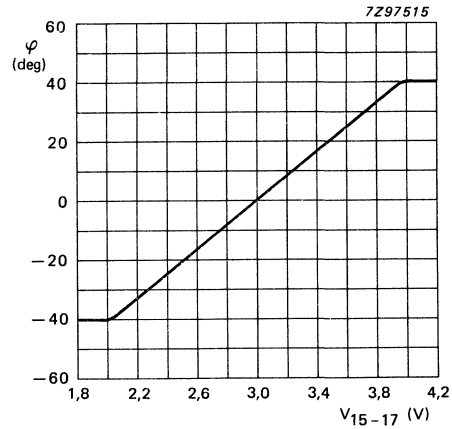


Fig. 5 Hue control voltage range.

APPLICATION INFORMATION

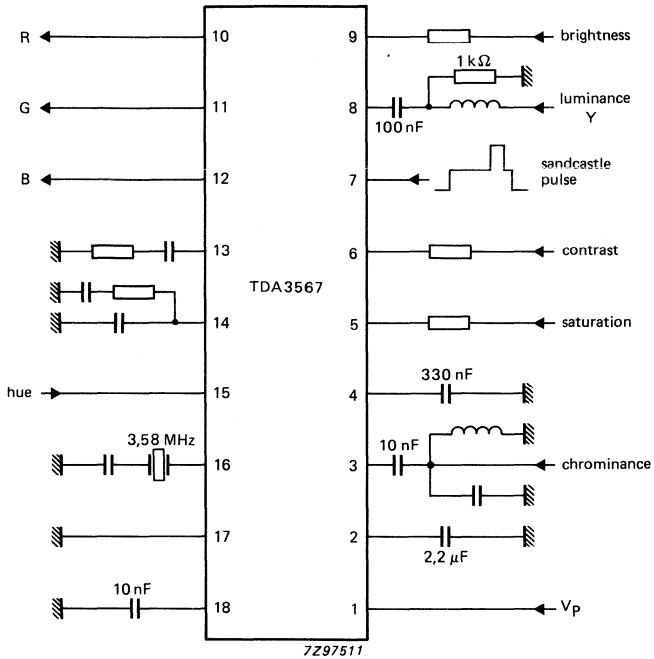


Fig. 6 Application diagram.

DEVELOPMENT DATA

NTSC DECODER WITH FAST RGB BLANKING

GENERAL DESCRIPTION

The TDA3569 NTSC decoder combines luminance amplifier, RGB matrix and RGB amplifiers to provide NTSC demodulation and direct drive of discrete output stages. A facility for fast blanking of the RGB outputs is included.

Features

- Automatic chrominance levelling (avoids saturation at chrominance input)
- Peaking circuit with d.c. control
- Fast RGB output blanking

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit	
Supply voltage		$V_P = V_{1-19}$	10,8	12	13,2	V	
Supply current		I_1	–	80	–	mA	←
Luminance input signal							
Input voltage (peak-to-peak value)		$V_{8-19(p-p)}$	–	450	–	mV	
Contrast control range			–	−17 to +3	–	dB	
Chrominance amplifier							
Input voltage (peak-to-peak value)		$V_{3-19(p-p)}$	–	550	–	mV	
Saturation control range			50	–	–	dB	
RGB matrix							
Output voltage (peak-to-peak value)	nominal luminance signal and nominal contrast (black-white)	$V_{12,13,14-19}$	4	5	6	V	
Sandcastle input							
RGB slicing level		V_{7-19}	1,0	1,5	2,0	V	←
Burst gate/clamping pulse separation level		V_{7-19}	6,5	7,0	7,5	V	

PACKAGE OUTLINE

20-lead DIL; plastic with internal heat-spreader (SOT146EE7).

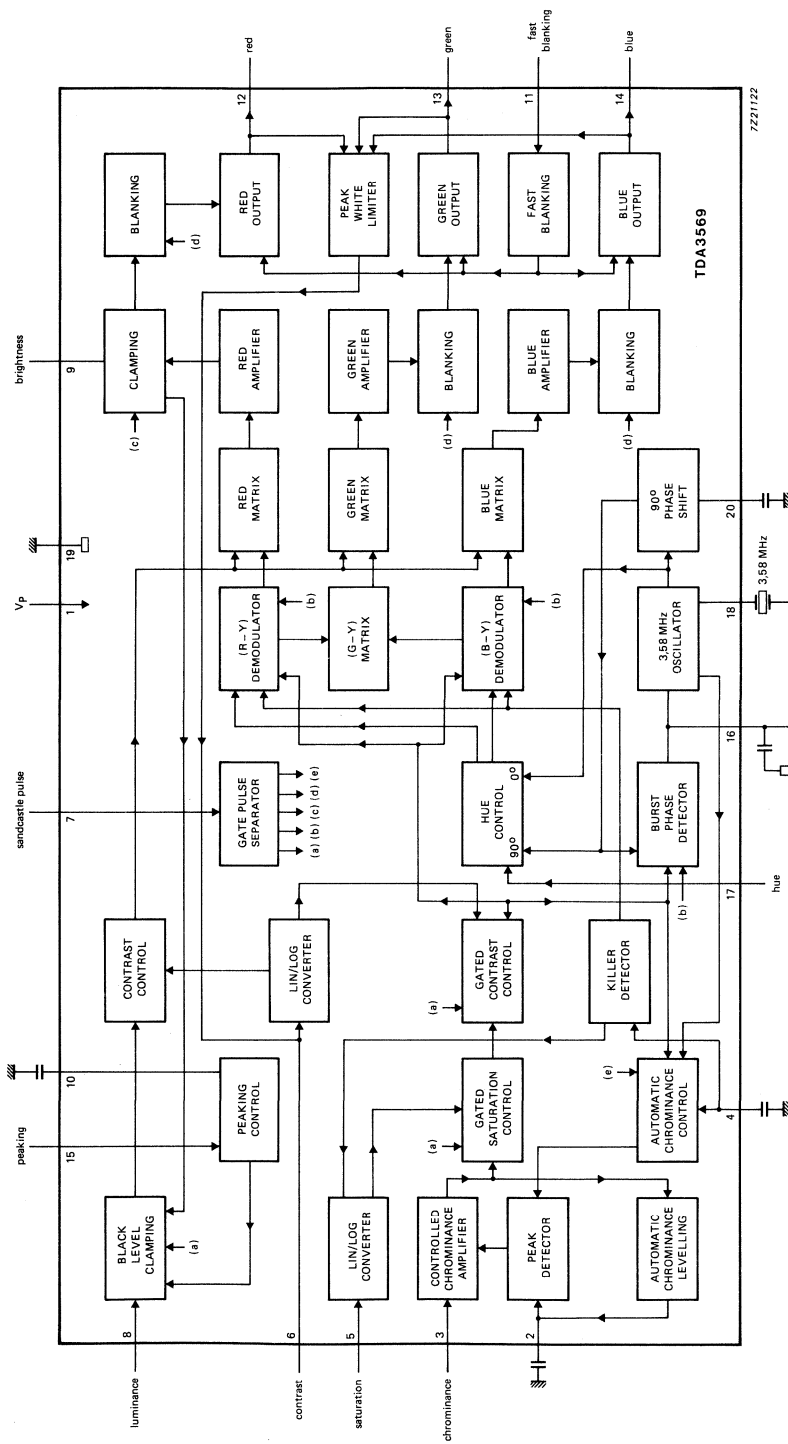


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

Luminance amplifier

The luminance amplifier is voltage driven and requires a positive video input signal of 450 mV peak-to-peak, a.c. coupled to pin 8. The coupling capacitor provides storage for the black level clamping circuit. After clamping the signal is fed to a peaking circuit in which the amount of overshoot is controlled from the voltage on pin 15.

Then next stage controls luminance signal contrast. Adjusted by the voltage on pin 6, the contrast control range is nominally −17 to +3 dB. The curve is linear as shown in Fig. 2.

Chrominance amplifier

The chrominance amplifier has an asymmetrical input and requires a.c. coupling to pin 3. The minimum peak-to-peak signal amplitude at the input is 55 mV (colour bar signal with 75% saturation; burst signal is 25 mV (peak-to-peak)). The gain control has a range greater than 30 dB but to avoid clipping, the input signal should not exceed 1,1 V (peak-to-peak).

After gain control, the chrominance signal is fed to an automatic chrominance levelling (ACL) circuit which avoids over-saturation when the incoming chrominance/burst ratio exceeds 2,2 : 1. The ACL circuit controls the chrominance amplitude via the automatic chrominance control (ACC) circuit.

The controlled chrominance signal is then fed to the saturation and contrast control stages. The chrominance and luminance contrast stages are directly coupled to ensure good tracking. Saturation is controlled via pin 5. This has a high impedance and a control range of 2 to 4 V, giving a linear saturation control greater than 50 dB. The burst signal is not affected by contrast or saturation controls.

After the amplification and control stages the chrominance signal is fed to the (R-Y) and (B-Y) demodulators, the burst phase detector and the ACC detector.

Oscillator and ACC circuit

The 3,58 MHz reference oscillator operates at the subcarrier frequency. The crystal is connected between pin 18 and ground. The oscillator does not require adjustment due to the small spreads of the IC. To check the free running frequency of the oscillator the loop is opened by connecting the saturation control (pin 5) to the positive supply line. The oscillator has an internal gain-limiting stage which holds the gain at unity. This ensures internal signals remain sinusoidal thus preventing higher harmonics of subcarrier signals and allowing hue control to be obtained by mixing two signals with phases of 0^{o} and 90^{o}. The 90^{o} phase shift is obtained via a Miller integrator and the bias capacitor for this is connected at pin 20.

The ACC detector compares the burst signal with the 0^{o} reference signal. After detection, the ACC signal is fed via a peak detector to control the chrominance amplifier and to a sample-and-hold circuit to drive the colour killer circuit.

The reference signal for the burst phase detector is provided by the 90^{o} phase-shifted signal. An RC network is used to obtain the required catching range and noise immunity for the output voltage of the burst phase detector.

The hue control is obtained by mixing the 0^{o} and 90^{o} oscillator signals before they are fed to the (R-Y) and (B-Y) demodulators. This means that the hue control reacts to control voltage changes without delay as it is not dependent on the PLL.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Demodulator circuits

The demodulators are driven by the amplified and controlled chrominance signals, the reference signals being from the hue control circuit. With nominal hue control, the phase angle of the (R-Y) reference signal is 0° and that for the (B-Y) reference signal is 90°.

For flesh tone correction the demodulated (R-Y) signal is matrixed with the demodulated (B-Y) signal according to the following equations:

$(R\text{-}Y)_{matrixed} = 1{,}61\ (R\text{-}Y)_{IN} - 0{,}42\ (B\text{-}Y)_{IN}$

$(G\text{-}Y)_{matrixed} = -0{,}43\ (R\text{-}Y)_{IN} - 0{,}11\ (B\text{-}Y)_{IN}$

$(B\text{-}Y)_{matrixed} = (B\text{-}Y)_{IN}$

In these equations $(R\text{-}Y)_{IN}$ and $(B\text{-}Y)_{IN}$ indicate the colour difference signal amplitudes when the chrominance signal is demodulated with a phase difference of 90° between the R-Y and B-Y demodulators and gain ratio B-Y/R-Y = 1,78 : 1.

RGB matrix and amplifier circuits

The three matrix and amplifier circuits are identical. The luminance signal and the colour difference signals are added in the matrix circuit to obtain the colour signal.

Output signals are 5 V (peak-to-peak) (black-white) for the following nominal input signals and control settings.

- Luminance 450 mV (peak-to-peak)
- Chrominance 550 mV (peak-to-peak) (burst/chrominance ratio of the input = 1 : 2,2)
- Contrast −3 dB (maximum)
- Saturation −10 dB (maximum)

The maximum available output voltage is approximately 7 V (peak-to-peak).

The black level of the red channel is compared with a variable external reference level (pin 9) which provides the brightness control. The control loop is closed via the luminance input.

The luminance input is varied to control the black level, therefore the green and blue outputs follow any variation of the red output. The output of the black level control can be varied between 2 V and 4 V. The corresponding brightness control voltage is shown in Fig. 4.

If the output signal approaches the level of 9 V the peak-white limiter circuit becomes active and reduces the output signal via the contrast control.

Blanking of RGB signals

A slicing level of about 1,5 V is used for this blanking function, so that the wide part of the sandcastle pulse is separated from the rest of the pulse. During blanking a level of + 2 V is available at the output.

The circuit also has a fast blanking input (pin 11) which blanks the RGB outputs within 50 ns.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 1)		$V_P = V_{1-19}$	–	13,2	V
Total power dissipation		P_{tot}	–	1,7	W
Storage temperature range		T_{stg}	−25	+150	°C
Operating ambient temperature range		T_{amb}	−25	+65	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 50 K/W

CHARACTERISTICS

$V_P = V_{1-19} = 12$ V; $T_{amb} = 25$ °C; all voltages refer to pin 19; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage (pin 1)		$V_P = V_1$	10,8	12	13,2	V
Supply current		I_1	–	80	–	mA
Total power dissipation		P_{tot}	–	0.96	–	W
Luminance input signal						
Input voltage (pin 8) (peak-to-peak value)	note 1	$V_{8(p\text{-}p)}$	–	450	–	mV
Input voltage level before clipping occurs in the input stage		V_8	–	–	1	V
Input current (pin 8)		I_8	–	0,15	1,0	μA
Contrast control range	see Fig. 2		–	−17 to +3	–	dB
Contrast control input current (pin 6)	$V_6 < 6$ V	I_6	–	0,5	15	μA
	peak white limiter active, $V_6 = 2{,}5$ V	I_6	–	7	–	mA
Input resistance (pin 6)	$V_6 > 6$ V	R_6	1,4	2,0	2,6	kΩ

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Peaking of luminance signal						
Input impedance (pin 15)		$\|Z_{10}\|$	–	10	–	kΩ
Output impedance (pin 10)		$\|Z_{15}\|$	–	75	–	Ω
Ratio of internal/ external current	pin 10 AC short-circuit to ground		–	10	–	
Chrominance amplifier						
Input signal amplitude (peak-to-peak value) (pin 3)	note 2	$V_{3(p-p)}$	–	550	–	mV
Input signal amplitude before clipping occurs in the input stage (peak-to-peak value)		$V_{3(p-p)}$	–	–	1,1	V
Minimum burst signal amplitude within the ACC control range (peak-to-peak value)			35	–	–	mV
ACC control range			30	–	–	dB
Change of the colour signal at the output for the complete control range		ΔV	–	–	+ 2	dB
Input impedance (pin 3)		$\|Z_3\|$	6	8	10	kΩ
Input capacitance (pin 3)		C_3	–	4	6	pF
Saturation control range	see Fig. 3		50	–	–	dB
Saturation control input current (pin 5)	$V_5 < 6$ V	I_5	–	1	20	μA
Input impedance (pin 5)	$V_5 = 6$ to 10 V	$\|Z_5\|$	1,5	2,1	2,7	kΩ
	colour killer active	$\|Z_5\|$	1,5	2,1	2,7	kΩ
	$V_5 > 10$ V	$\|Z_5\|$	0,7	1,0	1,5	kΩ
Tracking between luminance and chrominance contrast	for 10 dB of control		–	1	2	dB

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
ACL circuit						
Chrominance/burst ratio at which ACL commences	note 3		–	2,2	–	
Reference part						
Phase-locked loop						
Catching range		Δf	± 400	± 500	–	Hz
Phase shift for 400 Hz carrier frequency deviation		$\Delta\phi$	–	–	5	deg
Oscillator						
Temperature coefficient of oscillator frequency		TC_{osc}	–	1,5	2,5	Hz/K
Frequency deviation	ΔV_P = ± 10%	Δf_{osc}	–	150	250	Hz
Input resistance (pin 18)		R_{18}	260	360	460	Ω
Input capacitance (pin 18)		C_{18}	–	–	10	pF
ACC generation						
Voltage at pin 4 with nominal input signal		V_4	–	5,8	–	V
Voltage at pin 4 without burst input		V_4	–	2	–	V
Colour-off voltage (pin 4)		V_4	–	3,1	–	V
Δ colour-off-colour-on		ΔV_4	100	300	500	mV
Voltage at pin 2 with nominal input signal		V_2	5,2	5,8	6,4	V
Hue control						
Control voltage range	see Fig. 5					
Input current (pin 17)	$V_{17} < 5$ V	I_{17}	–	0,5	20	μA
Input impedance (pin 17)	$V_{15} > 5$ V	$\lvert Z_{17}\rvert$	1,5	2,5	3,5	kΩ
Demodulation part						
Demodulation signal ratios	note 4					
(R-Y)/(B-Y)	no (R-Y)	V_{12}/V_{14}	–	–0,42	–	
(R-Y)/(B-Y)	colour bar	V_{12}/V_{14}	–	1,4	–	
(G-Y)/(R-Y)	no (B-Y)	V_{13}/V_{14}	–	–0,25	–	
(G-Y)/(B-Y)	no (R-Y)	V_{13}/V_{14}	–	–0,11	–	
Frequency response	0 to 0,7 MHz		–	–	–3	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
RGB matrix and amplifiers						
Output signal amplitude (peak-to-peak value) (pins 12, 13 and 14)	with nominal luminance input and nominal contrast; note 5; black-white	$V_{12,13,14(p-p)}$	4,0	5,0	6,0	V
Output signal amplitude of the "blue" channel; (B-Y) signal (pin 14) (peak-to-peak value)	with nominal contrast and saturation; no luminance input	$V_{14(p-p)}$	–	3,8	–	V
Maximum peak-white level (pins 12, 13 and 14)	note 6	$V_{12,13,14}$	9,0	9,3	9,6	V
Available output current (pins 12, 13 and 14)	per pin	$I_{12,13,14}$	10	–	–	mA
Difference in black level between the three channels			–	–	600	mV
Black level shift with vision content			–	10	40	mV
Brightness control voltage range	see Fig. 4					
Brightness control input current (pin 9)		$-I_9$	–	–	50	μA
Black level variation with temperature		$\Delta V/\Delta T$	–	0,15	1,0	mV/K
Black level variation with contrast control		ΔV	–	75	200	mV
Relative spread between the three output signals			–	–	10	%
Relative variation in black level between the three channels	during variations of contrast (10 dB), brightness (± 1 V), and supply voltage (± 10%)	ΔV	–	0	20	mV
Differential drift of black level over a temperature range of 40 °C		ΔV	–	0	20	mV
Blanking level at the RGB outputs		V_{bl}	1,95	2,15	2,35	V

parameter	conditions	symbol	min.	typ.	max.	unit
Tracking of output black levels with supply voltage		$\frac{\Delta V_{bl}}{V_{bl}} \times \frac{V_P}{\Delta V_P}$	1,0	1,05	1,1	
Signal-to-noise ratio of output signals	note 7	S/N	62	–	–	dB
Residual 3,58 MHz in RGB outputs (peak-to-peak value)		$V_{R(p-p)}$	–	50	75	mV
Residual 7,1 MHz and higher harmonics in the RGB outputs (peak-to-peak value)		$V_{R(p-p)}$	–	50	75	mV
RGB output impedances		$\lvert Z_{10,11,12} \rvert$	–	–	50	Ω
Frequency response of total luminance and RGB amplifier circuits	0 to 5 MHz		–	–	–3	dB
Sandcastle input						
Level at which RGB blanking is activated		V_7	1,0	1,5	2,0	V
Level at which burst gate clamping pulses are separated		V_7	6,5	7,0	7,5	V
Delay between black level clamping and burst gating pulse		t_d	300	375	450	ns
Input current (pin 7)	V_7 = 0 to 1 V	I_7	–	–	–1	mA
	V_7 = 1 to 8,5 V	I_7	–	–20	–40	μA
	V_7 = 8,5 to 12 V	I_7	–	–	2	mA
Fast blanking						
Level at which fast blanking is activated		V_{11}	–	2	–	V
Allowable voltage at blanking input		V_{11}			5	V
Delay between fast blanking input and output		t_d			50	ns

DEVELOPMENT DATA

Notes to the characteristics

1. Signal with negative going sync; amplitude includes sync pulse amplitude.
2. Signal amplitude indicated is for colour bar with 75% saturation, thus the chrominance/burst ratio is 2,2 : 1.
3. The ACL circuit limits the chrominance signal to a particular value as soon as the chrominance/burst ratio exceeds 2,2 : 1. Limiting is performed via the ACC function.
4. These matrixed values are found by measuring the ratio of the various output signals. The values are derived from the matrix equations given in the 'FUNCTIONAL DESCRIPTION'.
5. Nominal contrast is specified as maximum contrast −3 dB; nominal satuarion is specified as maximum saturation −10 dB.
6. When this level is exceeded, the amplitude of the output signal is reduced with a discharge of the capacitor on pin 7 (contrast control), the discharge current is 7 mA.
7. The signal-to-noise ratio is specified as peak-to-peak signal amplitude with respect to the r.m.s. value of noise.

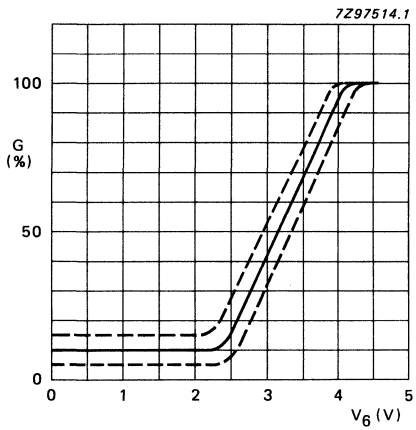


Fig. 2 Contrast control voltage range.

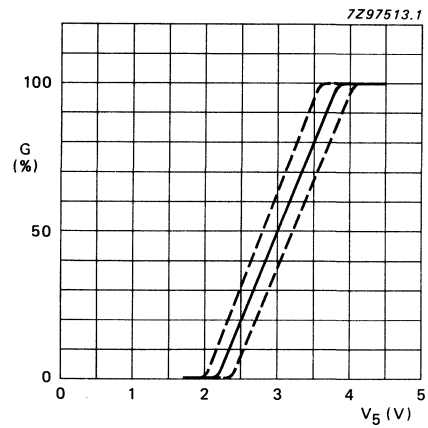


Fig. 3 Saturation control voltage range.

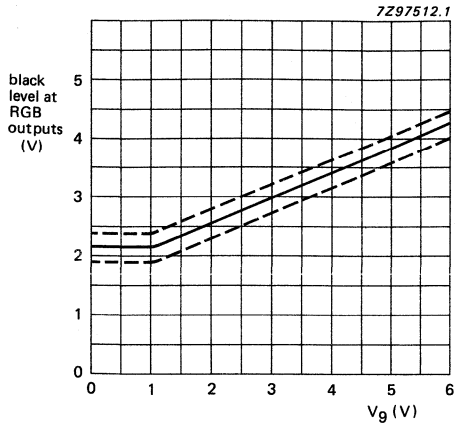


Fig. 4 Brightness control voltage range.

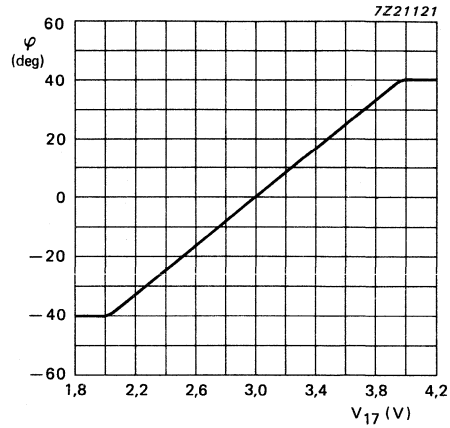


Fig. 5 Hue control voltage range.

DEVELOPMENT DATA

APPLICATION INFORMATION

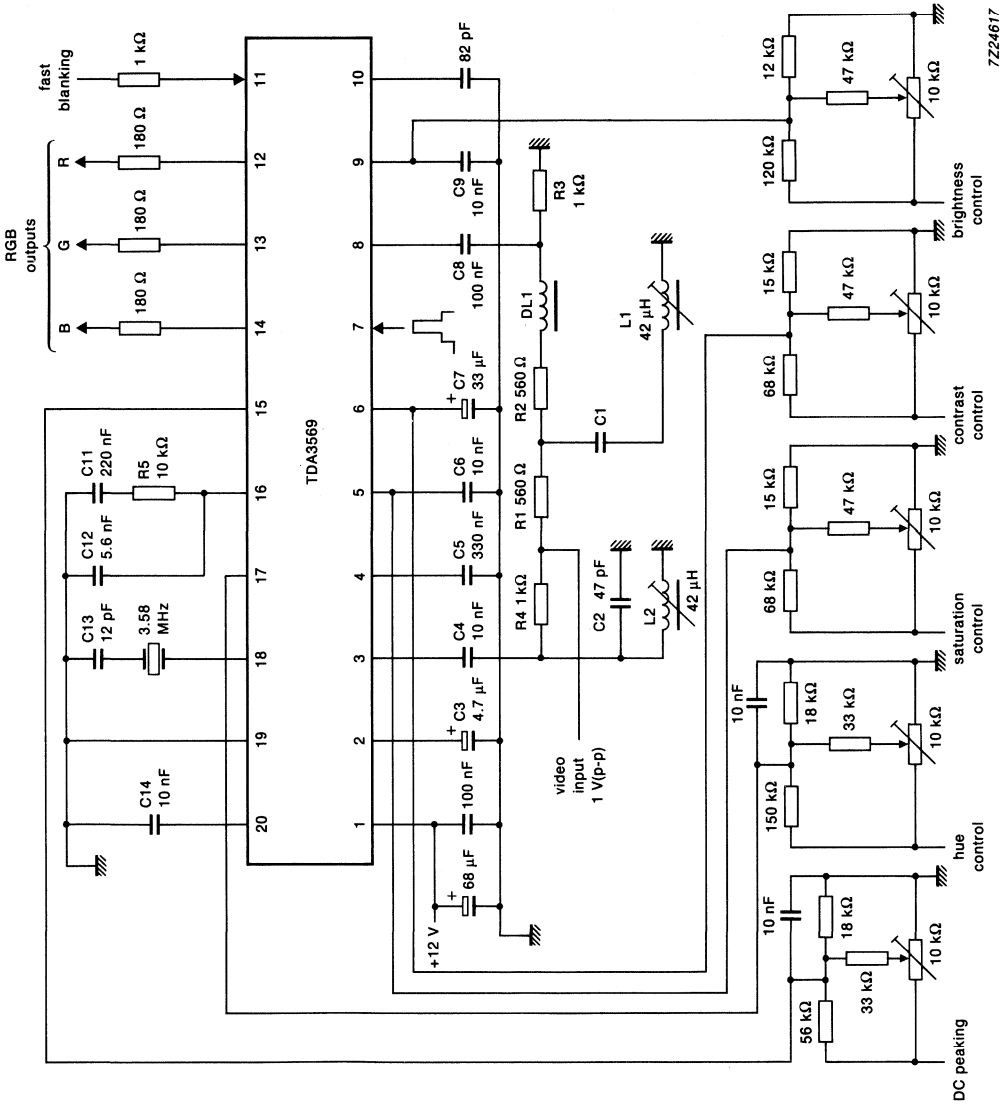


Fig. 6 Application diagram.

SECAM PROCESSOR CIRCUIT

GENERAL DESCRIPTION

The TDA3590A processor circuit converts SECAM signals into sequential phase-modulated (quasi-PAL) signals. It combines all the functions of the TDA3590, TDA3591 and TDA3591A to provide a complete SECAM processor system. The circuit is intended for use in conjunction with TDA3560, TDA3561, TDA3561A, TDA3562A or TDA3566 to provide SECAM/PAL/NTSC/black-and-white processor combinations.

Features

- Limiter/amplifier for chrominance signal
- SECAM demodulator
- Clamp circuits and de-emphasis for colour difference signals
- Modulator to convert colour difference signals into sequential, phase-modulated signals
- Identification circuit for horizontal, vertical or combined horizontal and vertical SECAM identification
- Divider circuit to provide 4,4 MHz carrier from 8,8 MHz signals generated in TDA3560/61/61A/62A/66
- Sandcastle pulse detector
- SECAM switch and PAL matrix
- Video amplifier
- Pin compatibility with TDA3590, TDA3591 and TDA3591A when application requires SECAM ident priority (does not apply with PAL ident priority)

QUICK REFERENCE DATA

Supply voltage	$V_P = V_{17-2}$	typ.	12 V
Supply current	$I_P = I_{17}$	typ.	100 mA
Chrominance amplifier and demodulator			
Input signal PAL (peak-to-peak value)	$V_{4-2(p-p)}$	typ.	550 mV
Input signal SECAM (peak-to-peak value)	$V_{4-2(p-p)}$	typ.	100 mV
Output signal PAL (peak-to-peak value) at $V_{16(p-p)} = 1{,}2$ V	$V_{8-2(p-p)}$	typ.	900 mV
Output signal SECAM (peak-to-peak value)	$V_{8-2(p-p)}$	typ.	500 mV
Identification			
Input voltage range for horizontal identification (pin 5)	V_{5-2}		0 to 8 V
Input voltage range for vertical identification (pin 5)	V_{5-2}		10,5 to 12,0 V
Voltage at pin 6 for PAL	V_{6-2}	typ.	10,2 V
Voltage at pin 6 for SECAM	V_{6-2}	typ.	7,0 V
Sandcastle pulse detector			
Vertical blanking level	V_{19-2}	typ.	1,5 V
Horizontal blanking level	V_{19-2}	typ.	3,5 V
Burst gating level	V_{19-2}	typ.	7,2 V
Luminance amplifier			
Luminance input signal (peak-to-peak value)	$V_{16-2(p-p)}$	typ.	1,2 V
Luminance output signal (peak-to-peak value)	$V_{15-2(p-p)}$	typ.	3,0 V
PAL matrix and SECAM switch			
Burst signal amplitude (peak-to-peak value)	$V_{11;\,12-2(p-p)}$	typ.	60 mV
Amplification for PAL		typ.	0,5 dB
Amplification for SECAM		typ.	6 dB

PACKAGE OUTLINE

24-lead DIL; plastic (with internal heat spreader) (SOT101B).

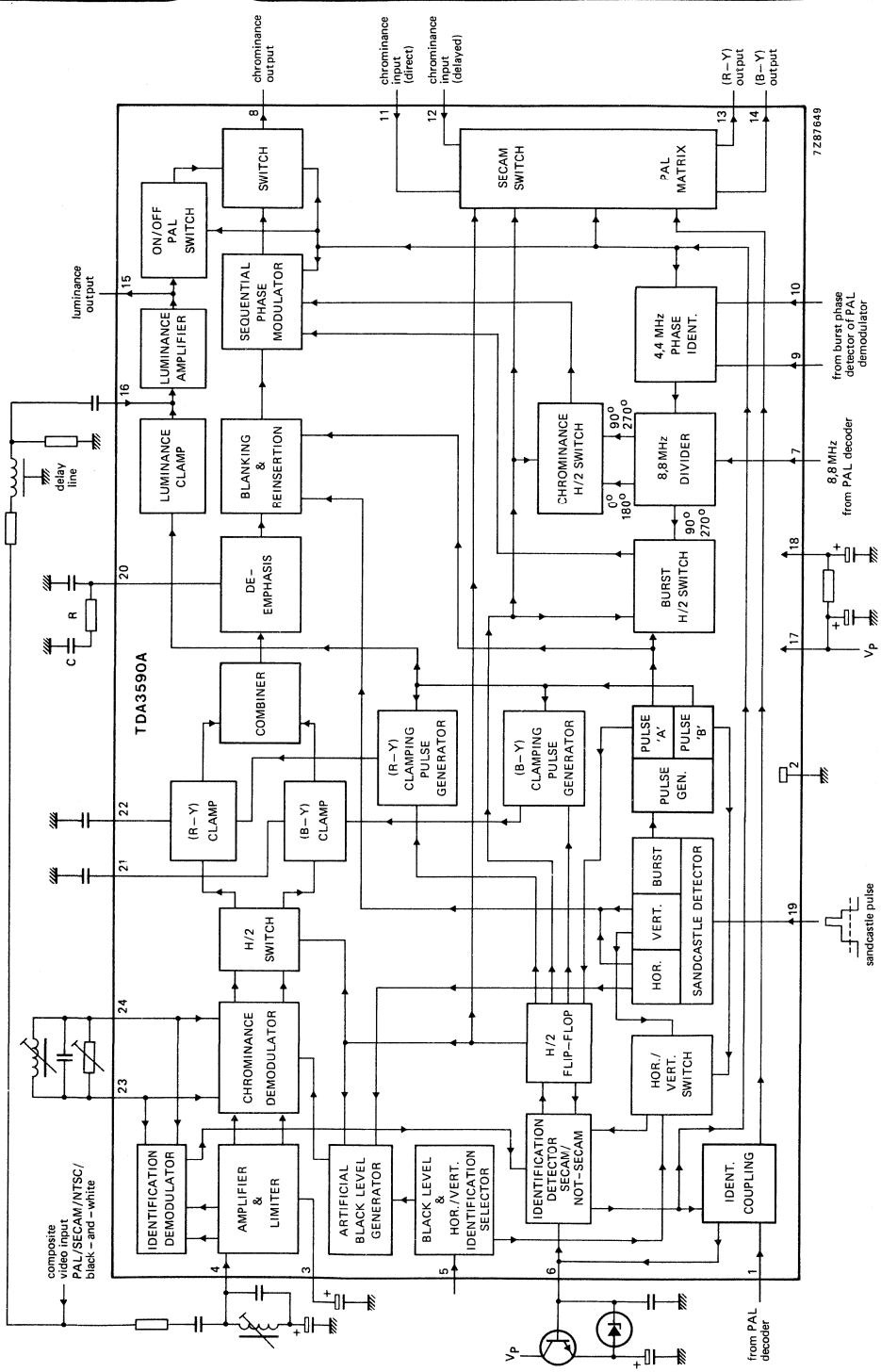


Fig. 1 Block diagram.

PINNING

1. Identification coupling input for PAL/not-PAL identification using half the saturation voltage of the PAL decoder.
2. Ground.
3. Limiter feedback.
4. SECAM video input.
5. Identification selection input using a d.c. level to preset the identification mode of horizontal/vertical detection + black level clamping/insertion.
6. Storage circuit input to SECAM/not-SECAM identification detector.
7. Divider circuit input of 8,8 MHz from the PAL decoder.
8. Chrominance signal output comprising PAL or processed SECAM (quasi-PAL).
9. Carrier signal phase identification input from the burst phase detector of the PAL decoder.
10. As for pin 9.
11. Direct chrominance input to SECAM switch/PAL matrix.
12. Delayed chrominance input to SECAM switch/PAL matrix.
13. Colour difference output (R-Y).
14. Colour difference output (B-Y).
15. Luminance output.
16. Luminance/PAL input.
17. Positive supply voltage (V_P).
18. Decoupled positive supply voltage.
19. Three-level sandcastle pulse input.
20. De-emphasis circuit connection.
21. Storage capacitor connection for (B-Y) clamp.
22. Storage capacitor connection for (R-Y) clamp.
23. Connection for reference tuned circuit for SECAM chrominance and identification demodulators.
24. As for pin 23.

FUNCTIONAL DESCRIPTION

Demodulation

The chrominance and identification demodulators of the TDA3590A both share the same reference tuned circuit (pins 23 and 24). The identification circuit automatically detects whether the incoming signal is SECAM or not-SECAM.

When the incoming signals are not-SECAM (PAL/NTSC/black-and-white) they are diverted via pin 16 to the chrominance output at pin 8 and no signal demodulation takes place. The delay line connected to pin 16 delays the signals to equalize the delay of the SECAM processor circuitry. When SECAM signals are received the PAL signal path is switched off.

Incoming SECAM signals are applied to pin 4 via an external bell filter. The signals are amplified, limited and then demodulated. The limiters give optimum i.f. interference suppression. Only one demodulator is necessary as the colour difference signals are available sequentially. After demodulation the colour difference signals are separated by an H/2 switch and then applied to (R-Y) and (B-Y) clamp circuits where the black levels are clamped to the same d.c. level. The optimum black level can be obtained at the end of the horizontal burst, so the timing of the (R-Y) and (B-Y) clamp is determined by the last 1,45 μs of the burst gate pulse.

The two colour difference signals are combined again after clamping and then applied to the modulator via de-emphasis, blanking and reinsertion circuits.

The ratio of (R-Y) to (B-Y) at the de-emphasis output (pin 20) is 1,78. The external de-emphasis components of R = 1 kΩ and C = 470 pF give a spread at the internal de-emphasis network $< 20\%$.

FUNCTIONAL DESCRIPTION (continued)

If artificial black level reinsertion is required the burst gating pulse (Fig. 2) is used to time black level clamping. Artificial black levels are inserted during the horizontal blanking period when $V_{5\text{-}2} > 2$ V. The clamp circuits then react to the artificial levels instead of the demodulated burst signals (this is necessary when no horizontal burst signals are available). The inserted signals may not be identical to the demodulated signals because of circuitry spread but this can be corrected by detuning the demodulator reference tuned circuit.

Modulation

A burst signal is reinserted into the combined SECAM signal at the input to the sequential phase modulator. The nominal duration of this burst is 2,85 μs which approximates to the duration of the PAL burst and, in combination with the horizontal blanking pulse (used as keying pulse in the SECAM switch), minimizes interference in the a.c.c. loop of the TDA3560/61/62.

At the input to the modulator the (R-Y) and (B-Y) signals have a positive phase position for magenta colour. The modulation carriers for the (R-Y) and (B-Y) signals are 90° out of phase; the burst is modulated in the + (R-Y) direction and is only present during an (R-Y) line, the modulated (R-Y) component has the same phase position as the (R-Y) burst for magenta colour.

The chrominance output from pin 8, in the SECAM mode, is a quasi-PAL signal with alternate line, sequential modulation. Odd and even harmonics of the 4,4 MHz carrier introduced by the modulator are suppressed by internal filters. A correction is made to the burst-chrominance ratio of the quasi-PAL signals for equal saturation of PAL and SECAM signals.

Identification

Identification of the SECAM signal is performed using the fact that only SECAM has a line-to-line difference in demodulated voltage level. This is detected during the last 1,5 μs of the burst gate pulse. A flip-flop, which is switched by the leading edge of the sandcastle time blanking pulse, provides the reference input to the identification detector. Here the phase of the flip-flop is compared with that of the changing voltage levels from the demodulator. The SECAM identification circuits operate when selected by the voltage on pin 5; this may be horizontal, vertical or combined horizontal and vertical identification, depending on the switching arrangements of pin 5. An internal voltage divider presets pin 5 to 6 V to give automatic selection of horizontal identification plus black level re-insertion. Vertical identification is selected by taking the voltage on pin 5 above 10,5 V, then the system compares the demodulator output voltage only during line scanning of the vertical blanking.

Information obtained from the identification detector is also used for colour killing and, if required, for switching to PAL.

Luminance amplification

The luminance amplifier input at pin 16 can be up to 1,2 V (peak-to-peak value) which equates to a peak-to-peak voltage of 2,7 V −7 dB. The amplifier gain is typically 8 dB. The luminance clamping circuit is activated during the SECAM identification timing (see Fig. 2).

Sandcastle pulse detection

The sandcastle pulse detector requires a three-level sandcastle pulse to provide horizontal blanking, vertical blanking and burst gate pulses. The detected burst gate pulse triggers a pulse generator which produces two timing pulses, pulse 'A' and pulse 'B' (see Fig. 2). Pulse 'A' is used to time the PAL burst modulator. Pulse 'B' provides the timing of the (R-Y) clamp (present only during a red line); the (B-Y) clamp (present only during a blue line); the luminance clamp (present every line); and the SECAM horizontal identification circuit.

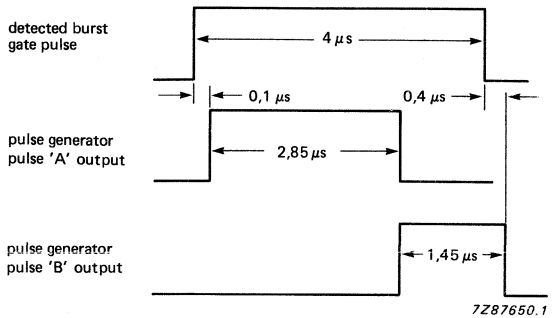


Fig. 2 Burst gate timing pulse generation.

PAL matrix and SECAM switch

The PAL matrix and SECAM switch is included in the TDA3590A to facilitate handling of the two chrominance signal types, PAL and SECAM. For PAL, the direct chrominance signal and the chrominance signal delayed by the PAL delay line are used by the PAL matrix to separate the two colour difference signals. Phase accuracy is not critical for this operation as the colour difference signals are not mixed. For SECAM, the quasi-PAL sequential colour difference signals are separated by switching. The gain of the switching circuit is two times that for normal PAL reception to maintain signal balance between the two systems. The (B-Y) output from the SECAM switch is a signal with no burst; the (R-Y) output has a burst modulated in the + (R-Y) direction during the + (R-Y) line. There is minimal crosstalk between the colour difference signals in the SECAM switch.

Carrier generation

The carrier for the sequential phase modulator is obtained using the 8,8 MHz input from the PAL decoder. This input is divided by two to provide two 4,4 MHz signals with a phase relationship of 90°. Correct phasing between the 4,4 MHz and the PAL decoder is ensured by the 4,4 MHz phase identifier circuit which resets the divider if the phasing is wrong (see Figs 3 and 4 for inter-connections). The inputs/outputs to the phase identifier have internal current sources in the case of SECAM.

Coupling of identification systems

Coupling of system identification between TDA3590A and a PAL decoder is performed using the functions of pins 1 and 6. The voltage level at pin 1 is controlled by the PAL/not-PAL detection of the PAL decoder; the voltage level at pin 6 is a function of SECAM/not-SECAM detection of the TDA3590A modified by the action of pin 6 external circuit.

The circuit action is as follows and is summarized in Table 1.

Channel switching — During channel switching pin 6 is taken rapidly to a high voltage (± 10,2 V) by the external circuit. This corresponds to the not-SECAM mode of the TDA3590A.

PAL — The high voltage level at pin 6 caused by channel switching is maintained by the TDA3590A when it recognizes the signal as not-SECAM. An internal current source keeps pin 6 voltage high, locking the TDA3590A in the not-SECAM mode. This condition is maintained even if reflected PAL signals are present. The PAL decoder recognizes the signal as PAL and takes pin 1 of TDA3590A to a voltage of between 0,5 and 2,6 V, depending on the setting of the saturation voltage. The system is thus locked in the PAL mode.

FUNCTIONAL DESCRIPTION (continued)

SECAM

The initial high voltage level (± 10,2 V) at pin 6 caused by channel switching sets the TDA3590A in the not-SECAM mode and during this time the PAL decoder detects a not-PAL signal. This causes a voltage at pin 1 of $< 0,4$ V which prevents the internal current source of TDA3590A maintaining the high voltage level of pin 6 which, in turn, allows the TDA3590A to detect SECAM. The initiation of SECAM detection is delayed by the action of pin 6 external circuit and commences when pin 6 approaches 9,1 V. The SECAM signals are converted by TDA3590A to quasi-PAL signals at pin 8 which are detected by the PAL decoder as PAL signals. The resulting modes of operation are SECAM for the TDA3590A and PAL for the PAL decoder, together giving a system operation in the SECAM mode.

Black-and-white

The TDA3590A is initially set in the not-SECAM mode as previously described. The PAL decoder detects not-PAL and the TDA3590A detects not-SECAM which results in a system operation in the colour-killing mode.

Table 1 System operating modes

TDA3590A mode	PAL decoder mode	system operating mode
SECAM	PAL	SECAM
SECAM	not-PAL	condition not used
not-SECAM	PAL	PAL
not-SECAM	not-PAL	black-and-white

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 17)	$V_P = V_{17-2}$	max.	13,2 V
Total power dissipation	P_{tot}	max.	1,88 W
Operating ambient temperature range	T_{amb}		−25 to + 65 °C
Storage temperature range	T_{stg}		−25 to + 150 °C

CHARACTERISTICS

$V_P = V_{17-2} = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified. The parameter values are valid only when the reference tuned circuit has been aligned as detailed in note 1.

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage range (pin 17)	V_{17-2}	10,8	12,0	13,2	V
Supply current (pin 17)	I_{17}	–	100	–	mA
Input current (pin 18)	I_{18}	–	–	170	μA
Total power dissipation	P_{tot}	–	1,2	–	W
Chrominance amplifier and demodulator					
Input signal PAL (peak-to-peak value)	$V_{4-2(p-p)}$	–	–	1,1	V
Input signal SECAM (peak-to-peak value)	$V_{4-2(p-p)}$	15	100	300	mV
Input resistance (pin 4)	R_{4-2}	–	10	–	kΩ
Input capacitance (pin 4)	C_{4-2}	–	–	5	pF
(R-Y)/(B-Y) ratio before modulation (pin 20)		–	1,78	–	
Relative black level deviation of colour difference signals before modulation (note 2)					
Output signal PAL (peak-to-peak value) at $V_{16(p-p)} = 1,2$ V	$V_{8-2(p-p)}$	–	900	–	mV
Output signal SECAM (peak-to-peak value)	$V_{8-2(p-p)}$	–	500	–	mV
Output impedance	$\lvert Z_{8-2} \rvert$	–	50	–	Ω
Input voltage for clamping on back porch of colour difference signals	V_{5-2}	–	–	0,5	V
Input voltage for artificial black level insertion after demodulation	V_{5-2}	2	–	–	V
Input resistance between pins 23 and 24	R_{23-24}	–	4	–	kΩ
Input capacitance between pins 23 and 24	C_{23-24}	–	15	–	pF
Linearity of (B-Y) signal (pin 8) (note 3)		85	92	–	%
Linearity of (R-Y) signal (pin 8) (note 4)		93	100	–	%
Input resistance (pin 5)	R_{5-2}	–	10	–	kΩ
Chrominance demodulator zero point stability (pin 20) (note 5)	f_0	–	5	–	kHz
Offset (B-Y) black level (pin 8) at f_0 clamping; $f_{offset} = 4,4$ MHz		–	−15	–	kHz
Offset (R-Y) black level (pin 8) at f_0 clamping; $f_{offset} = 4,4$ MHz		–	−25	–	kHz

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Identification SECAM/not-SECAM					
Input voltage range for horizontal identification (pin 5)	V_{5-2}	0	–	8	V
Input voltage range for vertical identification (pin 5)	V_{5-2}	10,5	–	V_P	V
Voltage at pin 6 for PAL	V_{6-2}	–	10,2	–	V
Voltage at pin 6 for SECAM	V_{6-2}	–	7,0	–	V
Identification ON for SECAM	V_{6-2}	–	10,6	–	V
Colour OFF for SECAM	V_{6-2}	–	9,7	–	V
Colour ON for SECAM	V_{6-2}	–	9,0	–	V
Voltage at pins 9 and 10 for SECAM	$V_{9-2;\ 10-12}$	–	10,5	–	V
Voltage between pins 9 and 10 for SECAM	V_{9-10}	–	–	3	mV
Permissible voltage range at pins 9 and 10 for PAL	$V_{9-2;\ 10-2}$	6,8	–	10,2	V
Sandcastle pulse detector and clamping pulse generator					
Voltage level at which the vertical blanking pulse is separated	V_{19-2}	1,0	1,5	2,0	V
required pulse amplitude (peak-to-peak value)	$V_{19-2(p-p)}$	2,1	–	2,9	V
Voltage level at which the horizontal blanking pulse is separated	V_{19-2}	3,0	3,5	4,0	V
required pulse amplitude (peak-to-peak value)	$V_{19-2(p-p)}$	4,1	–	6,6	V
Voltage level at which the burst gating pulse is separated	V_{19-2}	6,7	7,2	7,7	V
required pulse amplitude (peak-to-peak value)	$V_{19-2(p-p)}$	7,8	–	V_P	V
Input current at $V_{19-2} = 7$ V	I_{19}	–	–	40	μA
Carrier generator (note 6)					
Input signal from TDA3560/61/61A/62A/66 (peak-to-peak value)	$V_{7-2(p-p)}$	150	–	–	mV
Input resistance	R_{7-2}	–	4	–	kΩ
Input capacitance	C_{7-2}	–	5	–	pF

parameter	symbol	min.	typ.	max.	unit
Luminance amplifier					
Input signal (peak-to-peak value)	$V_{16\text{-}2(p\text{-}p)}$	–	1,2	1,7	V
Chrominance input signal when no luminance information is present (peak-to-peak value)	$V_{16\text{-}2(p\text{-}p)}$	–	–	1	V
Gain (pin 16 to 15) at f_{16} = 4,4 MHz	$G_{16\text{-}15}$	–	8	–	dB
Input current (pin 16)	I_{16}	–	–	1	μA
Input resistance during clamping (pin 16)	$R_{16\text{-}2}$	–	2,9	–	kΩ
Output impedance (pin 15) at I_{15} = 2 mA	$\lvert Z_{15\text{-}2}\rvert$	–	20	–	Ω
Frequency response at −3 dB (pin 16 to 15)	f	6	–	–	MHz
Gain (pin 16 to 8) at f_{16} = 4,4 MHz; not-SECAM condition	$G_{16\text{-}8}$	–	7	–	dB
Frequency response at −3 dB (pin 16 to 8) not-SECAM condition	f	–	5	–	MHz
PAL matrix and SECAM switch					
Burst signal amplitude (peak-to-peak value)	$V_{11;\,12(p\text{-}p)}$	–	60	–	mV
Input resistance	$R_{11;\,12\text{-}2}$	–	900	–	Ω
Input capacitance	$C_{11;\,12\text{-}2}$	–	3	–	pF
Amplification for PAL	A	–	0,5	–	dB
Amplification for SECAM	A	–	6	–	dB
Difference in amplification from inputs to one output for PAL	ΔA	–	–	0,5	dB
Line-to-line phase error in (R-Y) output for zero error in (B-Y) output for PAL		–	–	3,5	deg
Output impedance	$\lvert Z_{13;\,14\text{-}2}\rvert$	–	50	–	Ω
Identification PAL/not-PAL					
Input condition for PAL (pin 1)	$V_{1\text{-}2}$	0,8	–	2,1	V
Input conditions for not-PAL (pin 1):					
lower voltage level	$V_{1\text{-}2}$	–	–	$<0,4$	V
upper voltage level	$V_{1\text{-}2}$	$>2,6$	–	V_P	V

Notes to the characteristics

1. The parameter values given in the characteristics are valid only when the following alignment procedure is performed:
   a. Supply a SECAM signal input to pin 4 at 100 mV (peak-to-peak value) without deviation during a red and blue line (SECAM black colour information).
   b. Align the reference tuned circuit so that the output signal from pin 8 to the PAL decoder is minimum during scan (PAL black colour information).
2. When an artificial black level is inserted after demodulation the resulting black level deviation depends on the adjustment of the demodulator tuned circuit. It is therefore possible to obtain a value of 0%.
3. (B-Y) linearity is defined by $V_{out(yellow)}/V_{out(blue)}$ where f_{yellow} = (typ.) 4,02 MHz; f_{blue} = (typ.) 4,48 MHz; $V_{5\text{-}2}$ = 2,0 V.
4. (R-Y) linearity is defined by $V_{out(cyan)}/V_{out(red)}$ where f_{cyan} = (typ.) 4,68 MHz; f_{red} = (typ.) 4,12 MHz; $V_{5\text{-}2}$ = 2,0 V.
5. When the input signal to the limiter (pin 4) changes from 300 to 15 mV (peak-to-peak value) the zero point of the chrominance demodulator shifts by a typical value of 5 kHz.
6. The phase delay between the oscillator output of TDA3560/61/61A/62A/66 and the input to TDA3590A pin 7 must be adjusted for minimum burst amplitude at pin 28 of the PAL decoder.

APPLICATION INFORMATION

The pin-to-pin functions of the application shown in Fig. 3 are described against the corresponding pin numbers.

Pin 4. Chrominance input

Typical input signal values (peak-to-peak) are: SECAM 100 mV; PAL 0,55 V. The input signal, which should be free from any sound modulation, is applied single-ended to pin 4 via a filter which has the bell-shaped bandpass required for SECAM signals.

Pin 5. Horizontal/vertical identification

Selection of horizontal or vertical identification depends on the external voltage applied to pin 5. When the d.c. level on pin 5 changes with time (pulse information) a combination of horizontal and vertical identification is possible.

Horizontal identification

When the voltage at pin 5 is $< 0,5$ V horizontal identification and black level clamping occur. The clamping is during the back porch of the colour difference signals. If artificial black level insertion is required the voltage at pin 5 should be between 2 and 8 V.

Vertical identification

When the voltage on pin 5 is $> 10,5$ V vertical identification occurs (identification on 9 lines in the vertical blanking period). In this mode the black level is artificially inserted after demodulation.

Pin 6. System identification

During PAL reception the typical voltage at pin 6 is 10,2 V. This causes the luminance stage to be connected internally to the chrominance output at pin 8 and also activates the PAL matrix for normal PAL signals. During SECAM reception the typical voltage at pin 6 is 7 V. This changes the internal connection of the output from the luminance stage to the sequential phase modulator and enables the SECAM switch. Noisy SECAM signals cause the voltage at pin 6 to increase, colour killing occurs at 9,8 V and colour is reinstated at 9,1 V.

Pin 7. Carrier generation

An 8,8 MHz signal from the PAL decoder is applied via pin 7 to the divider circuit in the TDA3590A. From this two 4,4 MHz signals are obtained with a phase shift of 90° with respect to each other. These signals are applied to the modulator via an H/2 switch. The delay of the 8,8 MHz input must be adjusted for minimum burst amplitude of the chrominance signal at pin 28 of the PAL decoder. With this condition the burst generated by the TDA3590A is in phase with the (R-Y) reference signal for the PAL decoder demodulator (the a.c.c. of the PAL decoder operates in the + (R-Y) direction).

Pin 8. Chrominance output

During PAL reception this output is connected internally to the luminance stage and a composite PAL video signal is present at pin 8. During SECAM reception the sequential phase modulator is connected to this output to give a quasi-PAL signal from pin 8. Typical peak-to-peak amplitudes of the signal from pin 8 are 900 mV for PAL (with peak-to-peak input at pin 16 of 1,2 V) and 500 mV for SECAM. The output signals are applied via a chrominance bandpass filter to the chrominance a.c.c. amplifier input of the PAL decoder.

Pins 9 and 10. Divider resetting

The output of the PAL decoder burst phase detector is connected to pins 9 and 10 of TDA3590A. During SECAM reception this signal carries differential a.c. current information about the phase relationship of the 4,4 MHz dividers of both ICs. The TDA3590A generates a minimum relative voltage between pins 9 and 10 at an absolute voltage level of 10,5 V. This overrules the PAL decoder oscillator control function causing the oscillator to run at 2 x 4,43 MHz.

Pins 11, 12, 13 and 14. SECAM switch and PAL matrix

The PAL matrix circuit is enabled by system identification of PAL reception. The signal inputs to the matrix are the (direct) a.c.c. composite video output from the PAL decoder via an attenuator to pin 11 and a delayed version of the same signal via a glass delay line to pin 12. Active matrixing takes place in the IC and the separated (R-Y) and (B-Y) signals are available at pins 13 and 14 respectively.

The SECAM switch circuit is selected by system identification of SECAM reception. The inputs to the SECAM switch are the sequentially modulated quasi-PAL signals, direct and delayed, to pins 11 and 12 respectively. The SECAM switch separates the (R-Y) and (B-Y) signals which are then available at pins 13 and 14 respectively.

Pins 15 and 16. Luminance signals

The maximum peak-to-peak amplitude of the input to pin 16 should be 1,7 V. The relatively high input impedance of the luminance amplifier allows a 22 nF coupling capacitor to be used. The luminance amplifier has internal input clamping and a gain of 8 dB. The output is available at pin 15.

During SECAM reception the luminance signal is delayed approximately 470 ns by an external delay line to equalize the SECAM processing delay. The luminance and chrominance outputs are then correctly timed.

During PAL reception the PAL composite video signal passes through the external delay line and, after amplification, is available at pins 15 and 8.

APPLICATION INFORMATION (continued)

Pins 17 and 18. Supply voltage (+ 12 V)

Correct operation is ensured within the supply voltage range of 10,8 to 13,2 V. The typical power dissipation of the IC at 12 V is 1,2 W.

Pins 17 and 18 are separated by an external RC filter. Pin 18 supplies all the output stages and the biasing for several current sinks in the IC. Separation of the supply voltages minimizes crosstalk between the various parts of the IC. The capacitor at pin 18 must be small ($\approx 1\ \mu F$) to avoid the possibility of internal damage to the IC by discharge current should pin 17 be short-circuited to ground.

Pin 19. Sandcastle pulse

The required three-level sandcastle pulse may be coupled directly to the sandcastle pulse detector input at pin 19. The horizontal blanking, vertical blanking and burst gate pulses are separated by the IC.

Pin 20. De-emphasis

De-emphasis is performed at this pin with a 1 kΩ resistor and a 470 pF capacitor. Additional filtering of the 8,8 MHz signal using an 82 pF coupling capacitor prevents moiré patterns appearing on the screen.

Pins 21 and 22. Clamping of (R-Y) and (B-Y) signals

Clamping of the colour difference signals is performed after they have been separated. The normal value for the clamping storage capacitors is 100 nF but this may be increased to 470 nF if required.

Pins 23 and 24. Demodulator reference tuned circuit

The SECAM signal is applied to the demodulator via a bell filter and a limiter amplifier. Only one chrominance demodulator is used because of the sequential nature of the signal. The reference signal from the tuned circuit is applied to pins 23 and 24. Tuning and damping adjustments of the reference tuned circuit should be performed at $V_{5\text{-}2} > 2$ V (SECAM video (R-Y) (B-Y) information switched off). Adjustments should be such that minimum modulator voltage appears at pin 8, then any deviations between the black levels (when clamping on the back porch and when an artificial black level is filled in) can be made minimum.

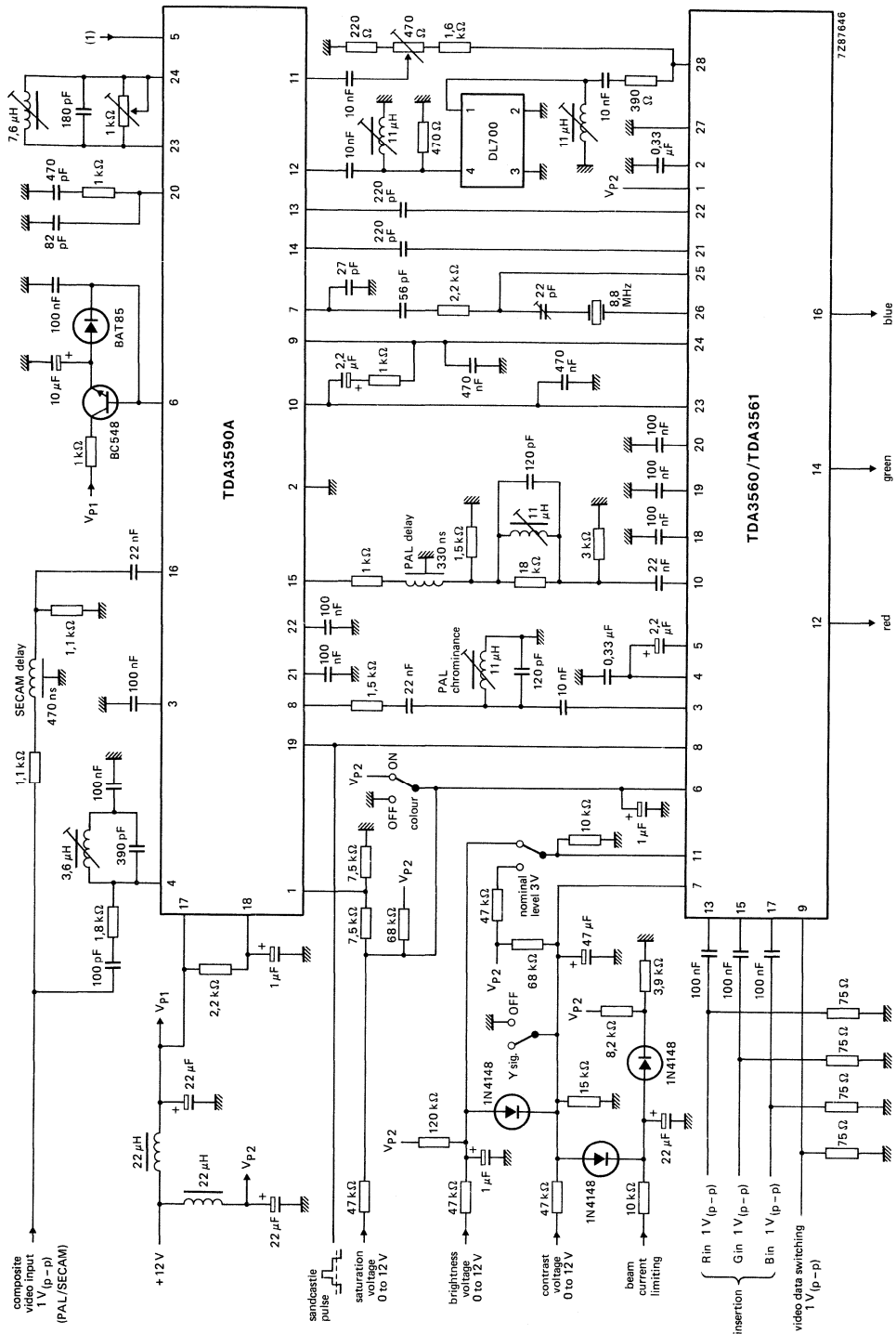


Fig. 3 PAL/SECAM decoder application.

(1) See Application Information for pin 5 — horizontal/vertical identification.

APPLICATION INFORMATION (continued)

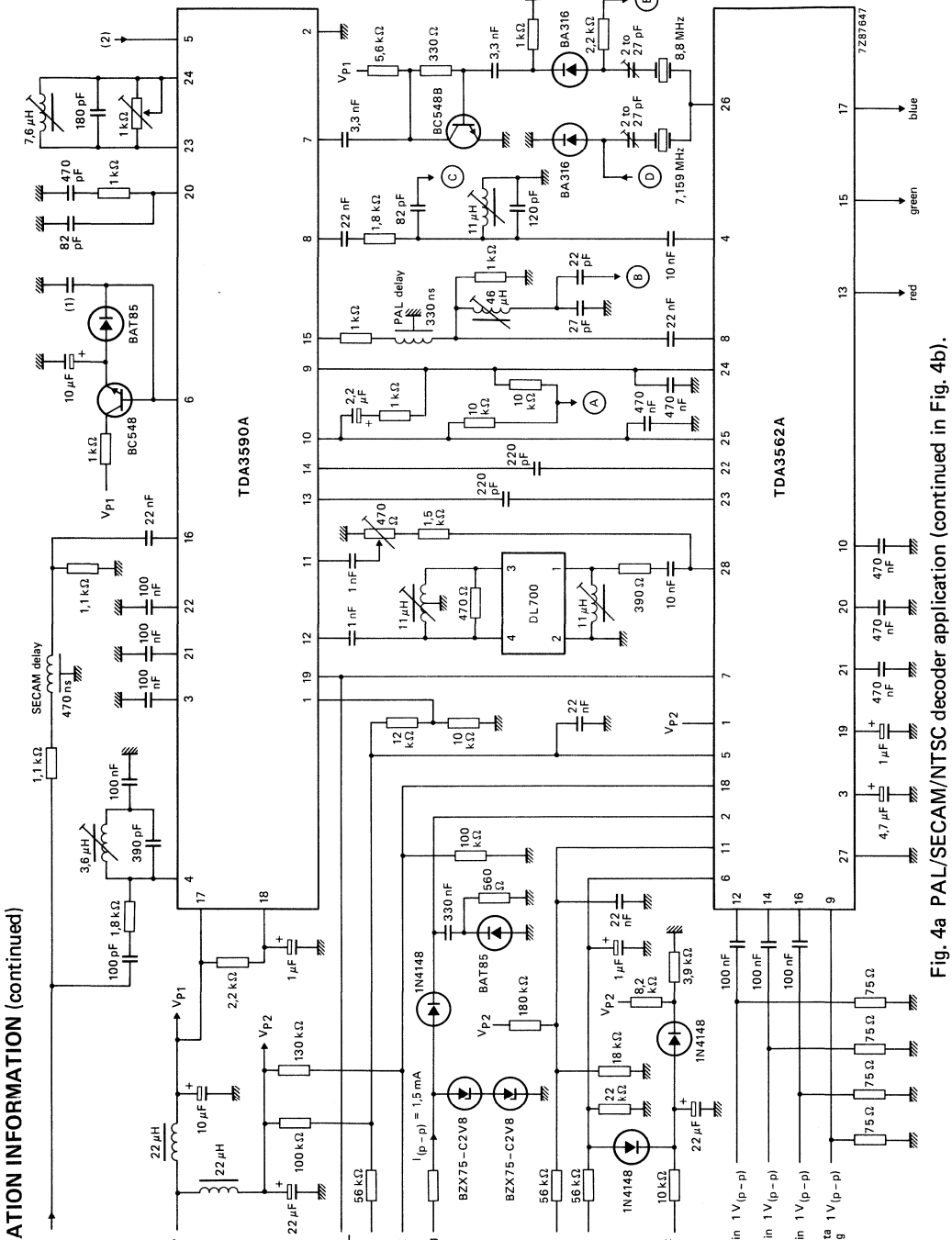
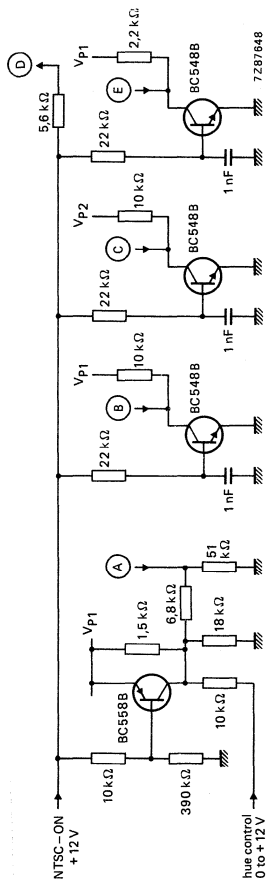


Fig. 4a PAL/SECAM/NTSC decoder application (continued in Fig. 4b).



(1) Capacitor value = 100 nF for horizontal identification or 1 μF for vertical identification.
(2) See Application Information for pin 5 — horizontal/vertical identification.

Fig. 4b PAL/SECAM/NTSC decoder application (continued from Fig. 4a).

SECAM-PAL TRANSCODER

GENERAL DESCRIPTION

The TDA3592A transcoder circuit converts SECAM input signals into true PAL signals, and can be used in combination with all types of PAL decoder.

Features

- Limiter input for chrominance signal
- SECAM demodulator
- Clamp circuits and de-emphasis for colour difference signals
- Modulator to provide true PAL signals
- 4,43 MHz oscillator
- Sandcastle pulse detector
- Identification circuit for horizontal and vertical SECAM identification
- Can be used with all types of PAL decoder
- Power-saving feature operates when supply voltage falls to (typ.) 5 V: SECAM processing shuts down but $\overline{\text{SECAM}}$ signal path remains active

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 17)		V_P	9,0	12,0	13,2	V
Supply current (pin 17)	V_P = 12 V	I_P	65	90	115	mA
Supply current (pin 17 and 18) (SECAM only)	V_P = 5 V	I_P	16	20	24	mA
Chrominance amplifier and demodulator						
Input signal $\overline{\text{SECAM}}$ (pin 3) (peak-to-peak value)		$V_{3-1(p-p)}$	–	–	1100	mV
Input signal SECAM (pin 3) (peak-to-peak value)		$V_{3-1(p-p)}$	15	100	300	mV
Output signal PAL (pin 9) (peak-to-peak value)	pin 3 = 280 kHz	$V_{9-1(p-p)}$	–	820	–	mV
Identification						
Input voltage range for horizontal identification (pin 4)		V_{4-1}	4,1	–	V_P	V
Input voltage range for vertical identification (pin 4)		V_{4-1}	0	–	2,9	V
Identification at pin 6		V_{6-1}	–	10,6	–	V
Slicing level reference voltage (pin 5)		V_{5-1}	–	7,0	–	V
Sandcastle pulse detector						
Vertical blanking level		V_{19-1}	–	1,5	–	V
Horizontal blanking level		V_{19-1}	–	3,5	–	V
Burst gating level		V_{19-1}	–	7,0	–	V
Luminance amplifier						
Luminance input signal (peak-to-peak value)		$V_{16-1(p-p)}$	–	1,2	–	V
Luminance amplifier gain at 4,4 MHz		G_{16-15}	–	7,0	–	dB

PACKAGE OUTLINE

24-lead DIL; plastic with heat spreader (SOT101B).

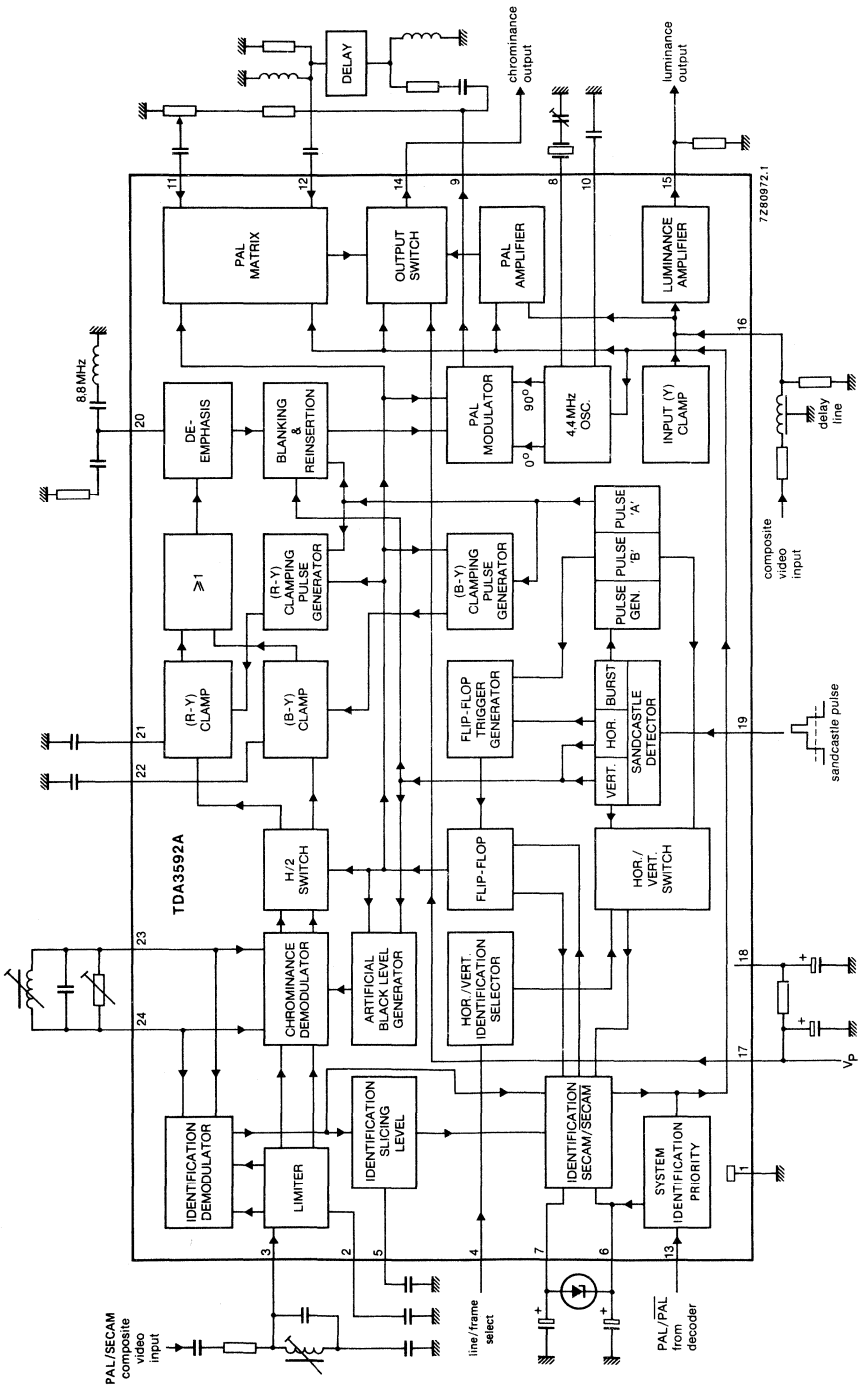


Fig. 1 Block diagram.

PINNING

1. Ground.
2. Limiter feedback.
3. Limiter input: chrominance input SECAM; identification input SECAM/$\overline{\text{SECAM}}$.
4. Identification selection input using a DC level to preset the identification mode.
   At $V_4 < 2{,}9$ V the TDA3592A is preset for frame identification.
   At $V_4 > 4{,}1$ V the TDA3592A is preset for line identification.
5. Storage capacitor input for floating level identification.
6. Storage capacitor input to SECAM/$\overline{\text{SECAM}}$ identification circuit.
7. Double time-constant input to SECAM/$\overline{\text{SECAM}}$ identification circuit.
8. 4,43 MHz oscillator.
9. Sequentially modulated output.
10. Decoupling capacitor for miller integrator feedback circuit.
11. Direct input chrominance signal.
12. Delayed input chrominance signal.
13. PAL/$\overline{\text{PAL}}$ input signal from PAL decoder.
14. Chrominance output signal.
15. Luminance output signal.
16. Luminance/$\overline{\text{SECAM}}$ input signal.
17. Positive supply voltage (V_P).
18. Decoupled positive supply voltage.
19. Three-level sandcastle pulse input.
20. De-emphasis circuit connection: R = 560 Ω; C = 1 nF.
21. Storage capacitor connection for (R-Y) clamp.
22. Storage capacitor connection for (B-Y) clamp.
23. Demodulator reference tuned circuit: nominal frequency = 4,33 MHz; nominal $Q_L = 2{,}45$.
24. As for pin 23.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Demodulation

The chrominance and identification demodulators of the TDA3592A both share the same reference tuned circuit (pins 23 and 24). The identification circuit automatically detects whether the incoming signal is SECAM or $\overline{\text{SECAM}}$ (NTSC, PAL or black-and-white).

When the incoming signals are PAL they are diverted via pin 16 to the chrominance output at pin 14 and no signal demodulation takes place. The delay line connected to pin 16 delays the signals to equalize the delay of the SECAM-PAL transcoding process. When SECAM signals are received, the PAL signal path is switched off.

Incoming SECAM signals are applied to pin 3 via an external bell filter. The signals are amplified, limited and then demodulated. Only one demodulator is necessary as the colour difference signals are available sequentially. After demodulation the colour difference signals are separated by an H/2 switch and then applied to (R-Y) and (B-Y) clamp circuits where the black levels are clamped to the same DC level. With all conditions at pin 4, artificial black levels are inserted during the horizontal blanking periods. This is done because of the possibility of horizontal burst signals not being available. The artificial levels may not be identical to the detected black level due to circuit spread but this can be corrected by detuning the reference tuned circuit.

The two colour difference signals are combined again after clamping and then applied to the modulator via de-emphasis, blanking and reinsertion circuits. The ratio of (R-Y) to (B-Y) at the de-emphasis output (pin 20) is 1,78.

Modulation

A burst signal is reinserted into the combined SECAM signal at the input to the PAL modulator. At this input the phase relationship for magenta colour is +(R-Y) and −(B-Y). The modulation carriers for the (R-Y) and (B-Y) signals are 90° out of phase; for a magenta colour the modulated (R-Y) component has the same phase position as the (R-Y) burst. The (B-Y) burst is modulated 180° out of phase with respect to the (B-Y) component of a magenta-coloured input signal.

Identification SECAM/$\overline{\text{SECAM}}$

Identification of the SECAM signal is performed using the fact that only SECAM signals have a line-to-line difference in voltage level. The identification circuit compares the phase of the demodulated voltage difference waveform with the phase of the flip-flop output. If the phase relationship is not correct, the flip-flop is reset by an extra pulse from the flip-flop trigger generator. For horizontal identification the phase comparison is performed during the period of pulse 'B' (see Fig. 2). When vertical identification is selected, the comparison is performed only during the horizontal scan of the vertical blanking. The SECAM identification circuits operate when selected by the voltage on pin 4; this may be horizontal, vertical or combined horizontal and vertical identification, depending on the switching arrangements of pin 4.
These are as follows:

- Horizontal identification preset when $V_{4\text{-}1} < 2{,}9$ V;
- Vertical identification preset when $V_{4\text{-}1} > 4{,}1$ V;
- Horizontal/vertical combination when sandcastle pulse is present on pin 4.

Information obtained from the identification detector is also used for colour killing and, if required, for switching to PAL.

Sandcastle pulse detection

The sandcastle pulse detector requires a three-level sandcastle pulse to provide horizontal blanking, vertical blanking and burst gate pulses. The detector burst gate pulse triggers a pulse generator which produces two timing pulses, pulse 'A' and pulse 'B' (see Fig. 2). Pulse 'A' is used to time the PAL modulator burst and to sample the (R-Y) and (B-Y) clamping pulse generators. A (R-Y) clamping pulse is generated only during a red line and a (B-Y) clamping pulse only during a blue line. Pulse 'B' times the SECAM horizontal identification.

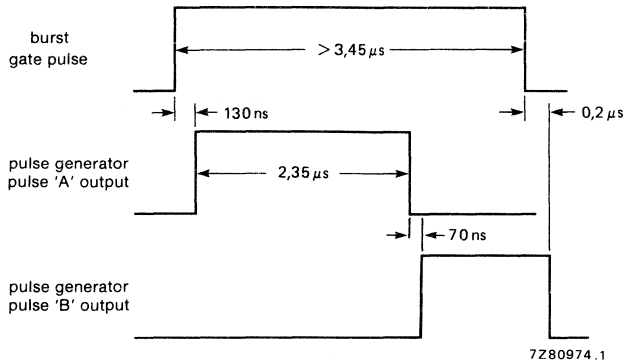


Fig. 2 Burst gate timing pulse generation.

Carrier generation

The carrier signal for the PAL modulator is obtained from a 4,43 MHz oscillator. An internal Miller integrator operates in conjunction with the decoupling capacitor at pin 10 to provide the required 90^{o} phase shift.

PAL matrix

The signal output from the PAL modulator at pin 9 is sequentially modulated with (R-Y) burst phased in the +(R-Y) direction, and (B-Y) burst phased in the −(B-Y) direction. This PAL signal is applied directly to pin 11 and via a 64 μs delay to pin 12. A true PAL signal is constructed in the PAL matrix by means of an additional/substraction process (in a correct H/2 sequence) using the delayed and undelayed inputs.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Coupling of identification systems

Coupling of a TDA3592A and a PAL decoder can be performed to obtain an optimum identification system. The system operates using the functions of pins 13, 6 and 7: the voltage level at pin 13 is controlled by the PAL/$\overline{\text{PAL}}$ detection of the PAL decoder; and the voltage level at pins 6 and 7 are functions of SECAM/$\overline{\text{SECAM}}$ detection in the TDA3592A.

The circuit action is as follows and is summarized in Table 1.

Channel switching — During channel switching pin 6 is taken rapidly to a high voltage (± 10,2 V), this corresponds to the $\overline{\text{SECAM}}$ mode of the TDA3592A.

PAL — The high voltage level at pin 6 caused by channel switching is maintained by the TDA3592A when it recognizes the signal as $\overline{\text{SECAM}}$ (this condition is maintained even if reflected PAL signals are present). The PAL decoder recognizes the signal as PAL and takes pin 13 of TDA3592A to a voltage greater than 1,7 V. The TDA3592A is now held in the $\overline{\text{SECAM}}$ condition by an internal current source at pin 6.

SECAM — The initial high voltage level (+ 10,2 V) at pin 6 caused by channel switching sets the TDA3592A in the $\overline{\text{SECAM}}$ mode and during this time the PAL decoder detects a $\overline{\text{PAL}}$ signal. This causes a voltage at pin 13 of $< 1{,}1$ V which prevents the internal current source of TDA3592A maintaining the high voltage level of pin 6 which, in turn, allows the TDA3592A to detect SECAM. The initiation of SECAM detection is delayed by the action of the external circuit at pins 6 and 7 and commences as pin 6 approaches 7,0 V. The SECAM signals are converted by TDA3592A to PAL signals at pin 14, which results in the PAL decoder switching to the PAL mode (the TDA3592A remains in the SECAM mode).

Black-and-white — The TDA3592A is initially set in the $\overline{\text{SECAM}}$ mode as previously described. The PAL decoder detects $\overline{\text{PAL}}$ and the TDA3592A detects $\overline{\text{SECAM}}$ which results in a system operation in the colour-killing mode.

Table 1 System operating modes

TDA3592A	PAL decoder mode	System operating mode
SECAM	PAL	SECAM
SECAM	$\overline{\text{PAL}}$	condition not used
$\overline{\text{SECAM}}$	PAL	PAL
$\overline{\text{SECAM}}$	$\overline{\text{PAL}}$	black-and-white

System priorities

When TDA3592A pin 13 is connected to the PAL/$\overline{\text{PAL}}$ output of a PAL decoder, the system will give PAL priority in signal identification. Connecting TDA3592A pin 13 to ground will give SECAM priority.

Luminance and chrominance signal paths

The signal input at pin 16 is clamped by a circuit which detects the top of the luminance signal sync pulse. This clamp, the luminance signal path to pin 15 and the $\overline{\text{SECAM}}$ signal path to pin 14 remain active when the supply voltage falls to (typ.) 5 V. At this level of supply voltage the SECAM processing circuits are switched off, giving a reduction in total power dissipation.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 17)	V_P	–	13,2	V
Total power dissipation	P_{tot}	–	1,78	W
Operating ambient temperature range	T_{amb}	−25	+70	°C
Storage temperature range	T_{stg}	−25	+150	°C

CHARACTERISTICS

$V_P = V_{17-1} = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified.
The parameter values are valid only when the reference tuned circuit has been aligned as detailed in note 1. All voltages are reference to ground pin 1.

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage (pin 17)		V_{17}	9,0	12	13,2	V
Supply current (pin 17)		I_{17}	65	90	115	mA
Supply current (pin 18)		I_{18}	40	–	160	μA
Decoupled supply voltage (pin 18)	$R_{ext17-18} = 2$ kΩ	V_{18}	8,8	11,8	13,2	V
External capacitance (pin 18)		C_{18}	–	–	10	μF
Total power dissipation		P_{tot}	–	1,08	1,38	W
Thermal resistance, junction to ambient		$R_{th\ j-a}$	–	40	45	K/W
Chrominance amplifier and demodulator						
Input signal SECAM (peak-to-peak value)		$V_{3(p-p)}$	–	–	1100	mV
Input signal SECAM at which correct limiting occurs (peak-to-peak value)		$V_{3(p-p)}$	15	100	300	mV
Input resistance (pin 3)		R_3	9,6	12,1	14,6	kΩ
Input capacitance (pin 3)		C_3	–	–	5	pF
Input resistance between pins 23 and 24		R_{23-24}	2,9	3,6	4,3	kΩ
Input capacitance between pins 23 and 24		C_{23-24}	–	12	–	pF
De-emphasis output resistance (pin 20)		R_{20}	0,9	1,1	1,3	kΩ
Chrominance demodulator zero point stability (pin 20)	note 2	f_0	–	5	–	kHz

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Chrominance amplifier and demodulator (continued)						
Linearity of (B-Y) demodulation (pin 20)	note 3	–	–	94	–	%
Linearity of (R-Y) demodulation (pin 20)	note 4	–	–	100	–	%
(R-Y)/(B-Y) ratio (pin 20)		–	–	1,78	–	%
Relative deviation of reinserted black level/demodulated black level (pin 20) as a function of temperature						
(R-Y) signals	note 5	–	–	0,22	–	kHz/°C
(B-Y) signals	note 5	–	–	0,22	–	kHz/°C
Identification SECAM/$\overline{\text{SECAM}}$	note 6					
Input voltage for line identification (pin 4)		V_4	4,1	–	V_P	V
Input voltage for frame identification (pin 4)		V_4	0	–	2,9	V
Switching level for line/frame identification (pin 4)		V_4	3,0	3,5	4,0	V
Input current (pin 4)		$-I_4$	–	5	25	μA
Voltage at pin 6 during $\overline{\text{SECAM}}$/PAL		V_6	–	10,2	–	V
Voltage at pin 6 during $\overline{\text{SECAM}}$/PAL		V_6	–	11,5	–	V
Voltage at pin 6 during SECAM		V_6	–	7,0	–	V
Identification at pin 6		V_6	–	10,6	–	V
Colour OFF for SECAM		V_6	9,8	10,1	10,4	V
Colour ON for SECAM		V_6	8,8	9,1	9,4	V
Slicing level reference voltage (pin 5)		V_5	–	8,4	–	V
Sandcastle pulse detector and clamping pulse generator						
Voltage level at which the vertical blanking pulse is separated		V_{19}	1,0	1,5	2,0	V
Voltage level at which the horizontal blanking pulse is separated		V_{19}	3,0	3,5	4,0	V
Voltage level at which the burst gating pulse is separated		V_{19}	6,5	7,0	7,5	V

parameter	conditions	symbol	min.	typ.	max.	unit
Sandcastle pulse detector and clamping pulse generator (continued)						
Input current	V_{19} = 0 V	$-I_{19}$	–	30	100	μA
Width of pulse 'A' (Fig. 2)	note 7		1,85	2,35	2,85	μA
Required width of pulse 'B' (Fig. 2)	note 7		0,6	–	–	μs
Luminance amplifier						
Input signal (peak-to-peak value) (pin 16)		$V_{16(p-p)}$	–	1,2	1,7	V
Gain (pin 16 to 15)	f_{16} = 4,4 MHz	G_{16-15}	6,5	7,5	8,5	dB
Input current (pin 16)		I_{16}	–	1,0	5,0	μA
Output impedance (pin 15)		Z_{15}	–	20	–	Ω
Frequency response at −3 dB (pin 15 and 16)		f	6,0	–	–	MHz
Gain (pin 16 to 14)	f_{16} = 4,4 MHz	G_{16-14}	6,0	7,0	8,0	dB
Frequency response at −3 dB (pin 14 and 16)		f	6,0	–	–	MHz
External load resistance (pin 15)		R_L	2,0	–	–	kΩ
Limiter, chrominance demodulator and PAL modulator	note 8					
Output resistance (pin 9)		R_9	–	25	–	Ω
DC output voltage during horizontal blanking (pin 9)		V_9	–	9,6	–	V
Internal biasing resistor for emitter follower (pin 9)			–	9,0	–	kΩ
External load resistance (pin 9)		$R_{L(9)}$	2	–	–	kΩ
Output signal (pin 9) when input to pin 3 has a Δf of 280 kHz; without external load (peak-to-peak value)		$V_{9(p-p)}$	–	0,82	–	mV
(R-Y)/(B-Y) ratio (pin 9)			1,50	1,78	2,11	
Chrominance/burst ratio for SECAM (pin 9)			2,5	3,0	3,5	
Linearity of (B-Y) signal (pin 9)	note 3		85	92	99	%
Linearity of (R-Y) signal (pin 9)	note 4		93	100	107	%
Black level shift as a function of temperature (pin 9)						
(R-Y) signals	note 9		–	0,22	–	kHz/°C
(B-Y) signals	note 9		–	0,22	–	kHz/°C

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Limiter, chrominance demodulator and PAL modulator (continued)						
Phase relationship of modulated (R-Y) burst to modulated (B-Y) burst (pin 9)			87	90	93	deg
Amplitude relationship of modulated (R-Y) burst to modulated (B-Y) burst (pin 9)			−1,5	0	+1,5	dB
Black level shift as a function of supply voltage (pin 9)						
(R-Y) signal			–	−1,5	–	kHz/V
(B-Y) signal			–	1,0	–	kHz/V
Oscillator						
Oscillator frequency (pin 9) (set with series capacitor)		f_{OSC}	–	4,433619	–	MHz
Frequency deviation without spread of external components (pin 9)		Δf_{OSC}	–	–	±150	Hz
Temperature coefficient of oscillator frequency (pin 9)			–	−2	−3	Hz/°C
Frequency deviation for change of V_P from 9,0 to 13,2 V		Δf_{OSC}	–	–	150	Hz
DC voltage (pin 8)		V_8	–	4,7	–	V
Input resistance (pin 8)		R_8	–	1	–	kΩ
DC voltage (pin 10)		V_{10}	–	4,4	–	V
Input resistance (pin 10)		R_{10}	–	2	–	kΩ
PAL matrix						
Input resistance (pin 11)		R_{11}	700	900	1100	Ω
Input resistance (pin 12)		R_{12}	700	900	1100	Ω
Output resistance (pin 14) (SECAM/$\overline{\text{SECAM}}$)		R_{14}	–	40	–	Ω
Internal emitter follower load resistance (pin 14)		$R_{INT(14)}$	–	7	–	kΩ
External load resistor (pin 14)		$R_{L(14)}$	2,4	–	–	kΩ
DC voltage (pin 11)		V_{11}	–	5,0	–	V
DC voltage (pin 12)		V_{12}	–	5,0	–	V
DC voltage (pin 14)	SECAM mode	V_{14}	–	6,2	–	V
DC voltage (pin 14)	$\overline{\text{SECAM}}$ mode and line blanking	V_{14}	–	4,9	–	V

parameter	conditions	symbol	min.	typ.	max.	unit
PAL matrix (continued)						
H/2 ripple on chrominance output (pin 14) (peak-to-peak value)	SECAM mode	$V_{14(p-p)}$	–	–	100	mV
Gain A; pin 11 to 14		G_A	9	10	11	dB
Gain B; pin 12 to 14 ((R-Y) at pin 9)		G_B	9	10	11	dB
Gain C; pin 12 to 14 ((B-Y) at pin 9)		G_C	9	10	11	dB
Gain A – gain B		G_A-G_B	–0,7	–	+0,7	dB
Gain A – gain C		G_A-G_C	–0,7	–	+0,7	dB
Gain B – gain C		G_B-G_C	–0,7	–	+0,7	dB
Phase A; pins 11, 14 to pins 12, 14 ((R-Y) at pin 9)			–	181,5	–	deg
Phase B; pins 11, 14 to pins 12, 14 ((B-Y) at pin 9)			–	1,5	–	deg
Phase A – phase B			178	180	182	deg
Identification PAL/$\overline{\text{PAL}}$						
Input condition for PAL (pin 13)		V_{13}	1,7	–	V_P	V
Input condition for $\overline{\text{PAL}}$ (pin 13)		V_{13}	–	–	1,1	V
Input current	V_{13} = 6 V	I_{13}	–	–	10	μA
Input resistance	V_{13} = 8,2 V	R_{13}	7,5	11,5	15,5	kΩ
Pin 6 internal current in PAL/$\overline{\text{SECAM}}$ mode		$-I_6$	0,24	0,4	0,58	mA
Switching level PAL/$\overline{\text{PAL}}$ (pin 13)		V_{13}	1,2	1,4	1,6	V

DEVELOPMENT DATA

CHARACTERISTICS AT LOW SUPPLY VOLTAGE

$V_P = V_{17-1} = 5$ V; $T_{amb} = 25$ °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply current		$I_{17}+I_{18}$	16	20	24	mA
Supply voltage switching level for preset SECAM signal path	SECAM processing OFF	V_{17-1}	6,5	7,5	8,2	V
Luminance amplifier						
Input signal (peak-to-peak value)		$V_{16(p-p)}$	–	0,45	0,56	V
Gain (pin 16 to 15)	$f_{16} = 4,4$ MHz	G_{16-15}	6,0	7,0	8,0	dB
Input current (pin 16)		I_{16}	–	1,0	5,0	μA
Output impedance (pin 15)		$\lvert Z_{15-1}\rvert$	–	20	–	Ω
Minimum load resistance (pin 15)		R_L	2	–	–	kΩ
Frequency response at –3 dB (pin 16 to 15)		f	6,0	–	–	MHz
Gain (pin 16 to 14)	$f_{16} = 4,4$ MHz	G_{16-14}	5,7	6,8	7,9	dB
Frequency response at –3 dB (pin 16 to 14)		f	6	–	–	MHz

Notes to the characteristics

1. The parameter values given in the characteristics are valid only when the following alignment procedure is performed:
   a. Supply a SECAM signal input to pin 3 at 100 mV (peak-to-peak value) without deviation during a red and blue line (SECAM black colour information).
   b. Align the reference tuned circuit so that the output signal from pin 14 to the PAL decoder is minimum during scan (PAL black colour information).
2. When the input signal to the limiter (pin 3) changes from 300 to 15 mV (peak-to-peak value) the zero point of the chrominance demodulator shifts by a typical value of 5 kHz; f = 4,33 MHz (typ.).
3. (B-Y) linearity is defined by $V_{out(yellow)}/V_{out(blue)}$ where f_{yellow} = (typ.) 4,02 MHz; f_{blue} = (typ.) 4,48 MHz.
4. (R-Y) linearity is defined by $V_{out(cyan)}/V_{out(red)}$ where f_{cyan} = (typ.) 4,68 MHz; f_{red} = (typ.) 4,12 MHz.
5. The parameter value is equated by: $\frac{(B\text{-}D)/F - (A\text{-}C)/E}{Y - X} \times \frac{\Delta f\ (kHz)}{^{o}C}$

   $E = \frac{E1 - E2}{2}$ $\quad F = \frac{F1 - F2}{2}$

   Where A = demodulated black level at temperature X
   B = demodulated black level at temperature Y
   C = artificial black level at temperature X
   D = artificial black level at temperature Y
   E1 = demodulated output signal at temperature X ($f_o - \Delta f$)
   E2 = demodulated output signal at temperature X ($f_o + \Delta f$)
   F1 = demodulated output signal at temperature Y ($f_o - \Delta f$)
   F2 = demodulated output signal at temperature Y ($f_o + \Delta f$)

   for B-Y: $f_o = f_{ob}$ = 4,25 MHz (Δf = 230 kHz)
   for R-Y: $f_o = f_{or}$ = 4,40625 MHz (Δf = 280 kHz)
6. During stable signal conditions V_7 is always at V_F(BAT85) below V_6.
7. The burst gate pulse width > 3,45 μs.
8. The specification figures are only valid when the reference tuned circuit is aligned as indicated in note 1.
9. Ensure that the 4,433 MHz carrier is in the correct phase; black level shift at temperature X = A and at Y = B.
   Output signal (Δf = 230 kHz for B-Y; Δf = 280 kHz for R-Y) at temperature X = E and at Y = F.
   The parameter is equated by: $\frac{(B/(F\text{-}B) - A/(E\text{-}A)}{Y - X} \times 230;\ 280\ kHz$
10. Chrominance definition — burst ratio at SECAM condition (pin 9).
    The parameter is equated by: $\frac{V_{out(p\text{-}p)}\ Red\ (R\text{-}Y)}{V_{burst(p\text{-}p)}\ (R\text{-}Y)}$.

DEVELOPMENT DATA

APPLICATION INFORMATION

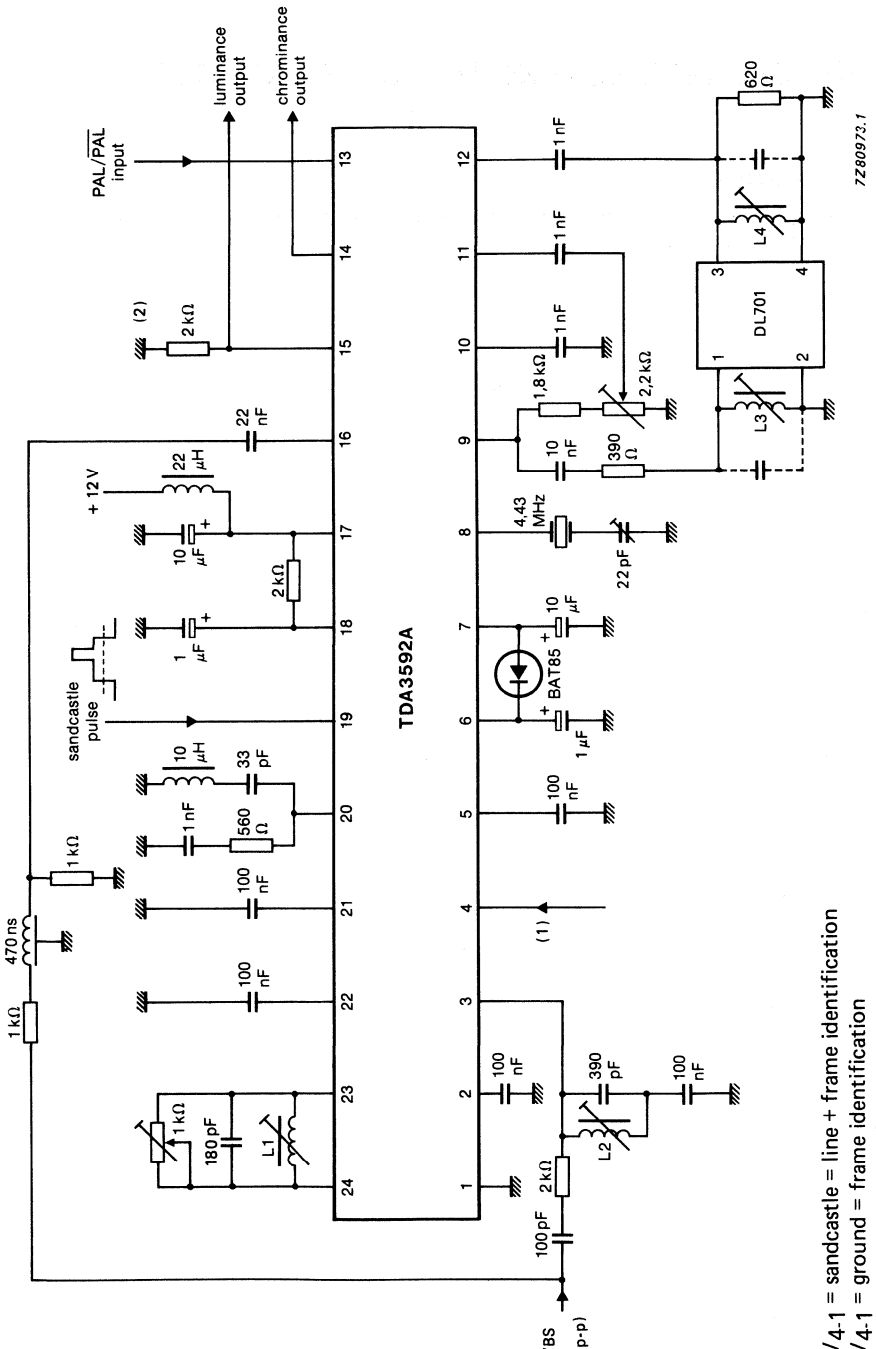


Fig. 3 Application circuit.

(1) V_{4-1} = sandcastle = line + frame identification
V_{4-1} = ground = frame identification
$V_{4-1} = V_P$ = line identification

(2) minimum load resistance at pin 15 = 2 kΩ

VERTICAL DEFLECTION AND GUARD CIRCUIT (90°)

GENERAL DESCRIPTION

The TDA3653B/C is a vertical deflection output circuit for drive of various deflection systems with currents up to 1.5 A peak-to-peak.

Features

- Driver
- Output stage
- Thermal protection and output stage protection
- Flyback generator
- Voltage stabilizer
- Guard circuit

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply (note 1)					
Supply voltage range					
pin 9	$V_P = V_{9-4}$	10	–	40	V
pin 6	V_{6-4}	–	–	60	V
Output (pin 5)					
Peak output voltage during flyback	V_{5-4M}	–	–	60	V
Output current	$I_{5(p-p)}$	–	1.2	1.5	A
Operating junction temperature range	T_j	−25	–	+150	°C
Thermal resistance junction to mounting base					
(SOT110B)	$R_{th\ j-mb}$	–	10	–	K/W
(SOT131)	$R_{th\ j-mb}$	–	3.5	–	K/W

Note to the quick reference data

1. The maximum supply voltage should be chosen such that during flyback the voltage at pin 5 does not exceed 60 V.

PACKAGE OUTLINES

TDA3653B: 9-lead SIL; plastic (SOT110B).
TDA3653C: 9-lead SIL; plastic power (SOT131).

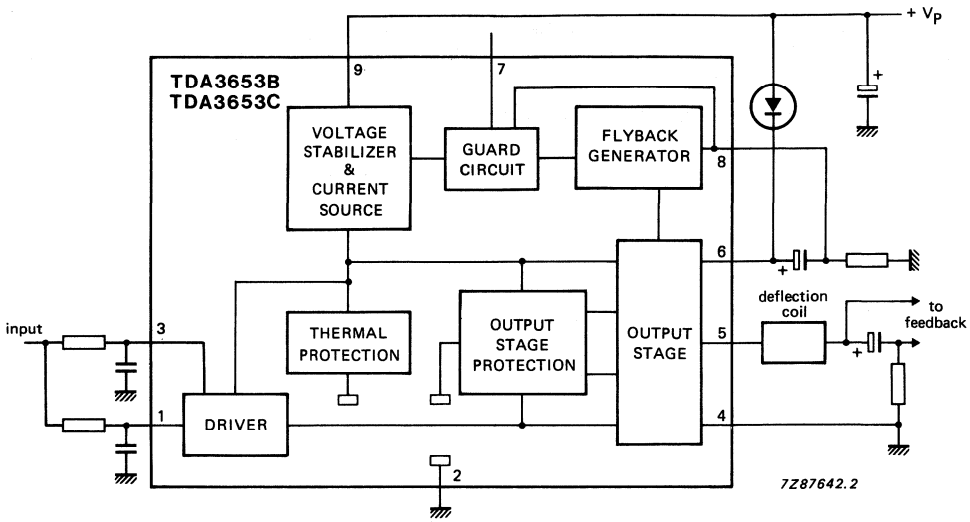


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

Output stage and protection circuit

Pin 5 is the output pin. The supply for the output stage is fed to pin 6 and the output stage ground is connected to pin 4. The output transistors of the class-B output stage can each deliver 0.75 A maximum. The maximum voltage for pin 5 and 6 is 60 V.

The output power transistors are protected such that their operation remains within the SOAR area. This is achieved by the co-operation of the thermal protection circuit, the current-voltage detector, the short-circuit protection and the special measures in the internal circuit layout.

Driver and switching circuit

Pin 1 is the input for the driver of the output stage. The signal at pin 1 is also applied via external resistors to pin 3 which is the input of a switching circuit. When the flyback starts, this switching circuit rapidly turns off the lower output stage and so limits the turn-off dissipation. It also allows a quick start of the flyback generator.

External connection of pin 1 to pin 3 allows for applications in which the pins are driven separately.

Flyback generator

During scan the capacitor connected between pins 6 and 8 is charged to a level which is dependent on the value of the resistor at pin 8 (see Fig.1).
When the flyback starts and the voltage at the output pin (pin 5) exceeds the supply voltage, the flyback generator is activated.
The supply voltage is then connected in series, via pin 8, with the voltage across the capacitor during the flyback period.
This implies that during scan the supply voltage can be reduced to the required scan voltage plus saturation voltage of the output transistors.
The amplitude of the flyback voltage can be chosen by changing the value of the external resistor at pin 8.
It should be noted that the application is chosen such that the lowest voltage at pin 8 is > 2.5 V, during normal operation.

Guard circuit

When there is no deflection current and the flyback generator is not activated, the voltage at pin 8 reduces to less than 1.8 V. The guard circuit will then produce a DC voltage at pin 7, which can be used to blank the picture tube and thus prevent screen damage.

Voltage stabilizer

The internal voltage stabilizer provides a stabilized supply of 6 V to drive the output stage, which prevents the drive current of the output stage being affected by supply voltage variations.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134); pins 4 and 2 externally connected to ground.

paramater	symbol	min.	max.	unit
Supply voltage (pin 9)	$V_P = V_{9-4}$	–	40	V
Supply voltage output stage (pin 6)	V_{6-4}	–	60	V
Output voltage (pin 5)	V_{5-4}	–	60	V
Input voltage (pins 1 and 3)	$V_{1;\,3-2}$	–	V_P	V
External voltage at pin 7	V_{7-2}	–	5.8	V
Peak output current (pin 5)				
repetitive	$\pm I_{5RM}$	–	0.75	A
non-repetitive	$\pm I_{5SM}$	–	1.5	A*
Peak output current (pin 8)				
repetitive	I_{8RM}	0.85	0.75	A
non-repetitive	$\pm I_{8SM}$	–	1.5	A*
Total power dissipation	P_{tot}	see Fig. 2		
Storage temperature range	T_{stg}	–65	+150	°C
Operating ambient temperature range	T_{amb}	see Fig. 2		
Operating junction temperature range	T_j	–25	+150	°C

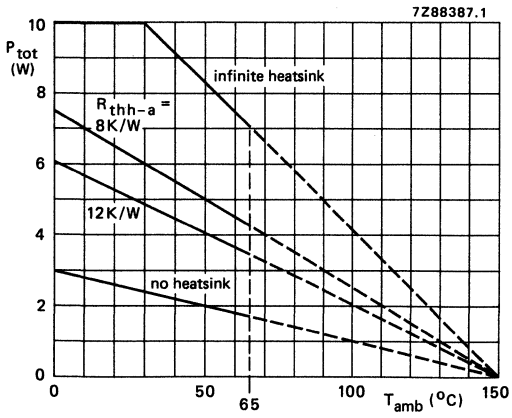


Fig. 2 Power derating curves (for SOT110B).

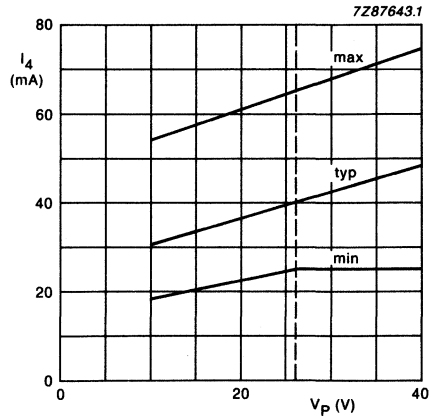


Fig. 3 Quiescent current I_4 as a function of supply voltage V_P.

* Non-repetitive duty factor maximum 3.3%.

CHARACTERISTICS

$V_P = V_{9-4} = 26$ V; $T_{amb} = 25$ °C; pins 2 and 4 externally connected to ground; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage (pin 9)	note 1	$V_P = V_{9-4}$	10	–	40	V
Supply voltage (pin 6)	note 1	V_{6-4}	–	–	60	V
Total supply current (pin 6 and pin 9)	note 2	$I_P = I_6 + I_9$	34	50	85	mA
Quiescent current (pin 4)	see Fig. 3	I_4	25	40	65	mA
Variation of quiescent current with temperature		ΔI_4	–	−0.04	–	mA/K
Output current						
Output current (pin 5) (peak-to-peak value)		$I_{5(p-p)}$	–	1.2	1.5	A
Output current flyback generator (pin 8)		$-I_8$	–	0.7	0.85	A
Output current flyback generator (pin 8)		I_8	–	0.6	0.75	A
Output voltage						
Peak voltage during flyback		V_{5-4M}	–	–	60	V
Saturation voltage to supply						
at $-I_5 = 0.75$ A		V_{6-5sat}	–	2.5	3.0	V
at $I_5 = 0.75$ A	note 3	V_{5-6sat}	–	2.5	3.0	V
at $-I_5 = 0.60$ A		V_{6-5sat}	–	2.2	2.7	V
at $I_5 = 0.60$ A	note 3	V_{5-6sat}	–	2.3	2.8	V
Saturation voltage to ground						
at $I_5 = 0.75$ A		V_{5-4sat}	–	2.3	2.7	V
at $I_5 = 0.60$ A		V_{5-4sat}	–	2.1	2.4	V
Flyback generator						
Saturation voltage						
at $-I_8 = 0.85$ A		V_{9-8sat}	–	1.6	2.1	V
at $I_8 = 0.75$ A	note 3	V_{8-9sat}	–	2.3	2.8	V
at $-I_8 = 0.70$ A		V_{9-8sat}	–	1.4	1.9	V
at $I_8 = 0.60$ A	note 3	V_{8-9sat}	–	2.2	2.7	V
Flyback generator active if:		V_{5-9}	4.0	–	–	V
Leakage current at pin 8		$-I_8$	–	5.0	100	μA
Input						
Input current (pin 1)	$I_5 = 0.75$ A	I_1	–	0.33	0.55	mA
Input voltage during scan (pin 1)	$I_5 = 0.75$ A	V_{1-2}	–	1.5	2.4	V
Input voltage during scan (pin 3) pins 1 and 3 not connected		V_{3-2}	0.8	–	V_P	V

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Input (continued)						
Input current during scan (pin 3)						
pins 1 and 3 not connected		I_3	0.03	–	–	mA
pins 1 and 3 connected		I_3	–	–	0.21	mA
Input resistance (pin 3)		R_3	3.9	5.3	6.7	kΩ
Input voltage during flyback (pin 1)		V_{1-2}	–	–	250	mV
Input voltage during flyback (pin 3)		V_{3-2}	–	–	250	mV
Guard circuit						
Output voltage (pin 7)	note 4					
loaded with 100 kΩ		V_{7-2}	4.4	5.1	5.8	V
loaded with 0.5 mA		V_{7-2}	3.6	4.4	5.3	V
Internal series resistance of pin 7		R_{i7}	0.95	1.35	1.7	kΩ
Guard circuit active if V_{8-2} is lower than	note 5	V_{8-2}	–	–	1.8	V
General data						
Thermal protection becomes active if junction temperature exceeds		T_j	158	175	192	°C
Thermal resistance junction to mounting base		$R_{th\ j\text{-}mb}$	–	10	12	K/W
Open loop gain at 1 kHz	note 6	G_{ol}	–	42	–	dB
Frequency response (–3 dB)	note 7	f	–	40	–	kHz

Notes to the characteristics

1. The maximum supply voltage should be chosen such that during flyback the voltage at pin 5 does not exceed 60 V.
2. When V_{5-4} = 13 V and no load at pin 5.
3. Duty factor maximum 3.3%.
4. Guard circuit is active.
5. During normal operation the voltage V_{8-2} may not be lower than 2.5 V.
6. R_{load} = 8 Ω; $I_{load(rms)}$ = 125 mA.
7. With 220 pF between pins 1 and 5.

APPLICATION INFORMATION

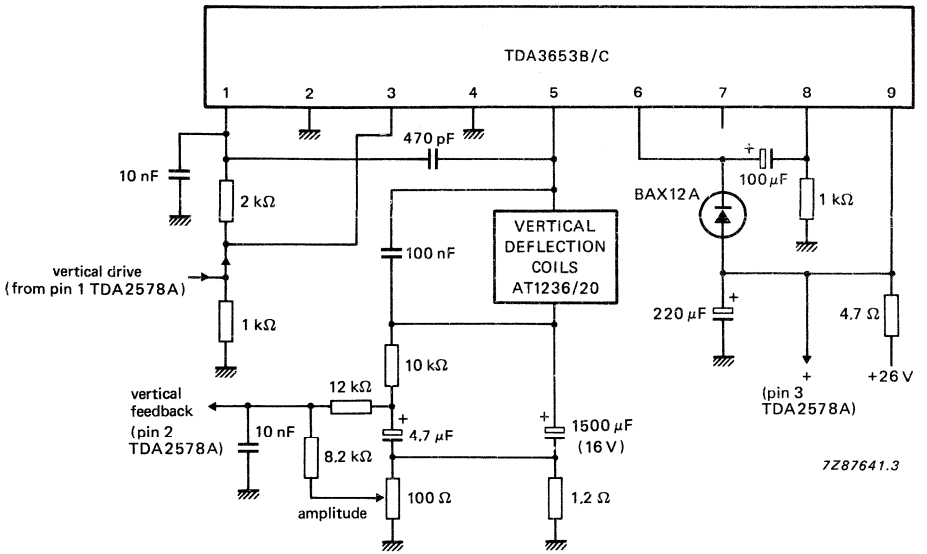


Fig. 4 Typical application circuit diagram of the TDA3653B/C (vertical output), when used in combination with the TDA2578A (see Fig. 5).

Note to deflection coils AT1236/20: L = 29 mH, R = 13.6 Ω; deflection current without overscan is 0.82 A peak-to-peak and EHT voltage is 25 kV.

APPLICATION INFORMATION (continued)

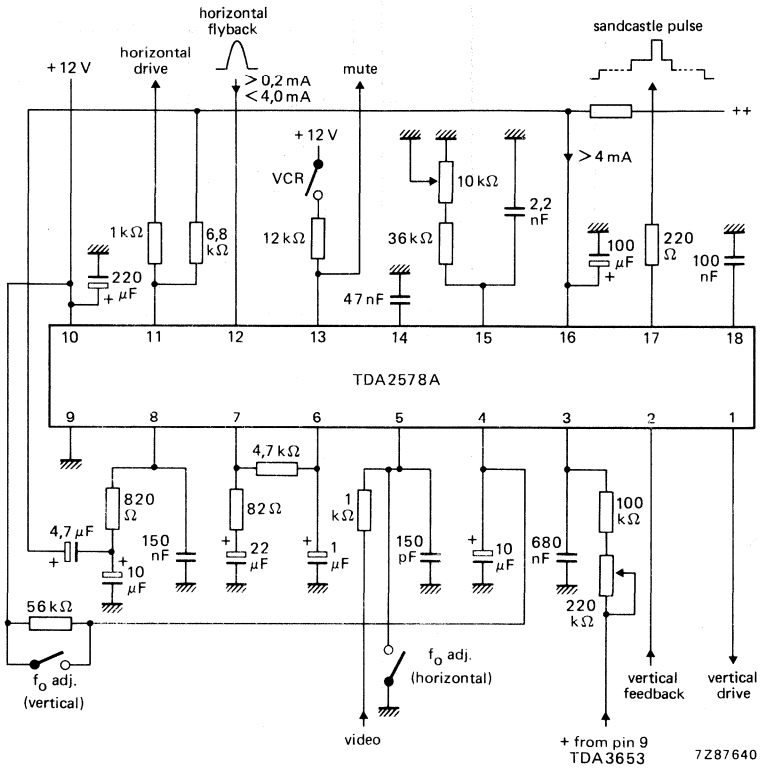


Fig. 5 Typical application circuit diagram; for combination of the TDA2578A with the TDA3653B/C (see Fig. 4).

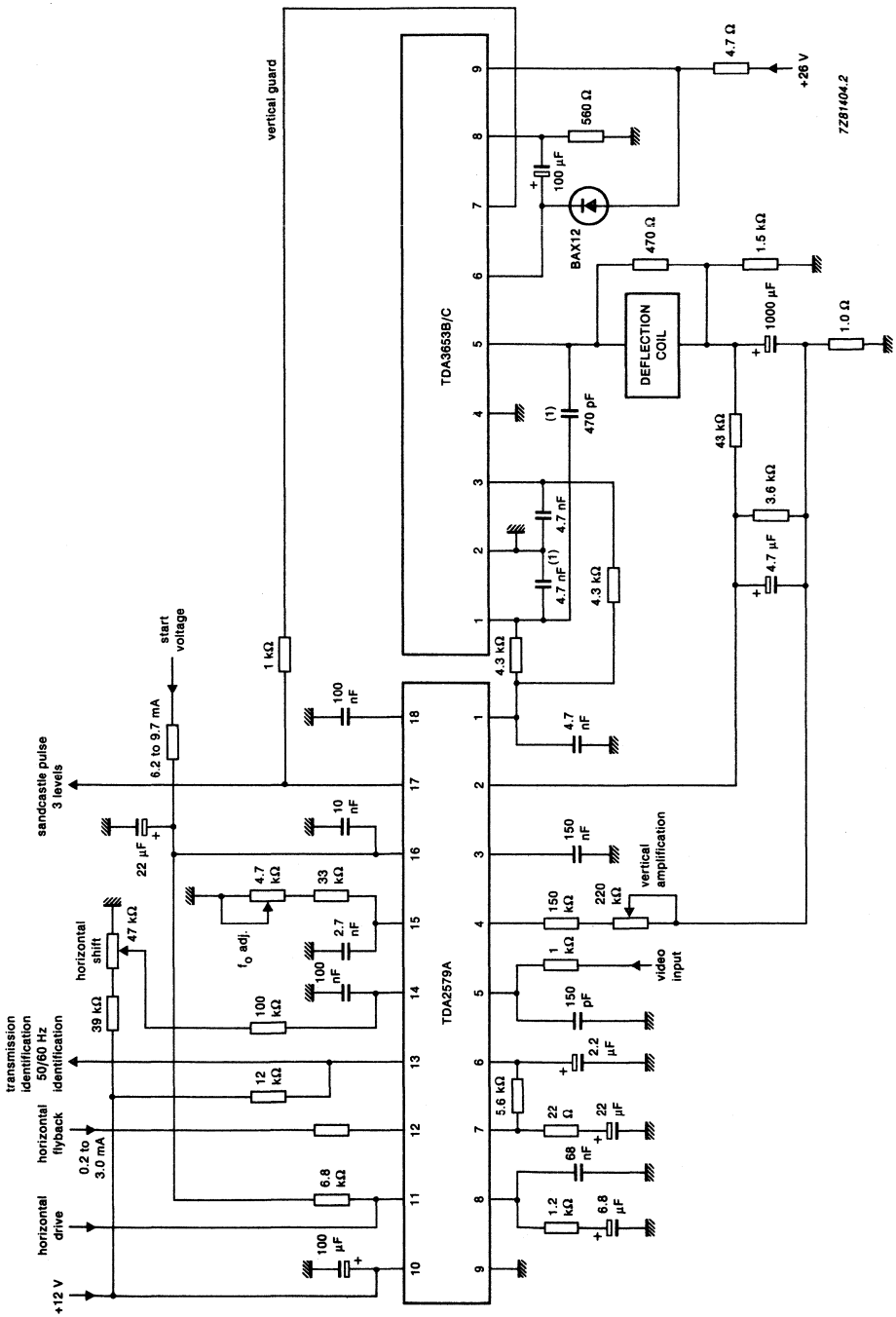


Fig.6 Application circuit diagram for combination with TDA2579A for 90° picture tube.

(1) Dependent on PCB layout.

VERTICAL DEFLECTION AND GUARD CIRCUIT (110°)

GENERAL DESCRIPTION

The TDA3654 is a full performance vertical deflection output circuit for direct drive of the deflection coils and can be used for a wide range of 90° and 110° deflection systems.
A guard circuit is provided which blanks the picture tube screen in the absence of deflection current.

Features

- Direct drive to the deflection coils
- 90° and 110° deflection system
- Internal blanking guard circuit
- Internal voltage stabilizer

QUICK REFERENCE DATA

Output voltage	V_{5-2}	max.	60 V
Output current (peak-to-peak)	$I_{5(p-p)}$	max.	3 A
Supply voltage	V_{9-2}	max.	40 V
Guard circuit output voltage	V_{7-2}	max.	5,6 V
Operating ambient temperature range	T_{amb}		−25 to +60 °C
Storage temperature	T_{stg}		−65 to +150 °C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	3,5 to 4 K/W

PACKAGE OUTLINES

TDA3654 : 9-lead SIL; plastic power (SOT131).
TDA3654Q : 9-lead SIL bent to DIL; plastic power (SOT157).

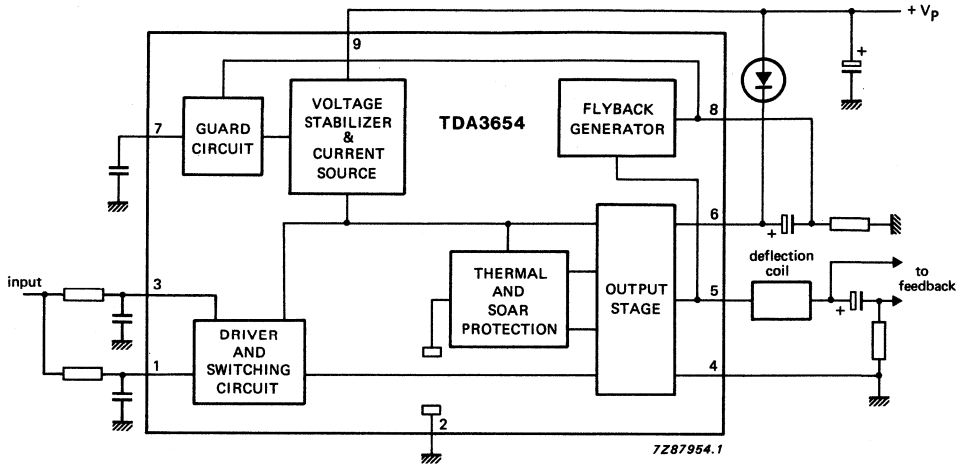


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

Output stage and protection circuits

The output stage consists of two Darlington configurations in class B arrangement.
Each output transistor can deliver 1,5 A maximum and the V_{CEO} is 60 V.
Protection of the output stage is such that the operation of the transistors remains well within the SOAR area in all circumstances at the output pin, (pin 5). This is obtained by the cooperation of the thermal protection circuit, the current-voltage detector and the short circuit protection.
Special measures in the internal circuit layout give the output transistors extra solidity, this is illustrated in Fig. 5 where typical SOAR curves of the lower output transistor are given. The same curves also apply for the upper output device. The supply for the output stage is fed to pin 6 and the output stage ground is connected to pin 4.

Driver and switching circuit

Pin 1 is the input for the driver of the output stage. The signal at pin 1 is also applied to pin 3 which is the input of a switching circuit (pin 1 and 3 are connected via external resistors).
This switching circuit rapidly turns off the lower output stage when the flyback starts and it, therefore, allows a quick start of the flyback generator. The maximum required input signal for the maximum output current peak-to-peak value of 3 A is only 3 V, the sum of the currents in pins 1 and 3 is then maximum 1 mA.

Flyback generator

During scan, the capacitor between pins 6 and 8 is charged to a level which is dependent on the value of the resistor at pin 8 (see Fig. 1).
When the flyback starts and the voltage at the output pin (pin 5) exceeds the supply voltage, the flyback generator is activated.
The supply voltage is then connected in series, via pin 8, with the voltage across the capacitor during the flyback period.
This implies that during scan the supply voltage can be reduced to the required scan voltage plus saturation voltage of the output transistors.
The amplitude of the flyback voltage can be chosen by changing the value of the external resistor at pin 8.
It should be noted that the application is chosen such that the lowest voltage at pin 8 is $> 1{,}5$ V, during normal operation.

Guard circuit

When there is no deflection current, for any reason, the voltage at pin 8 becomes less than 1 V, the guard circuit will produce a d.c. voltage at pin 7. This voltage can be used to blank the picture tube, so that the screen will not burn in.

Voltage stabilizer

The internal voltage stabilizer provides a stabilized supply of 6 V to drive the output stage, so the drive current is not affected by supply voltage variations.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).
Pins 2 and 4 are externally connected to ground.

Voltages				
Output voltage	V_{5-4}		0 to 60	V
Supply voltage	V_{9-4}		0 to 40	V
Supply voltage output stage	V_{6-4}		0 to 60	V
Input voltage	V_{1-2}		0 to V_{9-4}	V
Input voltage switching circuit	V_{3-2}		0 to V_{9-4}	V
External voltage at pin 7	V_{7-2}		0 to 5,6	V
Currents				
Repetitive peak output current	$\pm I_{5RM}$	max.	1,5	A
Non-repetitive peak output current (note 1)	$\pm I_{5SM}$	max.	3	A
Repetitive peak output current of flyback generator	I_{8RM}	max.	+ 1,5 −1,6	A A
Non-repetitive peak output current of flyback generator (note 1)	$\pm I_{8SM}$	max.	3	A
Temperatures				
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range (see Fig. 3)	T_{amb}		−25 to + 60	°C
Operating junction temperature range	T_j		−25 to + 150	°C

CHARACTERISTICS

T_{amb} = 25 °C, supply voltage (V_{9-4}) = 26 V; unless otherwise stated; pin 1 externally connected to pin 3. Pins 2 and 4 externally connected to ground.

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage, pin 9 (note 2)	V_{9-4}	10	–	40	V
Supply voltage output stage	V_{6-4}	–	–	60	V
Supply current, pins 6 and 9 (note 3)	I_6+I_9	35	55	85	mA
Quiescent current (note 4)	I_4	25	40	65	mA
Variation of quiescent current with temperature	TC	–	–0,04	–	mA/K
Output current					
Output current, pin 5 (peak-to-peak)	$I_{5(p-p)}$	–	2,5	3	A
Output current flyback generator, pin 8	$+I_{8(p-p)}$	–	1,25	1,5	A
	$-I_{8(p-p)}$	–	1,35	1,6	A
Output voltage					
Peak voltage during flyback	V_{5-4}	–	–	60	V
Saturation voltage to supply					
at I_5 = –1,5 A	$V_{6-5(sat)}$		2,5	3,2	V
at I_5 = 1,5 A (note 5)	$V_{5-6(sat)}$		2,5	3,2	V
at I_5 = –1,2 A	$V_{6-5(sat)}$		2,2	2,7	V
at I_5 = 1,2 A (note 5)	$V_{5-6(sat)}$		2,3	2,8	V
Saturation voltage to ground					
at I_5 = 1,2 A	$V_{5-4(sat)}$	–	2,2	2,7	V
at I_5 = 1,5 A	$V_{5-4(sat)}$	–	2,5	3,2	V
Flyback generator					
Saturation voltage					
at I_8 = –1,6 A	$V_{9-8(sat)}$	–	1,6	2,1	V
at I_8 = 1,5 A (note 5)	$V_{8-9(sat)}$	–	2,3	3	V
at I_8 = –1,3 A	$V_{9-8(sat)}$	–	1,4	1,9	V
at I_8 = 1,2 A (note 5)	$V_{8-9(sat)}$	–	2,2	2,7	V
Leakage current at pin 8	$-I_8$	–	5	100	μA
Flyback generator active if:	V_{5-9}	4	–	–	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Input					
Input current, pin 1, for I_5 = 1,5 A	I_1	–	0,33	0,55	mA
Input voltage during scan, pin 1	V_{1-2}	–	2,35	3	V
Input current, pin 3, during scan (note 6)	I_3	0,03	–	–	mA
Input voltage, pin 3, during scan (note 6)	V_{3-2}	0,8	–	V_{9-4}	V
Input voltage, pin 1, during flyback	V_{1-2}	–	–	250	mV
Input voltage, pin 3, during flyback	V_{3-2}	–	–	250	mV
Guard circuit					
Output voltage, pin 7 R_L = 100 kΩ (note 9)	V_{7-2}	4,1	4,5	5,8	V
Output voltage, pin 7 at I_L = 0,5 mA (note 9)	V_{7-2}	3,4	3,9	5,3	V
Internal series resistance of pin 7	Ri_7	0,95	1,35	1,7	kΩ
Guard circuit activates (note 7)	V_{8-2}	–	–	1,0	V
General data					
Thermal protection activation range	T_j	158	175	192	°C
Thermal resistance					
From junction to mounting base	$R_{th\ j\text{-}mb}$	–	3,5	4	K/W
Power dissipation	P_{tot}	–	see Fig. 3		
Open loop gain at 1 kHz; (note 8)	G_o	–	33	–	
Frequency response, –3 dB; (note 10)	f	–	60	–	kHz

Notes to the characteristics

1. Non-repetitive duty factor 3,3%.
2. The maximum supply voltage should be chosen so that during flyback the voltage at pin 5 does not exceed 60 V.
3. When V_{5-4} is 13 V and no load at pin 5.
4. See Fig. 4.
5. Duty cycle, d = 5% or d = 0,05.
6. When pin 3 is driven separately from pin 1.
7. During normal operation the voltage V_{8-2} may not be lower than 1,5 V.
8. $R_L = 8\ \Omega$; $I_L = 125$ mA (r.m.s.).
9. If guard circuit is active.
10. With a 22 pF capacitor between pins 1 and 5.

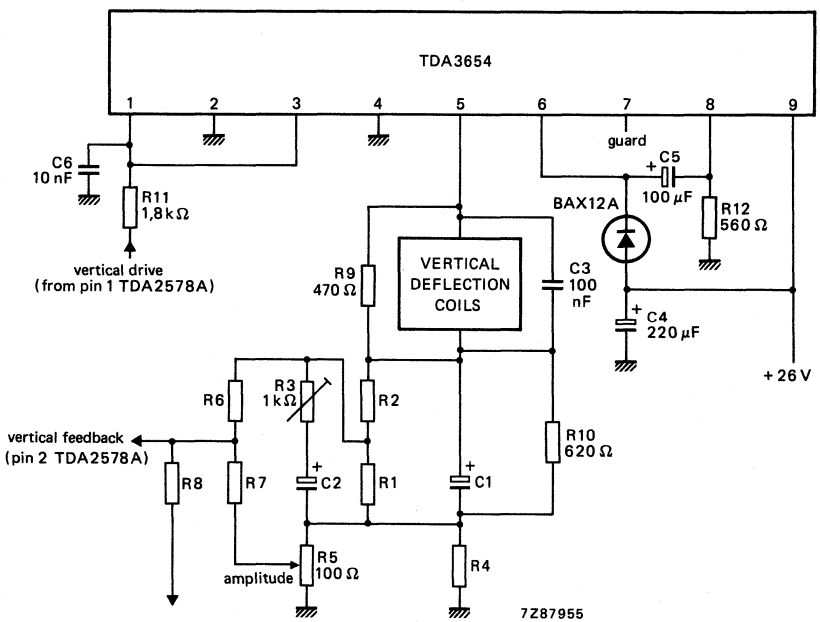


Fig. 2 Application diagram.

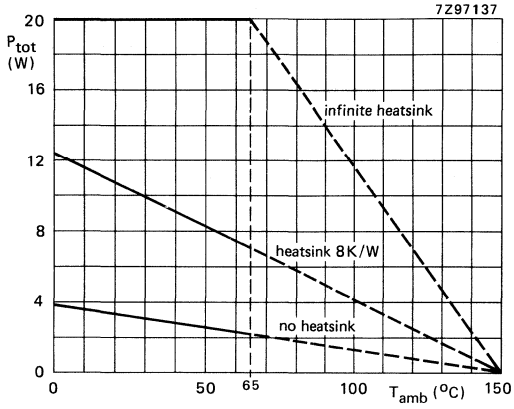


Fig. 3 Power derating curve.

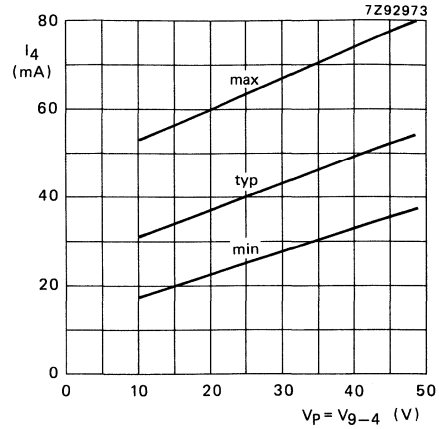
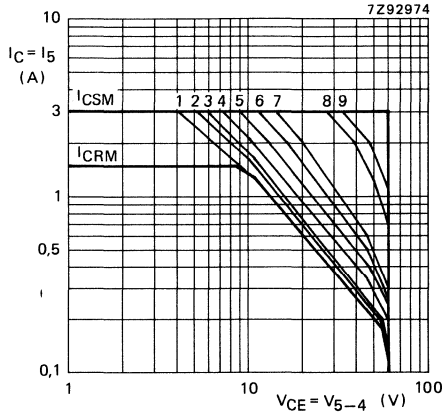


Fig. 4 Quiescent current as a function of the supply voltage.

curve	t_p	δ	peak junction temperature
1	d.c.	—	150 °C
2	10 ms	0,5	150 °C
3	10 ms	0,25	150 °C
4	1 ms	0,5	150 °C
5	1 ms	0,25	150 °C
6	1 ms	0,05	150 °C
7	1 ms	0,05	180 °C
8	0,2 ms	0,1	150 °C
9	0,2 ms	0,1	180 °C



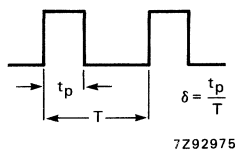


Fig. 5 Typical SOAR of lower output transistor.

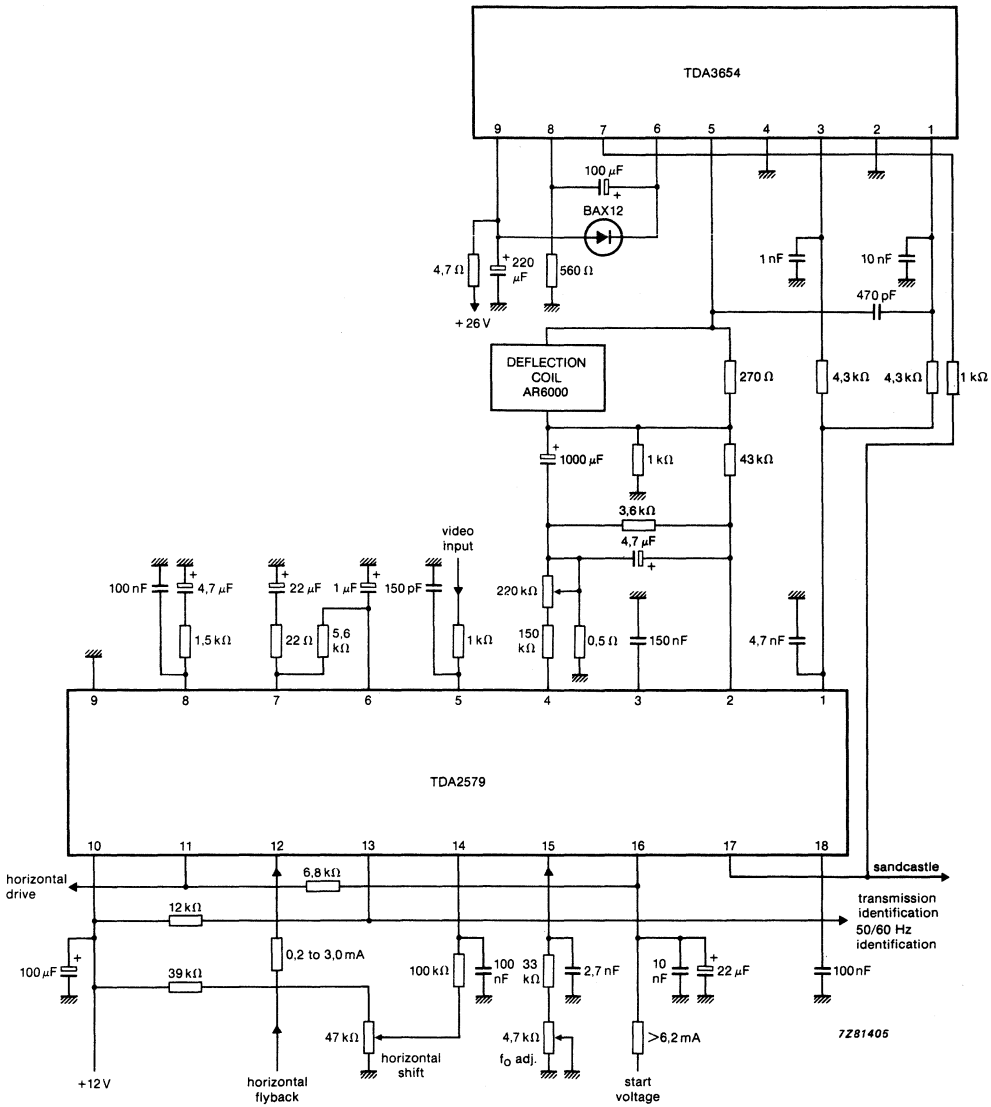


Fig. 6 Application diagram in combination with TDA2579.

SECAM IDENTIFICATION CIRCUIT

GENERAL DESCRIPTION

The TDA3724 is a monolithic integrated circuit for SECAM identification in PAL/SECAM (B,G) video tape recorders.

QUICK REFERENCE DATA

Supply voltage (pin 10)	$V_P = V_{10-8}$	typ.	10 V
Supply current (pin 10)	$I_P = I_{10}$	typ.	16 mA
Identification inputs	V_{3-8} (p-p)	min.	0,22 V
Identification inputs	V_{4-8} (p-p)	min.	0,22 V
Identification output current	I_1	min.	3 mA

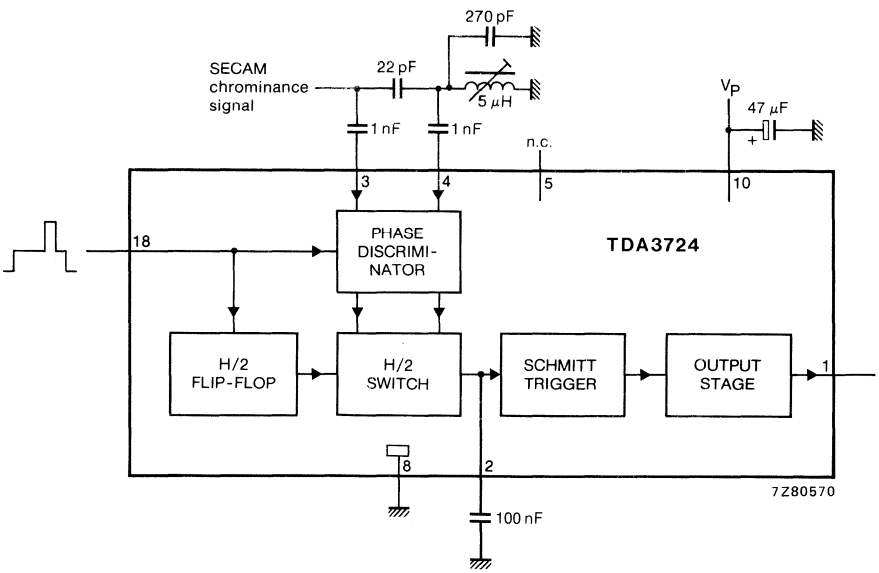


Fig. 1 Block diagram.

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_P = V_{10-8}$	max.	13,2	V
Voltage range at pins 3,4,18	V_{n-8}		0 to V_P	V
Voltage range at pin 2	V_{2-8}		½V_P to V_P	V
Current at pin 1	$-I_1$		5	mA
Storage temperature range	T_{stg}		−25 to +150	°C
Operating ambient temperature range	T_{amb}		0 to 70	°C

CHARACTERISTICS

V_P = 10 V; T_{amb} = 25 °C; measured in Fig. 1; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply at pin 10					
Supply voltage	$V_P = V_{10-8}$	9,6	10	13,2	V
Supply current at V_P = 10 V	I_{10}	–	16	21	mA
Supply current at V_P = 13,2 V	I_{10}	–	–	28	mA
Output voltage at pin 1 (open collector of pnp transistor) at SECAM mode	V_{1-8}	9,3	–	–	V
Output current pin 1 at SECAM mode	$-I_1$	3	–	–	mA
Output current pin 1 at NOT SECAM mode	$-I_1$	–	–	10	μA
Charge capacitor for ident. integration	C_{2-8}	100	–	2000	nF
Identification inputs pin 3,4					
input voltage	$V_{3,4-8\ (p-p)}$	0,22	–	1,0	V
input resistance	$R_{3,4-8}$	14	–	22	kΩ
Sandcastle input pin 18					
input voltage for active discriminating stage	V_{18-8}	6,0	–	V_P	V

SECAM (L) CHROMINANCE PROCESSOR FOR VIDEO RECORDERS

GENERAL DESCRIPTION

The TDA3725 is a monolithic integrated circuit for chrominance processing in SECAM (L) video recorders.

Features

- SECAM identification with output stage of SECAM/NOT SECAM identification
- Input to force recording or playback mode
- A.G.C. amplifier and soft limiting amplifier for SECAM chrominance inputs
- Divide by 4 of the chrominance frequencies for recording mode
- Rectifier and multiplier to generate 4 times SECAM chrominance frequencies at playback mode with external filtering
- Output for monitoring

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 10)	$V_P = V_{10\text{-}8}$	–	10	–	V
Supply current (pin 10)	$I_p = I_{13}$	–	38	–	mA
Chroma input signal (record)	$V_{11\text{-}8(p\text{-}p)}$	25	–	–	mV
Chroma input signal (playback)	$V_{9\text{-}8(p\text{-}p)}$	25	–	–	mV
Identification inputs	$V_{3\text{-}8(p\text{-}p)}$	0,22	–	1	V
Identification inputs	$V_{4\text{-}8(p\text{-}p)}$	0,22	–	1	V
Identification output current	I_1	3	–	–	mA
Monitor output	$V_{14\text{-}8(p\text{-}p)}$	–	0,6	–	V
Suppression of 2,2 MHz	α_{14}	–	35	–	dB
Suppression of 8,8 MHz	α_{14}	–	10	–	dB
Recording output (a.c.)	$V_{16\text{-}8(p\text{-}p)}$	–	3	–	V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

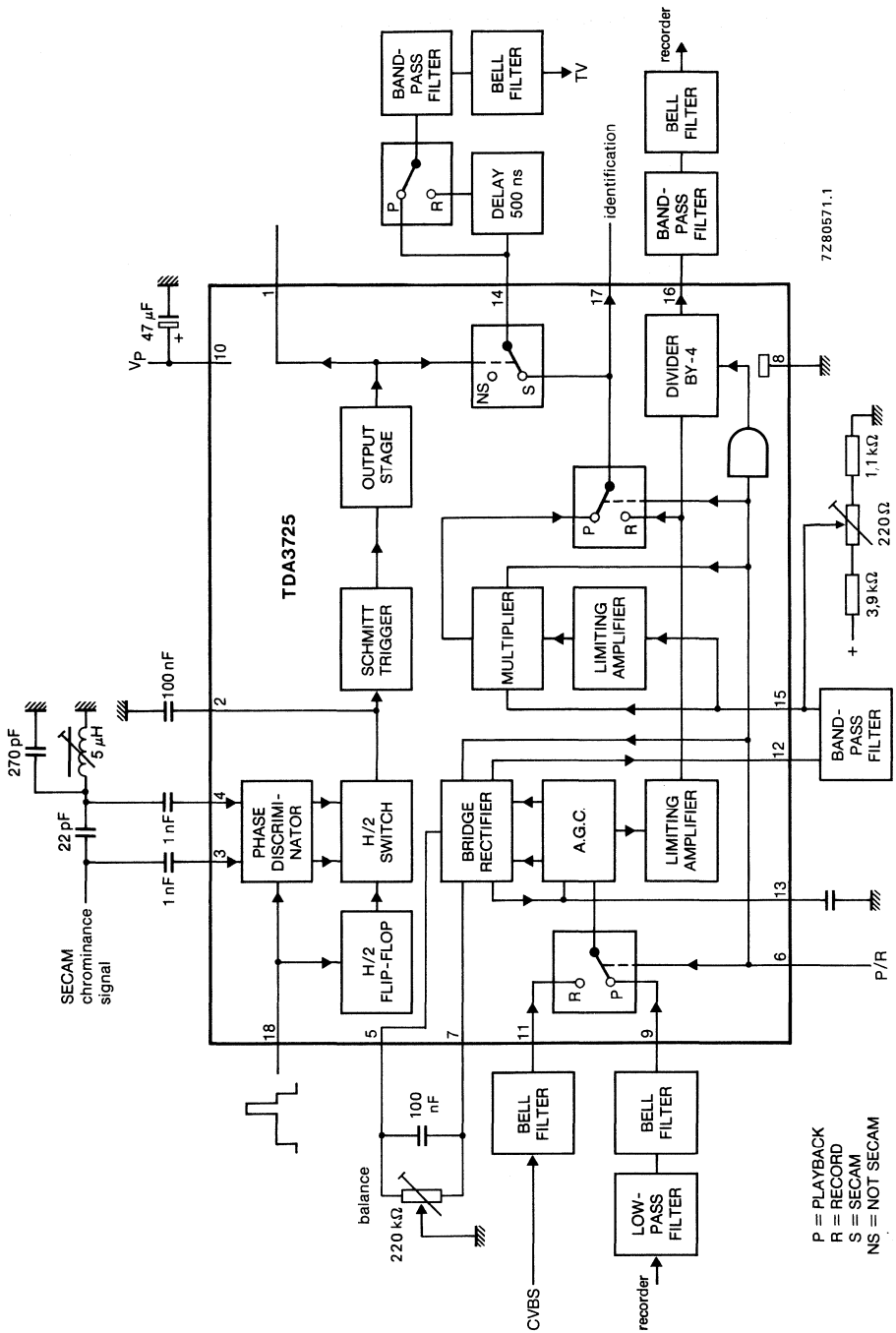


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	typ.	max.	unit
Supply voltage pin 10	$V_P = V_{10-8}$	–	–	13,2	V
Voltage range at pins 3,4,5,6, 7,9,11,15,18 to pin 8 (ground)	V_{n-8}	0	–	V_P	V
Voltage range at pin 2 to pin 8	V_{2-8}	$\frac{1}{2}V_P$	–	V_P	V
Currents at pins 1,12,13,14,16,17	$-I_n$	–	–	5	mA
Storage temperature range	T_{stg}	−25	–	+ 150	°C
Operating ambient temperature range	T_{amb}	0	–	+ 70	°C

CHARACTERISTICS

V_P = 10 V; T_{amb} = 25 °; measured in Fig. 1, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 10)					
Supply voltage	$V_P = V_{10-8}$	9,6	10	13,2	V
Supply current at V_P = 10 V	I_{10}	–	38	50	mA
Supply current at V_P = 13,2 V	I_{10}	–	–	66	mA
Input switch and a.g.c.					
Input signal at record mode	$V_{11-8(p-p)}$	25	–	500	mV
Input signal at playback mode	$V_{9-8(p-p)}$	25	–	150	mV
Output signal (rectified) pin 12 (2,2 MHz)	$V_{12-8(p-p)}$	–	300	–	mV
d.c. level	V_{12-8}	5,0	5,5	–	V
Suppression of 1,1 MHz	α_{12}	30	32	–	dB
Suppression of 3,3 MHz	α_{12}	40	42	–	dB
Suppression of 4,4 MHz	α_{12}	10	14	–	dB
Output resistance	R_{12-8}	–	V_T/I_C	–	Ω
Mixer and limiter					
Input resistance pin 15	R_{15-8}	0,5	–	–	MΩ
Output signal pin 14 (4,4 MHz)	$V_{14-8(p-p)}$	0,3	0,4	–	V
d.c. level	V_{14-8}	5,0	5,5	–	V
Suppression of 2,2 MHz and 6,6 MHz	α_{14}	30	35	–	dB
Suppression of 8,8 MHz	α_{14}	12	14	–	dB
Output resistance	R_{14-8}	–	V_T/I_C	–	Ω
Output signal pin 17 (4,4 MHz)	$V_{17-8(p-p)}$	0,3	0,4	–	V
d.c. level	$V_{17-8(p-p)}$	6,0	6,5	–	V
Output resistance	R_{17-8}	–	V_T/I_C	–	Ω
Divider and limiter					
Output signal pin 16	$V_{16-8(p-p)}$	2,5	3	–	V
d.c. level	V_{16-8}	3,5	4	–	V
Output resistance	R_{16-8}	–	V_T/I_C	–	Ω
Input for playback/record switching					
Input voltage record	V_{6-8}	0	–	5	V
Input voltage playback	V_{6-8}	7	–	V_P	V
Identification					
Output voltage pin 1 (open collector of pnp transistor) in SECAM mode	V_{1-8}	9,3	–	–	V
Output current pin 1 in SECAM mode	$-I_1$	3	–	–	mA
Output current pin 1 in NOT SECAM mode	$-I_1$	–	–	1	μA
Charge capacitor for ident integration	C_{2-8}	100	–	1000	nF
Threshold colour forced on	V_{2-8}	8	–	V_P	V
Threshold killer forced on	V_{2-8}	5,8	–	6,2	V
Identification input voltage pin 3	$V_{3-8(p-p)}$	0,22	–	1	V
Identification input voltage pin 4	$V_{4-8(p-p)}$	0,22	–	1	V
Input resistance pins 3,4	$R_{3,4-8}$	14	18	22	kΩ
Sandcastle input pin 18					
Input voltage for inactive discriminating stage	V_{18-8}	0	–	4,8	V
Input voltage for active discriminating stage	V_{18-8}	6	–	V_P	V

FREQUENCY DEMODULATOR AND DROP OUT COMPENSATOR FOR VIDEO RECORDERS

GENERAL DESCRIPTION

The TDA3730 is a monolithic integrated circuit for luminance processing in the playback path of video recorders. The device incorporates two signal channels, one for the main signal and one for the drop out signal.

Features

- FM preamplifier
- Limiter in main and drop out channel
- Demodulator in main and drop out channel
- Drop out detector with Schmitt-trigger
- Electronic switches for FM and video signal controlled by drop out detector
- Linear and dynamic video de-emphasis
- D.C. reference stabilizer

QUICK REFERENCE DATA

Supply voltage (pin 7 and pin 23)	$V_P = V_{7,\ 23\text{-}5,\ 25}$	typ.	10 V
Supply current (pin 7 + pin 23)	$I_P = I_7 + I_{23}$	typ.	40 mA
FM input signal (pin 17) (peak-to-peak value)	$V_{17\text{-}25(p\text{-}p)}$	typ.	100 mV
Video output signal (pin 26) (peak-to-peak value)	$V_{26\text{-}5(p\text{-}p)}$	typ.	2 V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

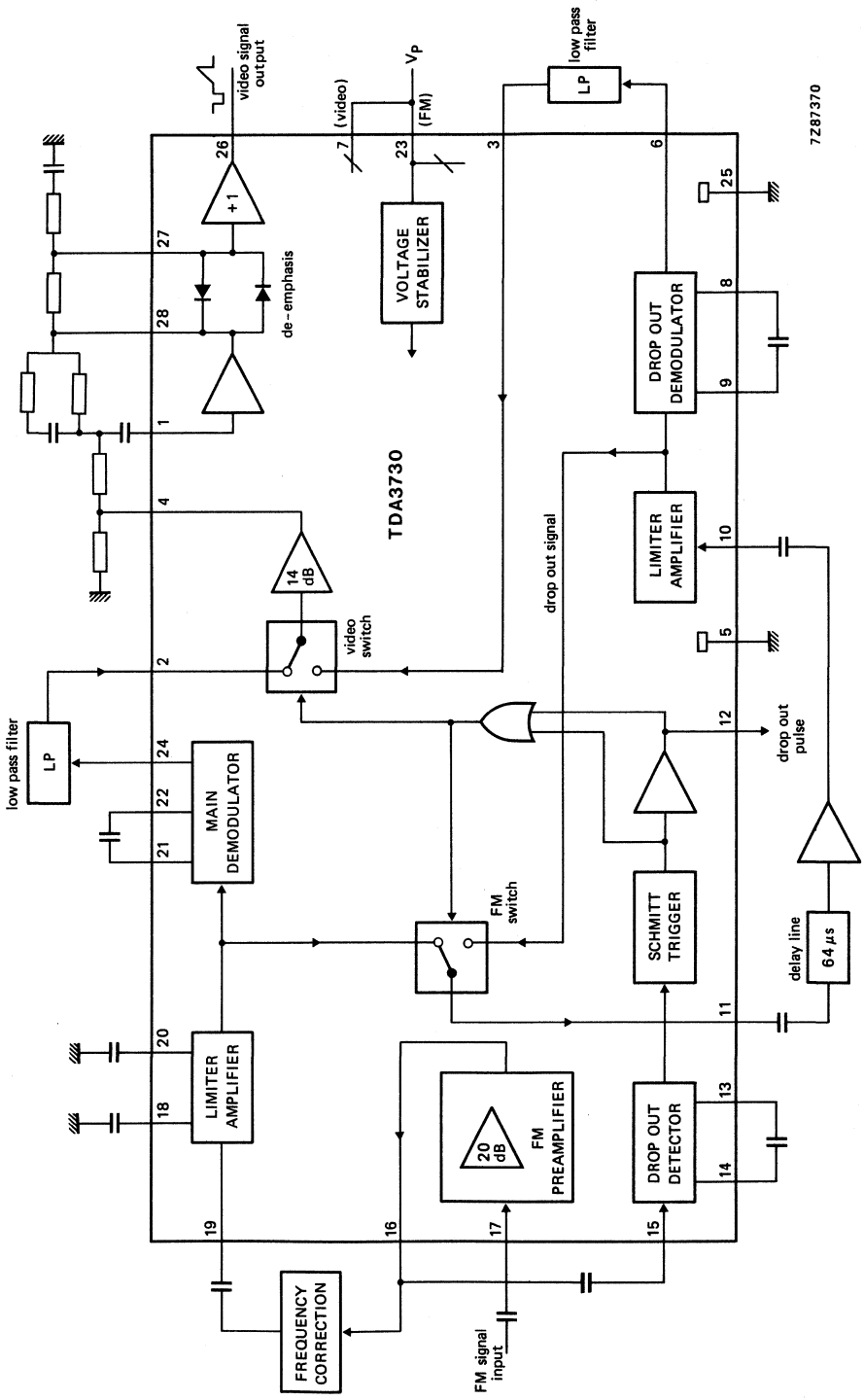


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pins 7 and 23)	$V_P = V_{7,23-5,25}$	max.	13,2 V
Voltage range at pins 1, 2, 3, 4, 5, 6, 10, 11, 12, 15, 16, 17, 18, 19, 20, 24, 26 to pin 5 and 25 (ground)	$V_{n-5,25}$		0 to V_P V
Voltage at pins 8, 9, 13, 14, 21, 22 to pin 5 and 25 (ground)	$V_{n-5,25}$	max.	V_P V
Voltage at pins 27, 28 to pin 5 and 25 (ground)	$V_{n-5,25}$	min.	0 V
Currents			
at pins 8, 9, 13, 14, 21, 22	$-I_n$	max.	3 mA
at pins 27 and 28	I_n	max.	3 mA
Total power dissipation	P_{tot}	max.	1,4 W
Storage temperature range	T_{stg}		−25 to + 150 °C
Operating ambient temperature range	T_{amb}		0 to + 70 °C

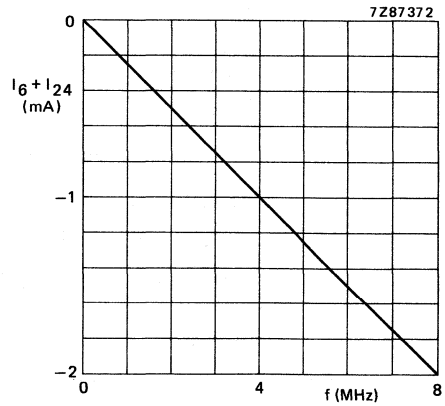


Fig. 2 Steepness of the main and drop out demodulator.

CHARACTERISTICS

$V_P = V_{7, 23-5, 25} = 10$ V; $T_{amb} = 25$ °C; measured in test circuit Fig. 3; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 7 and pin 23)					
Supply voltage	$V_P = V_{7, 23-5, 25}$	9,6	10	13,2	V
Supply current	$I_{P1} = I_7$	–	23	–	mA
	$I_{P2} = I_{23}$	–	17	–	mA
FM amplifier					
Input voltage (pin 17) (peak-to-peak value)	$V_{17-25(p-p)}$	–	100	–	mV
Input resistance	R_{17-25}	10	–	–	kΩ
Gain	G_v	–	20	–	dB
Bandwidth ($R_G \leqslant 50\ \Omega$)	B	–	12	–	MHz
Output signal amplitude (pin 16) (peak-to-peak value)	$V_{16-25(p-p)}$	–	–	1,3	V
Main limiter amplifier (pin 19)					
FM input signal (peak-to-peak value)	$V_{19-25(p-p)}$	–	0,5	1	V
Input resistance	R_{19-25}	–	600	–	Ω
Start of limiting (referred to pin 11) (peak-to-peak value)	$V_{19-25(p-p)}$	–	–	2,5	mV
Drop out limiter amplifier (pin 10)					
FM input signal (peak-to-peak value)	$V_{10-5(p-p)}$	–	–	0,8	V
Input resistance	R_{10-5}	–	1	–	kΩ
Start of limiting (referred to pin 11) (peak-to-peak value)	$V_{10-5(p-p)}$	–	–	80	mV
Main and drop out demodulators					
Range of output voltages (pin 6 and pin 24) (peak-to-peak value)	$V_{6, 24-5, 25(p-p)}$	–	–	3,5	V
Linearity (bandwidth = 1 to 6 MHz)		–5	–	+5	%
Steepness (see Fig. 2)	S	–	0,25	–	mA/MHz
FM switch (pin 11)					
Output amplitude (peak-to-peak value)	$V_{11-5(p-p)}$	–	0,5	–	V
D.C. output voltage	V_{11-5}	–	8,4	–	V

parameter	symbol	min.	typ.	max.	unit
Video switch (pin 4)					
Input voltage (pin 2 and pin 3) (peak-to-peak value)	$V_{2,\ 3\text{-}5(p\text{-}p)}$	–	–	0,5	V
Input resistance (open base)	$R_{2,\ 3\text{-}5}$	20	–	–	kΩ
Voltage gain	G_v	–	14	–	dB
D.C. output voltage at $V_{2,\ 3\text{-}5} = 9{,}5$ V	$V_{4\text{-}5}$	–	5,4	–	V
De-emphasis amplifier (linear)					
Video output signal (pin 28) (peak-to-peak value)	$V_{28\text{-}5(p\text{-}p)}$	–	–	3	V
Gain-bandwidth product	G.B.	30	–	–	MHz
D.C. output voltage	$V_{28\text{-}5}$	–	4,8	–	V
Dynamic de-emphasis					
Output signal (pin 26) (peak-to-peak value) at $V_{28\text{-}5(p\text{-}p)} = 1$ V; f = 1 MHz sine	$V_{26\text{-}5(p\text{-}p)}$	–	632	–	mV
D.C. output voltage	$V_{26\text{-}5}$	–	3,4	–	V
Output current (emitter follower)	$-I_{26}$	–	–	5	mA
Drop out detector and Schmitt-trigger					
Input voltage for lower drop out threshold (pin 15) (peak-to-peak value)	$V_{15\text{-}5(p\text{-}p)}$	–	110	–	mV
Hysteresis of the Schmitt-trigger	V/V	–	1,5	–	dB
Input resistance	$R_{15\text{-}5}$	1,4	–	–	kΩ
D.C. output voltage without drop out	$V_{12\text{-}5}$	–	–	2	V
D.C. output voltage with drop out	$V_{12\text{-}5}$	5	–	–	V
OR-gate (internal)					
Switching voltage threshold (pin 12) for signal flow from pin 2 to pin 4	$V_{12\text{-}5}$	–	–	1,5	V
for signal flow from pin 3 to pin 4	$V_{12\text{-}5}$	3	–	–	V

APPLICATION INFORMATION

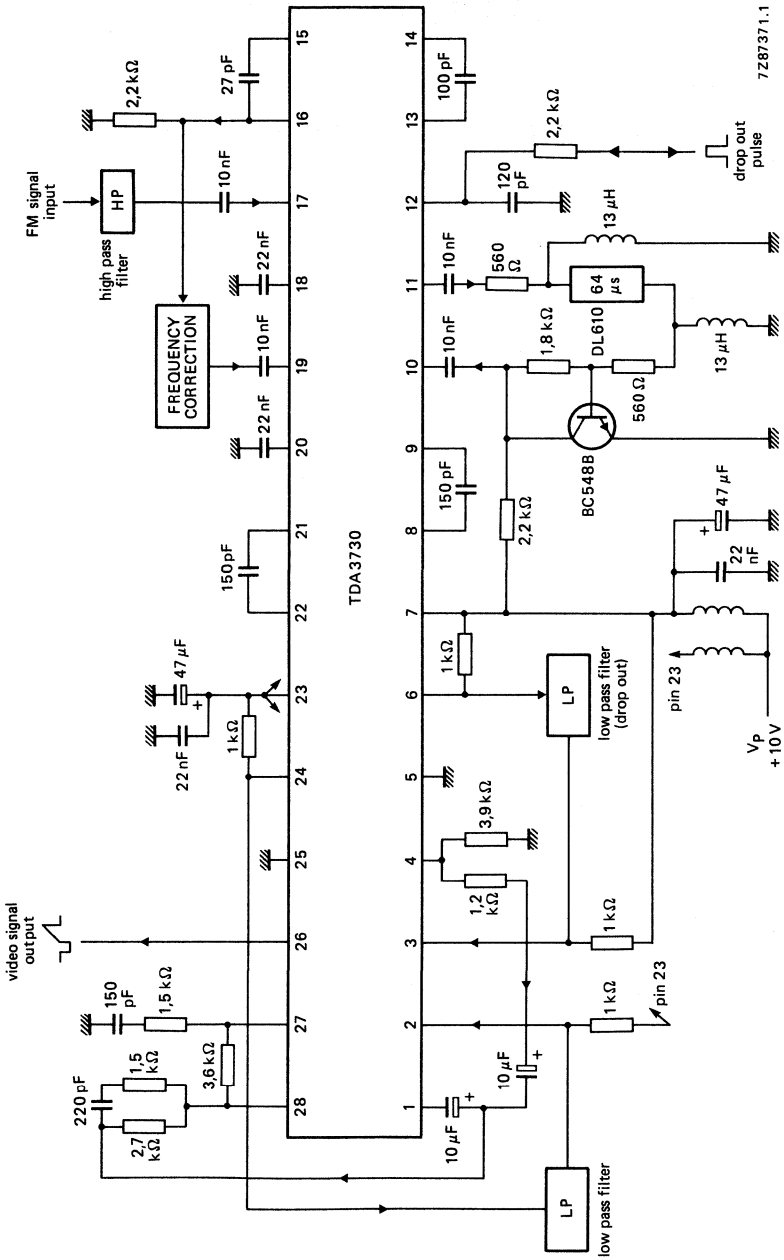


Fig. 3 Application diagram; also used as test circuit.

VIDEO PROCESSOR AND FREQUENCY MODULATOR FOR VIDEO RECORDERS

GENERAL DESCRIPTION

The TDA3740 is a monolithic integrated circuit for video signal processing and frequency modulation in video recorders.

Features

- Video controlled amplifier with clamping stage
- Fast and slow white amplitude detector
- Sync amplitude detector
- Black and white clip
- Insertion of sync and composite video signals
- Adder stage for composite video and chrominance signals
- Two-stage amplification for the composite video signal with dynamic (adjustable) and linear pre-emphasis
- White clip with external determination of clipping level
- Voltage controlled oscillator (frequency modulator)
- Blanking stage for the voltage controlled oscillator and limiter amplifier
- Reference voltage source

QUICK REFERENCE DATA

Supply voltage (pin 18, 28)	$V_P = V_{18,28-27}$	typ.	10 V
Supply current (pin 18, 28) (record mode)	$I_P = I_{18,28}$	typ.	58 mA
Supply current (pin 18) (playback mode)	$I_P = I_{18}$	typ.	28 mA
Composite video input signal (peak-to-peak value)	$V_{3-27(p-p)}$	typ.	350 mV
Composite colour video output signal (peak-to-peak value)	$V_{7-27(p-p)}$	typ.	2 V
Chrominance input signal (peak-to-peak value)	$V_{9-27(p-p)}$	typ.	240 mV
Output current (pin 22, 23)	$I_{22,23}$	typ.	8,5 mA

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

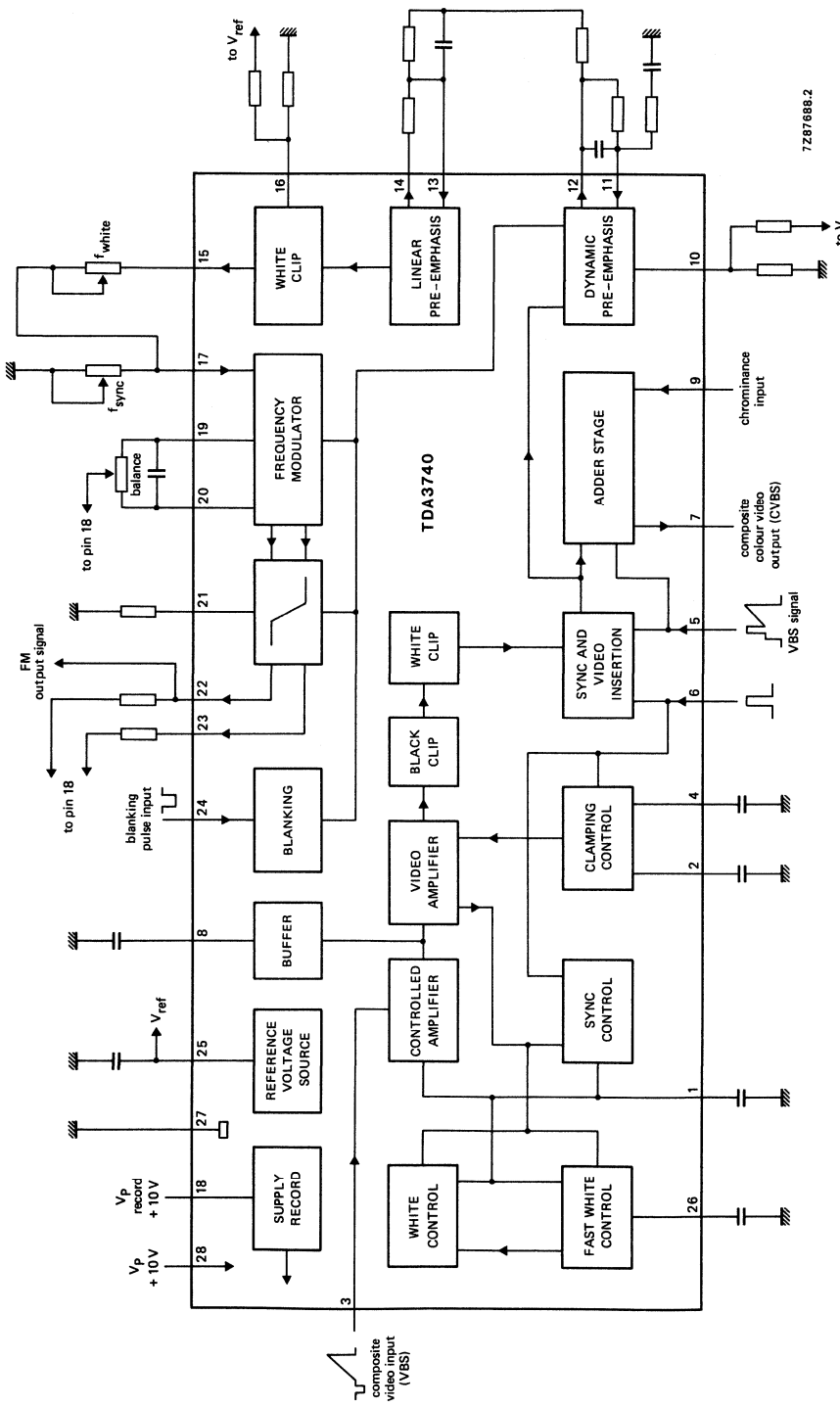


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 18, 28)	$V_P = V_{18,\,28\text{-}27}$	max.	13,2	V

With pin 27 connected to ground and pin 18 and 28 to supply voltage (V_P) all voltages between 0 and V_P are allowed.

Total power dissipation	P_{tot}	max.	1,4	W
Storage temperature range	T_{stg}		−25 to +150	°C
Operating ambient temperature range	T_{amb}		0 to +70	°C

CHARACTERISTICS

$V_P = V_{18\text{-}28} = 10$ V; $T_{amb} = 25$ °C; measured in test circuit Fig. 2; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 18, 28)					
Supply voltage	$V_P = V_{18,\,28\text{-}27}$	9	10	13,2	V
Supply current					
at record (FM kill inactive)	$I_P = I_{18,\,28}$	–	58	–	mA
at playback	$I_P = I_{28}$	–	28	–	mA
Controlled amplifier					
Composite video input signal (peak-to-peak value)	$V_{3\text{-}27(p\text{-}p)}$	0,20	0,35	0,62	V
Video signal control range (referred to 0,35 V input signal at pin 3)	$\alpha_{3\text{-}27}$	±5	±6	–	dB
Input resistance	$R_{3\text{-}27}$	7	10	13	kΩ
Input capacitance	$C_{3\text{-}27}$	–	–	10	pF
Composite colour video output signal (peak-to-peak value)	$V_{7\text{-}27(p\text{-}p)}$	1,9	2	2,1	V
Frequency response (0 to 3 MHz)	$\alpha_{7\text{-}3}$	−0,5	–	0,5	dB
Sync recovering and insertion of composite video signal					
Threshold voltage for sync recovering	$V_{6\text{-}27}$	3,0	3,5	4,0	V
Input resistance	$R_{6\text{-}27}$	100	–	–	kΩ

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Insertion of composite video signal					
insertion inactive	V_{5-27}	0	–	0,9	V
video + chroma mute	V_{5-27}	2,5	–	3,0	V
insertion black level	V_{5-27}	3,1	3,25	3,4	V
insertion white level (90% CVBS)	V_{5-27}	3,7	4,0	4,3	V
Input resistance	V_{5-27}	100	–	–	kΩ
Gain	G_{7-5}	2,9	4,5	6,5	dB
Frequency response (0 to 5 MHz)	α_{7-5}	–	–	3	dB
Signal suppression pin 7 at mute		−40	–	–	dB
Clamping control					
Duration of clamping pulse (note 1) with C_{2-27} = 100 nF; C_{4-27} = 2,2 nF	t_d	1	3	4,5	μs
Max. leakage current of external capacitor	I_{L2}	–	–	1	μA
Black and white clip					
Black clip relative to black level	ΔV_{7-27}	−40	−25	0	mV
White clip at pin 7 (referred to nominal VBS)		103	105	107	%
Chrominance signal adder and output stage					
Burst input signal (peak-to-peak value)	$V_{9-27(p-p)}$	–	240	400	mV
Input resistance	R_{9-27}	4	5,6	–	kΩ
D.C. level of top sync	V_{7-27}	2,4	2,7	3,0	V
Sync amplitude at CVBS output pin 7	$V_{7-27(p-p)}$	570	600	630	mV
Gain (f = 4,43 MHz)	G_{7-9}	7	8	9	dB
Output resistance	R_{7-27}	–	–	30	Ω
Frequency response (0 to 5 MHz)	α_{7-9}	−0,5	–	+0,5	dB
Dynamic and linear pre-emphasis; white limiter					
Input resistance pin 11	R_{11-27}	15	–	–	kΩ
Output resistance (emitter follower with internal current source)	R_{12-27}	–	–	30	Ω
Gain-bandwidth product					
dynamic (V_{24-27} = Vp)		24	36	–	MHz
linear		30	–	–	MHz

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Range of dynamic pre-emphasis (fixed by external resistors at pin 10)	$V_{10\text{-}27}$	0	–	2,5	V
Gain adjustment range at 1 MHz and $V_{7\text{-}27}$ = 632 mV	$G_{12\text{-}7}$	1,5	–	8	dB
Output resistance (emitter follower with internal current source)	$R_{14\text{-}27}$	–	–	30	Ω
White clip level deviation relative to $V_{16\text{-}27}$ = 1,5 V	$V_{16\text{-}15}$	75	–	125	mV
Range of clipping determination (note 2)	$V_{16\text{-}27}$	1	–	3	V
Frequency modulator					
D.C. level at pin 21 (note 3)	$V_{21\text{-}27}$	1,8	1,9	2,0	V
FM output voltage (note 3) $R_{21\text{-}27}$ = 1,5 kΩ, $R_{22,\ 23\text{-}18}$ = 470 Ω	$V_{22,\ 23\text{-}27}$	–	660	–	mV
Slope between 3 MHz and 6 MHz	$\frac{\Delta f_{22,23}}{\Delta I_{17}}$	–	10,5	–	$\frac{KHz}{\mu A}$
Linearity between 3 MHz and 6 MHz	m	95	–	–	%
Suppression of the 2nd harmonic referred to the 1st harmonic 3,8 MHz (balanced)	α_{harm}	40	46	–	dB
Frequency drift dependent on: drift of supply voltage (V_P = 9 – 13,2 V)	$\frac{\Delta f_{22,23}}{\Delta V_P}$	–	5	10	$\frac{KHz}{V}$
drift of ambient temperature (T_{amb} = 0 – 70 °C) at 3,8 MHz	$\Delta f_{22,23}$	–85	–	+85	kHz
at 4,8 MHz	$\Delta f_{22,23}$	–85	–	+85	kHz
Drift of frequency span dependent on temperature drift (T_{amb} = 0 – 70 °C)	Δf	–70	–	+70	kHz
Input voltage to switch FM off	$V_{24\text{-}27}$	–	–	2	V
Input voltage to switch FM on	$V_{24\text{-}27}$	3	–	–	V
Input resistance	$R_{24\text{-}27}$	10	–	–	kΩ

parameter	symbol	min.	typ.	max.	unit
Reference voltage source (pin 25)					
Output voltage	$V_{25\text{-}27}$	–	5,5	–	V
Output current (additional to application)	I_{25}	−3	–	+5	mA
Output voltage drift dependent on drift of supply voltage (V_P = 9 – 13,2 V)	$\frac{\Delta V_{25\text{-}27}}{\Delta V_P}$	−10	–	+10	$\frac{mV}{V}$
drift of ambient temperature (T_{amb} = 0 – 70 °C)	$\Delta V_{25\text{-}27}$	−90	–	+90	mV

Notes

1. Duration of clamping pulse is determined by $C_{4\text{-}27}$ as follows: t_d (μs) = 1,364 . $C_{4\text{-}27}$ (nF).
2. White clipping level is fixed by the external resistors at pin 16, e.g. $R_{16\text{-}25}$ = 3,3 kΩ and $R_{16\text{-}27}$ = 2 kΩ results in 160% clipping level.
3. FM output amplitude at pins 22 and 23 is determined by the external fixed resistors $R_{21\text{-}27}$, $R_{22\text{-}18}$ and $R_{23\text{-}18}$.

DEVELOPMENT DATA

APPLICATION INFORMATION

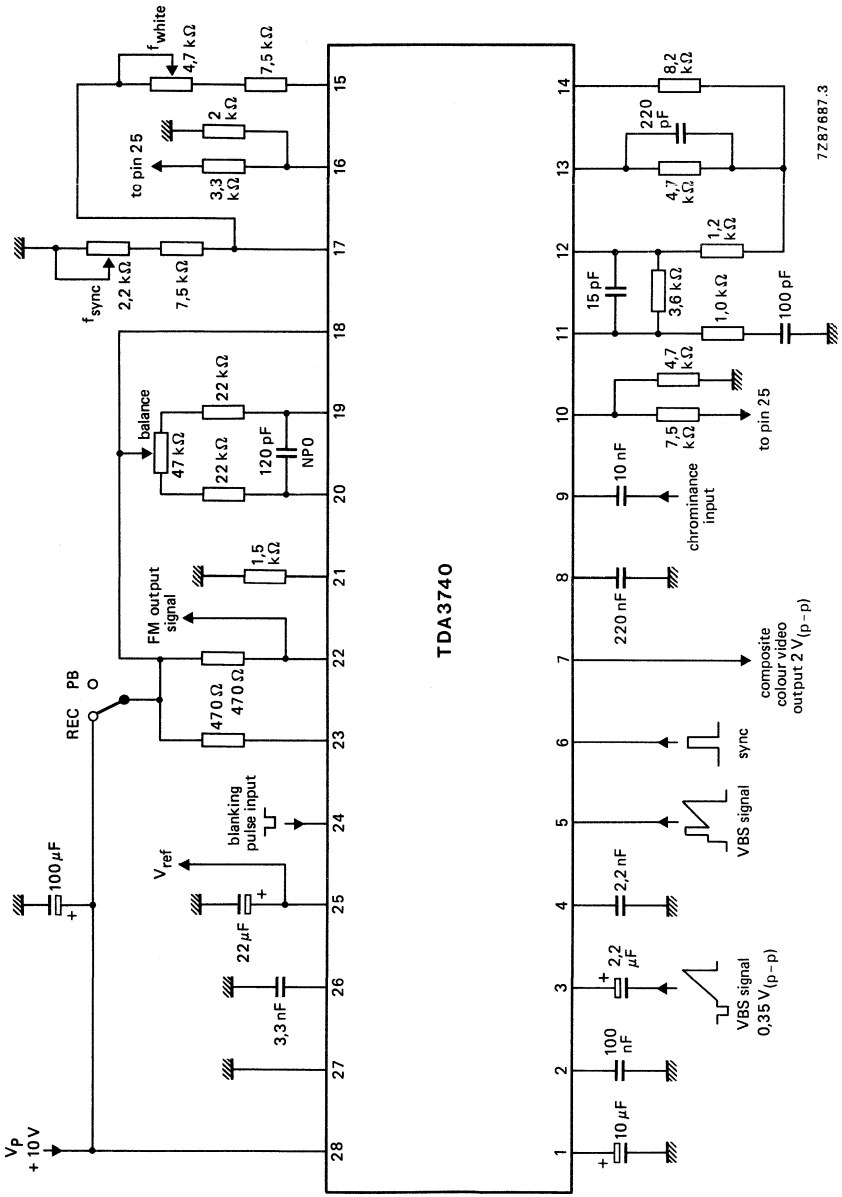


Fig. 2 Application diagram; also used as test circuit.

REC = record.
PB = playback.

PAL/NTSC/SECAM SYNCHRONIZATION PROCESSOR FOR VIDEO RECORDERS

GENERAL DESCRIPTION

The TDA3755 is a monolithic integrated circuit for PAL/NTSC SECAM synchronization processing in VHS video recorders.

Features

- Adaptive sync separator
- Internal vertical sync pulse integrator
- Composite sync and vertical pulse output
- Current controlled oscillator (CCO) with 320/321 times horizontal frequency
- Horizontal phase detector with current output
- Video identification and mute circuit
- Burst gating pulse output (externally adjustable phase relationship)
- Test-picture output
- Subcarrier frequency output switched in phase in accordance with VHS standard
- Fast phase correction of subcarrier frequency
- Selection input to force PAL or NTSC function
- Still picture input

QUICK REFERENCE DATA

Supply voltage (pin 13)	$V_P = V_{13-15}$	typ.	10 V
Supply current (pin 13)	$I_P = I_{13}$	typ.	24 mA
Sync separator			
Sync pulse input voltage (peak-to-peak value)	$V_{3-15(p-p)}$	typ.	300 mV
Sync pulse output voltage (peak-to-peak value)	$V_{1-15(p-p)}$	min.	7,3 V
Vertical sync pulse			
Output voltage (peak-to-peak value)	$V_{18-15(p-p)}$	min.	2,7 V
Phase detector			
Catching range	Δf	min.	± 3,0 %
Oscillator			
Oscillator frequency			
PAL	f_{osc}	typ.	5,02 MHz
NTSC	f_{osc}	typ.	5,04 MHz
Output frequency			
PAL	f_o	typ.	627 kHz
NTSC	f_o	typ.	629 kHz
Output sinewave (peak-to-peak value)	$V_{8-15(p-p)}$	typ.	3 V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

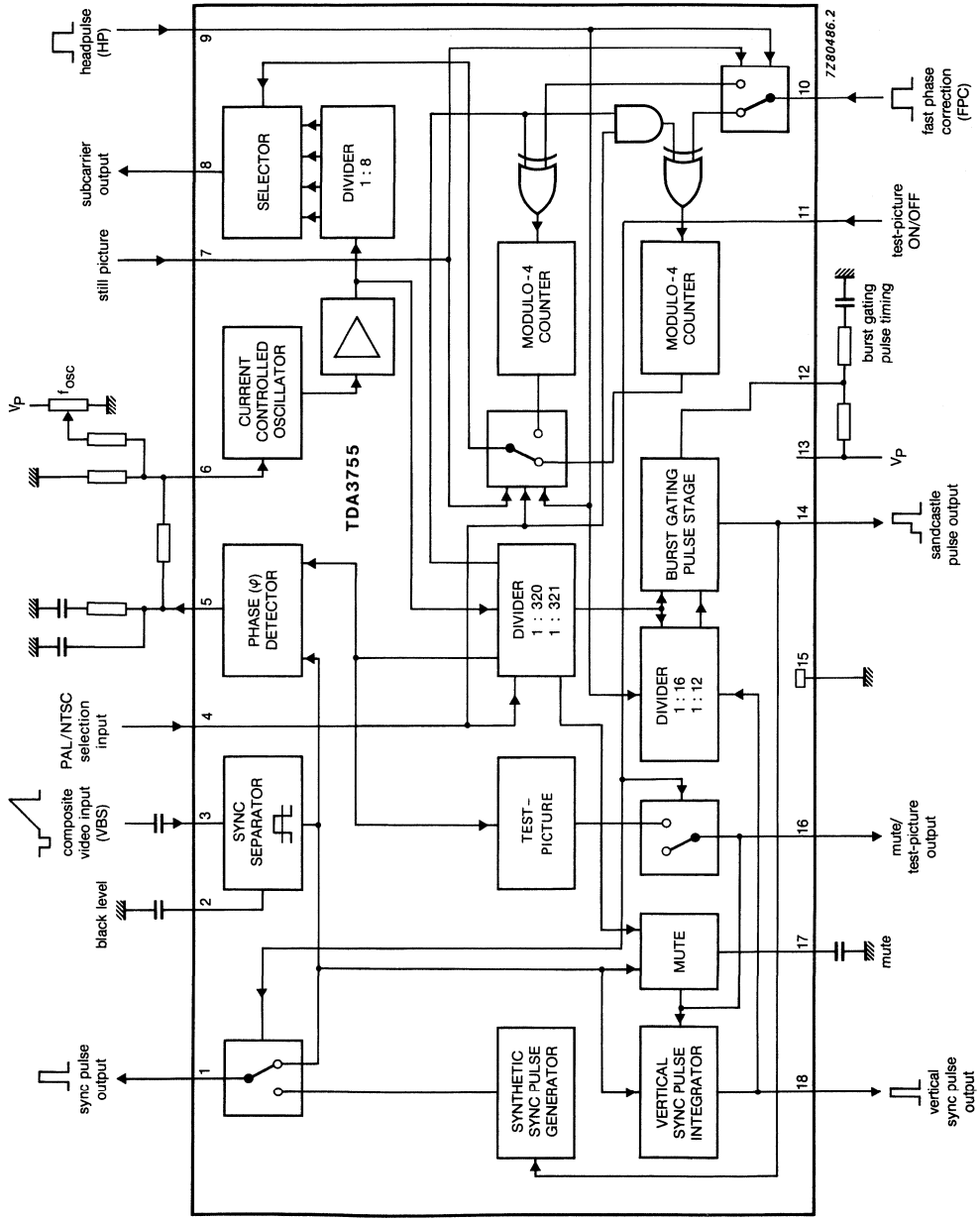


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 13)	$V_P = V_{13-15}$	max.	13,2 V
Voltage range at pins 2, 3, 4, 7, 9, 10, 11, 17 to pin 15 (ground)	V_{n-15}		0 to V_P V
Voltage range at pin 12	V_{12-15}	min.	0 V
Voltage range at pin 6	V_{6-15}	max.	8 V
Currents			
at pins 1, 5, 8, 14, 16, 18	$\pm I_n$	max.	5 mA
at pin 6	$-I_6$	max.	1 mA
at pin 12	I_{12}	max.	2 mA
Total power dissipation	P_{tot}	max.	1 W
Storage temperature range	T_{stg}		−25 to + 150 °C
Operating ambient temperature range	T_{amb}		0 to + 70 °C

CHARACTERISTICS

V_P = 10 V; T_{amb} = 25 °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 13)					
Supply voltage range	$V_P = V_{13-15}$	9,6	–	13,2	V
Supply current	$I_P = I_{13}$	–	24	–	mA
Sync separator (pin 3)					
Colour composite video input voltage (note 1) (peak-to-peak value)	$V_{3-15(p-p)}$	–	1	–	V
Sync pulse amplitude (peak-to-peak value)	$V_{3-15(p-p)}$	75	–	600	mV
Slicing level, relative to sync pulse amplitude (note 2)		–	50	–	%
Internal resistance of video source	R_G	–	–	1	kΩ
Sync output voltage HIGH at $-I_1$ = 1 mA	V_{1-15}	7,8	–	–	V
Sync output voltage LOW at I_1 = 1 mA	V_{1-15}	–	–	0,5	V
Delay between signal at input pin 3 and sync pulse at output pin 1	t_d	–	0,2	–	μs
Vertical sync pulse (pin 18; note 3)					
Output voltage HIGH at $-I_{18}$ = 1 mA	V_{18-15}	2,7	–	5,0	V
Output voltage LOW at I_{18} = 1,6 mA	V_{18-15}	–	–	0,5	V
Duration of HIGH state of internally generated output pulse	t_p	–	190	–	μs
Delay between leading edge of input signal at pin 3 and leading edge of output pulse at pin 18	t_d	32	–	64	μs
Selection input (pin 4)					
Input voltage for NTSC state	V_{4-15}	–	–	0,3	V
Input current at V_{4-15} = 0 V	$-I_4$	–	–	20	μA
Input voltage for PAL state pin 4 open circuit or	V_{4-15}	2	–	–	V

parameter	symbol	min.	typ.	max.	unit
Test picture/mute/synthetic sync pulse					
Minimum voltage at pin 11 for test picture mode **active** (note 4)	$V_{11\text{-}15}$	4,8	–	–	V
Maximum voltage at pin 11 for test picture mode **inactive**	$V_{11\text{-}15}$	–	–	3,8	V
Output voltage at pin 16					
at test picture "black" or at mute	$V_{16\text{-}15}$	–	2,75	–	V
at test picture "white"	$V_{16\text{-}15}$	–	4,50	–	V
at "in sync condition"	$V_{16\text{-}15}$	–	–	0,5	V
Input current (pin 11)	$-I_{11}$	–	–	25	μA
Oscillator/phase detector					
Oscillator frequency (note 5)					
PAL	f_{osc}	–	5,02	–	MHz
NTSC	f_{osc}	–	5,04	–	MHz
Oscillator conversion gain	k_o	–	16,13	–	MHz/mA
D.C. control voltage	$V_{6\text{-}15}$	–	2,1	–	V
Input current for f = 5,016 MHz	$-I_{16}$	–	310	–	μA
Holding range (note 6)	Δf	± 3,2	–	–	%
Catching range (note 6)	Δf	± 3,0	–	–	%
Control loop gain	k_v	–	380×10^3	–	s^{-1}
Output of lower subcarrier (note 7) (peak-to-peak value)	$V_{8\text{-}15(p\text{-}p)}$	–	3	–	V
Output current	I_8	–	–	2	mA
D.C. output voltage	$V_{8\text{-}15}$	–	3,1	–	V
2nd harmonic suppression without switching	α_{2nd}	20	–	–	dB
Switching position prior to centre of sync pulse (pin 3)	t_s	–	2	–	μs
Output peak current of phase detector during sync pulse	$\pm I_5$	–	3,78	–	mA
Output voltage range (note 8)	$V_{5\text{-}15}$	1,4	–	2,8	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Sandcastle pulse (pin 14; note 9)					
Output voltage HIGH (note 10) at $-I_{14}$ = 1 mA	V_{14-15}	7,8	–	–	V
Output voltage INTERMEDIATE at $-I_{14}$ = 1 mA	V_{14-15}	2,3	3,0	3,7	V
Output voltage LOW at I_{14} = 1 mA	V_{14-15}	–	–	0,5	V
Lower part is starting prior to the centre of sync pulse at pin 3 and ending with the upper part	t_{14-3}	–	2,6	–	μs
Fast phase correction/head pulse					
Threshold voltage for fast phase correction (note 11)	V_{10-15}	–	7,2	–	V
Input current	$-I_{10}$	–	–	20	μA
Threshold voltage of head pulse input	V_{9-15}	–	1,4	–	V
Input current	$-I_9$	–	–	20	μA
D.C. input voltage	V_{7-15}	–	5,6	–	V
Input resistance	R_{7-15}	3	–	–	kΩ
Subcarrier phase switching (note 12)					
Phase switching of subcarrier phase in accordance with head pulse if	V_{7-15}	–	5,6*	–	V
LOW state of still picture input	V_{7-15}	–	–	0,5	V
Continuous phase switching regardless of head pulse if	V_{7-15}	–	V_P	–	V

* Or not connected.

Notes to characteristics

1. The sync separator input signal is shown in Fig. 2.

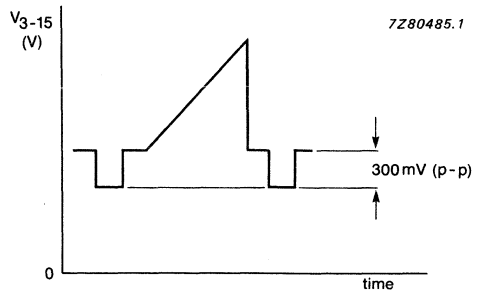
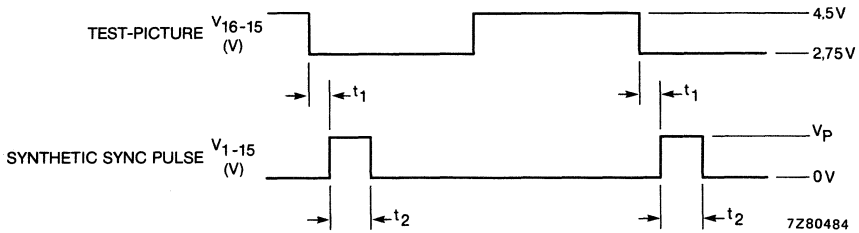


Fig. 2 Colour composite video input signal at pin 3.

2. The black level and the top sync level are detected internally and stored in capacitors at pin 2 and pin 3 respectively.
3. The vertical sync pulse output is disabled by mute.
4. In test picture mode the synthetic sync pulse is fed to output pin 1 and the vertical pulse consists of an uninterrupted block pulse of 192 μs triggering at every transition of head pulse (HP) at pin 9. The timing of test picture and synthetic sync pulse is shown in Fig. 3.



Where: The value of t_1 is dependent upon adjustment of the burst gating pulse delay.
Time t_2 is the burst gating pulse duration.

Fig. 3 Timing of test picture and synthetic sync pulse.

5. Oscillator adjustment during test picture mode made only, at $V_{11-15} > 4{,}8$ V, $V_{7-15} = 0$ V and $V_{4-15} > 2$ V or open circuit; measurement is $f_{osc}/8$ at output pin 8.
6. The holding range and catching range are both determined by the resistor connected between pin 5 and pin 6.
7. The phase of the lower subcarrier is switched in accordance with the VHS standard. PNP emitter follower, internal resistive load of 10 kΩ (typ.) to V_P.
8. The output voltage at pin 5 is disabled during test picture mode.

Notes to characteristics (continued)

9. The burst gating pulse is superimposed on an uninterrupted horizontal pulse. It is suppressed 16 times starting with every transition of the head pulse at pin 9. If a vertical pulse is detected during that time the burst gating pulses are additionally suppressed until line 12 and line 324 respectively. In any event the number of suppressed burst gating pulses is even.
10. The timing of the upper part of the sandcastle pulse is determined by the components connected to pin 12 (Fig. 4) and is independent of supply voltage variations.
11. The fast phase correction pulses have to be in the burst gating reference pulse. For any HIGH to LOW transitions of the correction pulse the phase is corrected by -90^o if the head pulse input is LOW and by $+90^o$ if the head pulse input is HIGH.
12. Subcarrier phase switching is detailed in Table 1.
    Subcarrier is 40,000 x f_H for NTSC state and 40,125 x f_H for PAL state.

Table 1 Subcarrier phase switching

still picture input	PAL		NTSC	
	HP = HIGH	HP = LOW	HP = HIGH	HP = LOW
HIGH	-90^o	-90^o	-90^o	-90^o
not connected	0^o	-90^o	$+90^o$	-90^o
LOW	0^o	0^o	$+90^o$	$+90^o$

APPLICATION INFORMATION

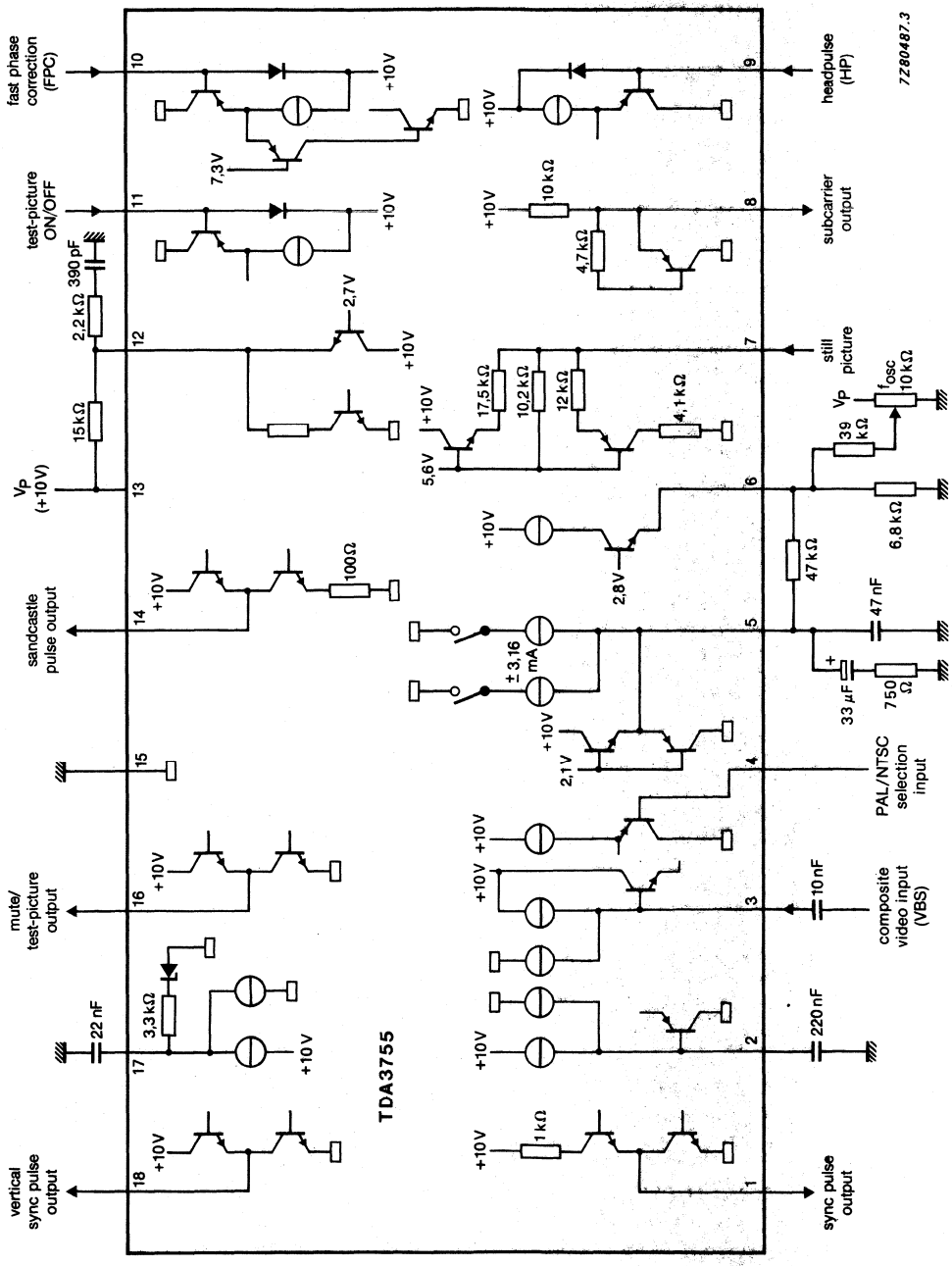


Fig. 4 Application circuit diagram.

PAL CHROMINANCE SIGNAL PROCESSOR FOR VIDEO RECORDERS

GENERAL DESCRIPTION

The TDA3760 is a monolithic integrated circuit for chrominance signal processing in video recorders.

Features

- Automatic gain controlled pre-amplifier with record/playback selection
- Signal mixer with balancing stage
- Output stage for the 627 kHz chrominance signal, with facility for being disabled by colour killer and record/playback mode switch
- Amplitude detector with automatic gain control for the preamplifier
- 4,43 MHz voltage controlled oscillator (VCO) for recording and playback
- 4,43 MHz fixed oscillator for playback
- Phase detector controlled synchronization of the VCO
- Subcarrier mixer
- H/2 demodulator for the production of PAL identification and colour killing signals
- Flip-flop for PAL identification
- Sandcastle pulse processing
- Colour killing stage with hysteresis
- Internal record/playback selection
- Second phase detector for fast phase correction of sub-carrier

QUICK REFERENCE DATA

Supply voltage (pin 9)	$V_P = V_{9\text{-}15}$	typ.	10 V
Supply current (pin 9)	$I_P = I_9$	typ.	45 mA
Inputs			
Chrominance signal			
4,43 MHz for record (peak-to-peak value)	$V_{2\text{-}15(p\text{-}p)}$	typ.	200 mV
627 kHz for playback (peak-to-peak value)	$V_{1\text{-}15(p\text{-}p)}$	typ.	200 mV
Outputs			
Chrominance signal			
4,43 MHz (peak-to-peak value)	$V_{24\text{-}15(p\text{-}p)}$	typ.	490 mV
627 kHz (peak-to-peak value)	$V_{26\text{-}15(p\text{-}p)}$	typ.	2 V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

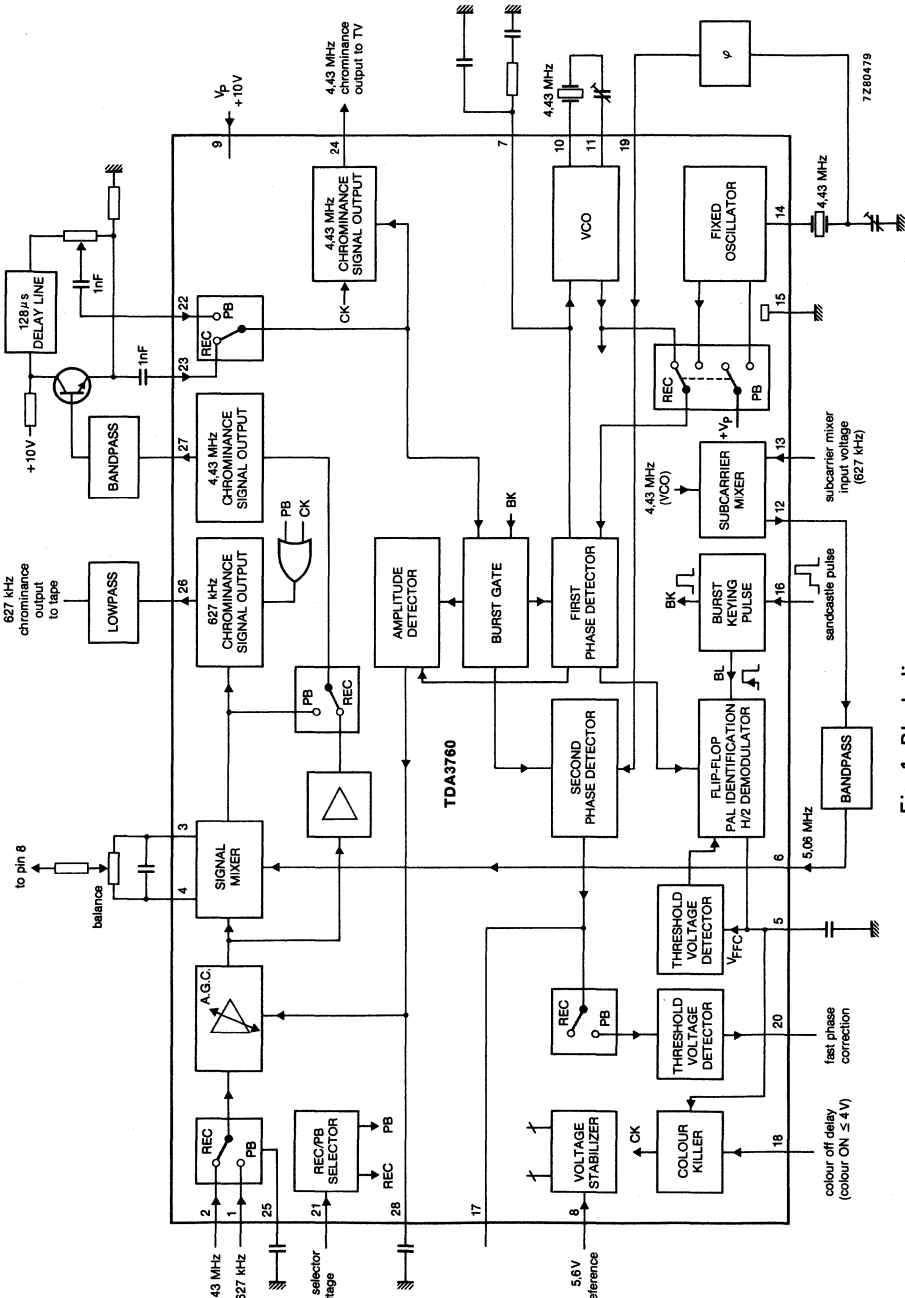


Fig. 1 Block diagram.

BK = burst key pulse
BL = blanking pulse
FFC = flip-flop correction
FPC = fast phase correction

REC = record
PB = playback
CK = colour killer

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 9)	$V_P = V_{9\text{-}15}$	max.	13,2	V
Voltage range at pins 1, 2, 5, 7, 8, 9, 16, 17, 18, 19, 20, 21, 22, 23 to pin 15 (ground)	$V_{n\text{-}15}$		0 to V_P	V
Voltage ranges				
at pins 3, 4, 28*	$V_{3,\ 4,\ 28\text{-}15}$		3 to 6	V
at pin 6, 25*	$V_{6,\ 25\text{-}15}$		0 to 5	V
at pin 10*	$V_{10\text{-}15}$		1,5 to 4	V
at pin 13*	$V_{13\text{-}15}$		0 to 3	V
at pin 14*	$V_{14\text{-}15}$		0 to 8	V
Voltages				
at pin 12	$V_{12\text{-}15}$	max.	V_P	V
at pin 24	$V_{24\text{-}15}$	max.	7	V
Currents				
at pins 11, 18	$-I_{11,\ 18}$	max.	2	mA
at pins 12, 26, 27	$-I_{12,\ 26,\ 27}$	max.	5	mA
at pin 24	$-I_{24}$	max.	3	mA
Total power dissipation	P_{tot}	max.	1,4	W
Storage temperature range	T_{stg}		−25 to +150	°C
Operating ambient temperature range	T_{amb}		0 to +70	°C

* Measured with $V_{8\text{-}15} = 5{,}6$ V

CHARACTERISTICS

$V_P = V_{9-15} = 10$ V; $V_{8-15} = 5{,}6$ V; $T_{amb} = 25\ ^oC$; burst key duration 4 μs; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 9)					
Supply voltage	$V_P = V_{9-15}$	9,6	–	13,2	V
Supply current for playback and burst keying					
at $-I_{12, 18, 24, 26, 27} = 0$	$I_P = I_9$	–	45	–	mA
at $-I_{12, 18, 24, 26, 27} = 0$; $V_P = 12$ V	$I_P = I_9$	–	46	–	mA
A.G.C. preamplifier (pins 1 and 2)					
Input voltage* (f = 4,43 MHz) during record (peak-to-peak value)	$V_{2-15(p-p)}$	20	–	400	mV
Input voltage* (f = 627 kHz) during playback (peak-to-peak value)	$V_{1-15(p-p)}$	30	–	400	mV
Input resistance	$R_{1, 2-15}$	7	–	–	kΩ
Input capacitance	$C_{1, 2-15}$	–	–	5	pF
627 kHz chrominance signal (pin 26)* (transposed on to 627 kHz signal)					
Output voltage (peak-to-peak value)	$V_{26-15(p-p)}$	–	2	–	V
Signal suppression at output					
for f = 1,25 MHz	α_{26}	–	35	–	dB
for f = 5,06 MHz (externally balanced via pins 3 and 4)	α_{26}	–	40	–	dB
during colour killing (pin 25)	α_{26}	40	–	–	dB
D.C. output voltage	V_{26-15}	–	6,7	–	V
4,43 MHz chrominance signal (pin 27)*					
Output voltage during record (peak-to-peak value)	$V_{27-15(p-p)}$	–	1,15	–	V
during playback after signal mixing (peak-to-peak value)	$V_{27-15(p-p)}$	–	–	3,1	V
Signal suppression at output					
for f = 5,06 MHz (externally balanced)	α_{27}	–	40	–	dB
for f = 8,86 MHz	α_{27}	–	30	–	dB
for f = 3,81 MHz	α_{27}	–	38	–	dB
for f = 3,18 MHz	α_{27}	–	30	–	dB
D.C. output voltage	V_{27-15}	–	7	–	V

* The chrominance signal values hold for a 75% saturated colour bar signal.

parameter	signal	min.	typ.	max.	unit
4,43 MHz chrominance signal amplifier*					
Burst input signal					
at pin 22 (peak-to-peak value)	$V_{22\text{-}15(p\text{-}p)}$	–	225	–	mV
at pin 23 (peak-to-peak value)	$V_{23\text{-}15(p\text{-}p)}$	–	225	–	mV
Input resistance					
at pin 22	$R_{22\text{-}15}$	6	–	–	kΩ
at pin 23	$R_{23\text{-}15}$	6	–	–	kΩ
Output voltage of the chrominance signal					
at pin 24 (peak-to-peak value)	$V_{24\text{-}15(p\text{-}p)}$	–	490	–	mV
Signal suppression at output (pin 24)					
during colour killing	α_{24}	35	–	–	dB
D.C. output voltage					
during colour-on	$V_{24\text{-}15}$	–	2,4	–	V
during colour-off (killed)	$V_{24\text{-}15}$	–	0,7	–	V
Subcarrier mixer					
627 kHz input voltage; sine-wave (peak-to-peak value)	$V_{13\text{-}15(p\text{-}p)}$	220	–	–	mV
Input resistance	$R_{13\text{-}15}$	1	–	–	kΩ
D.C. output voltage	$V_{12\text{-}15}$	–	7,9	–	V
5,06 MHz output voltage selective** (peak-to-peak value)	$V_{12\text{-}15(p\text{-}p)}$	–	800	–	mV
Signal suppression at output**					
for f = 4,43 MHz	α_{12}	20	–	–	dB
for f = 5,68 MHz	α_{12}	30	–	–	dB
Subcarrier input					
5,06 MHz input voltage (peak-to-peak value)	$V_{6\text{-}15(p\text{-}p)}$	250	–	–	mV
Input resistance	$R_{6\text{-}15}$	1,9	–	–	kΩ
Input capacitance	$C_{6\text{-}15}$	–	–	5	pF

* Chrominance signal values hold for a 75% saturated colour bar signal.

** Measured with a 0,32 V (peak-to-peak), 627 kHz input signal on pin 13 ($-I_{12}$ = 1 mA).

CHARACTERISTICS (continued)

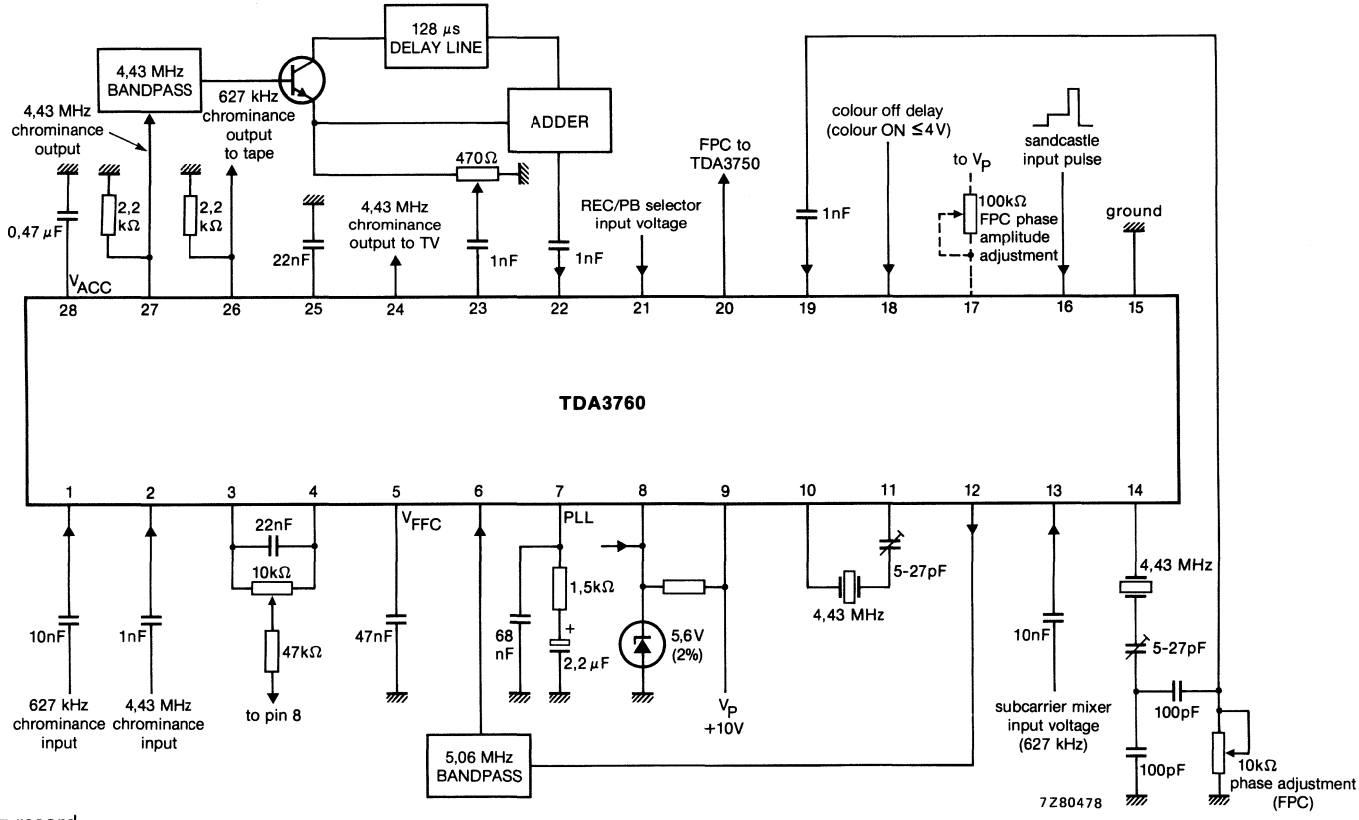
parameter	symbol	min.	typ.	max.	unit
4,43 MHz voltage controlled oscillator (VCO)					
Input resistance	$R_{10\text{-}15}$	–	430	–	Ω
Input capacitance	$C_{10\text{-}15}$	–	–	10	pF
Output resistance	$R_{11\text{-}15}$	–	–	200	Ω
PLL-controlled oscillator catching range	Δf	± 500	–	–	Hz
Phase difference between oscillator and burst signal for ± 400 Hz deviation of crystal frequency	φ	± 7	–	–	deg
4,43 MHz fixed oscillator					
Oscillator temperature coefficient*	TC	–	–	–3	Hz/K
Record/playback selector (pin 21)					
Input voltage for record**	$V_{21\text{-}15}$	–	–	4	V
Input current with $V_{21\text{-}15}$ = 4 V	I_{21}	–	–	130	μA
Input voltage for playback	$V_{21\text{-}15}$	8	–	–	V
Input current with $V_{21\text{-}15}$ = 8 V	I_{21}	–	–	430	μA
Input resistance	$R_{21\text{-}15}$	7	–	–	kΩ
Colour (on/off) killer delay					
Delay for chrominance signal OFF at ΔV = 1 V; C = 1 μF; PNP emitter follower with internal current of 0,1 mA	t_d	–	10	–	ms
Input voltage (pin 18)					
for forced colour ON	$V_{18\text{-}15}$	–	–	4	V
for forced colour OFF	$V_{18\text{-}15}$	5,5	–	9	V
Voltage stabilizer (pin 8)					
Range of external reference voltage	$V_{8\text{-}15}$	5,3	–	5,8	V
Input current	$-I_8$	–	–	120	μA

* Not considering the effects of external components.
** Pin open: record.

parameter	symbol	min.	typ.	max.	unit
Sandcastle pulse input (pin 16)					
Input voltage for burst keying	$V_{16\text{-}15}$	7,1	–	–	V
Input current	I_{16}	–	–	5	μA
Delay time of BK	t_d	–	0,55	–	μs
Input voltage for triggering of flip-flop	$V_{16\text{-}15}$	2	–	–	V
Fast phase correction					
Input voltage* (peak-to-peak value)	$V_{19\text{-}15(p\text{-}p)}$	200	–	400	mV
Input resistance	$R_{19\text{-}15}$	3,3	–	–	kΩ
Output voltage					
without correction below phase differences of ± 50° at $I_{20} < \pm 20$ μA and $V_{17\text{-}15} < 6{,}5$ V	$V_{20\text{-}15}$	–	–	5,2	V
with correction above phase differences of ± 65° at $I_{20} < \pm$ 20 μA and $V_{17\text{-}15} > 7{,}1$ V	$V_{20\text{-}15}$	9	–	–	V
Output resistance	$R_{20\text{-}15}$	–	35	–	kΩ

* Phase difference between output pin 14 and input pin 19 should be $\varphi = 90°$.

APPLICATION INFORMATION



REC = record
PB = playback
FPC = fast phase correction
FFC = flip-flop correction

Fig. 2 Application diagram.

NTSC CHROMINANCE SIGNAL PROCESSOR FOR VIDEO RECORDERS

GENERAL DESCRIPTION

The TDA3765 is a monolithic integrated circuit for chrominance signal processing in video recorders.

Features

- Automatic gain controlled pre-amplifier with record/playback selection
- Signal mixer with balancing stage
- Output stage for the 629 kHz chrominance signal, with facility for being disabled by colour killer and record/playback mode switch
- Amplitude detector with automatic gain control for the preamplifier
- 3,58 MHz voltage controlled oscillator (VCO) for recording and playback
- 3,58 MHz fixed oscillator for playback
- Phase detector controlled synchronization of the VCO
- Subcarrier mixer
- Sandcastle pulse processing
- Colour killing stage with hysteresis
- Internal record/playback selection
- Second phase detector for fast phase correction of sub-carrier

QUICK REFERENCE DATA

Supply voltage (pin 9)	$V_P = V_{9\text{-}15}$	typ.	10 V
Supply current (pin 9)	$I_P = I_9$	typ.	45 mA
Inputs			
Chrominance signal			
3,58 MHz for record (peak-to-peak value)	$V_{2\text{-}15(p\text{-}p)}$	typ.	200 mV
629 kHz for playback (peak-to-peak value)	$V_{1\text{-}15(p\text{-}p)}$	typ.	200 mV
Outputs			
Chrominance signal			
3,58 MHz (peak-to-peak value)	$V_{24\text{-}15(p\text{-}p)}$	typ.	490 mV
629 kHz (peak-to-peak value)	$V_{26\text{-}15(p\text{-}p)}$	typ.	2 V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

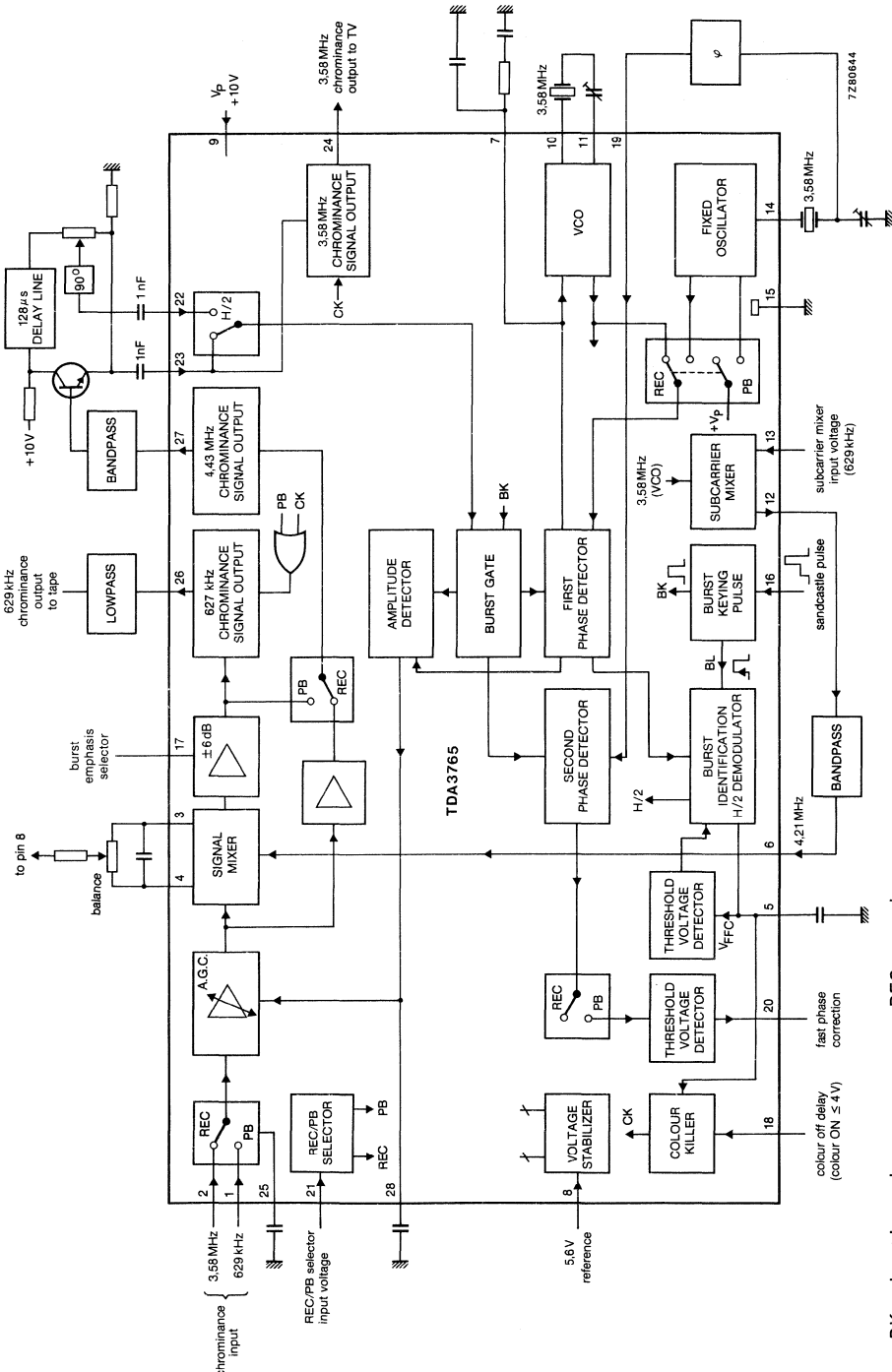


Fig. 1 Block diagram.

BK = burst key pulse
BL = blanking pulse
FFC = flip-flop correction
FPC = fast phase correction

REC = record
PB = playback
CK = colour killer

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 9)	$V_P = V_{9-15}$	max.	13,2	V
Voltage range at pins 1, 2, 5, 7, 8, 9, 16, 18, 19, 20, 21, 22, 23 to pin 15 (ground)	V_{n-15}		0 to V_P	V
Voltages ranges				
at pins 3, 4, 28*	$V_{3, 4, 28-15}$		3 to 6	V
at pin 6, 25*	$V_{6, 25-15}$		0 to 5	V
at pin 10*	V_{10-15}		1,5 to 4	V
at pin 13*, 17*	$V_{13, 17-15}$		0 to 3	V
at pin 14*	V_{14-15}		0 to 8	V
Voltages				
at pin 12	V_{12-15}	max.	V_P	V
at pin 24	V_{24-15}	max.	7	V
Currents				
at pins 11, 18	$-I_{11, 18}$	max.	2	mA
at pins 12, 26, 27	$-I_{12, 26, 27}$	max.	5	mA
at pin 24	$-I_{24}$	max.	3	mA
Total power dissipation	P_{tot}	max.	1,4	W
Storage temperature range	T_{stg}		−25 to + 150	°C
Operating ambient temperature range	T_{amb}		0 to + 70	°C

* Measured with $V_{8-15} = 5{,}6$ V.

CHARACTERISTICS

$V_P = V_{9-15} = 10$ V; $V_{8-15} = 5{,}6$ V; $T_{amb} = 25\ ^oC$; burst key duration 4 μs; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 9)					
Supply voltage	$V_P = V_{9-15}$	9,6	–	13,2	V
Supply current for playback and burst keying					
at $-I_{12, 18, 24, 26, 27} = 0$	$I_P = I_9$	–	47	–	mA
at $-I_{12, 18, 24, 26, 27} = 0$; $V_P = 12$ V	$I_P = I_9$	–	49	–	mA
A.G.C. preamplifier (pins 1 and 2)					
Input voltage* (f = 3,58 MHz) during record (peak-to-peak value)	$V_{2-15(p-p)}$	20	–	400	mV
Input voltage* (f = 629 kHz) during playback (peak-to-peak value)	$V_{1-15(p-p)}$	30	–	400	mV
Input resistance	$R_{1, 2-15}$	7	–	–	kΩ
Input capacitance	$C_{1, 2-15}$	–	–	5	pF
629 kHz chrominance signal (pin 26)* (transposed on to 629 kHz signal)					
Output voltage (peak-to-peak value)	$V_{26-15(p-p)}$	–	2	–	V
Signal suppression at output					
for f = 1,26 MHz	α_{26}	–	35	–	dB
for f = 4,21 MHz (externally balanced via pins 3 and 4)	α_{26}	–	40	–	dB
during colour killing (pin 25	α_{26}	40	–	–	dB
D.C. output voltage	V_{26-15}	–	6,7	–	V
3,58 MHz chrominance signal (pin 27)*					
Output voltage					
during record (peak-to-peak value)	$V_{27-15(p-p)}$	–	1,15	–	V
during playback after signal mixing (peak-to-peak value)	$V_{27-15(p-p)}$	–	–	3,1	V
Signal suppression at output					
for f = 4,21 MHz (externally balanced)	α_{27}	–	40	–	dB
for f = 7,16 MHz	α_{27}	–	30	–	dB
for f = 2,95 MHz	α_{27}	–	38	–	dB
for f = 2,32 MHz	α_{27}	–	30	–	dB
D.C. output voltage	V_{27-15}	–	7	–	V

* The chrominance signal values hold for a 75% saturated colour bar signal.

parameter	symbol	min.	typ.	max.	unit
3,58 MHz chrominance signal amplifier*					
Burst input signal					
at pin 22 (peak-to-peak value)	$V_{22\text{-}15(p\text{-}p)}$	–	225	–	mV
at pin 23 (peak-to-peak value)	$V_{23\text{-}15(p\text{-}p)}$	–	225	–	mV
Input resistance					
at pin 22	$R_{22\text{-}15}$	6	–	–	kΩ
at pin 23	$R_{23\text{-}15}$	6	–	–	kΩ
Output voltage of the chrominance signal at pin 24 (peak-to-peak value)	$V_{24\text{-}15(p\text{-}p)}$	–	490	–	mV
Signal suppression at output (pin 24) during colour killing	α_{24}	35	–	–	dB
D.C. output voltage					
during colour-on	$V_{24\text{-}15}$	–	2,4	–	V
during colour-off (killed)	$V_{24\text{-}15}$	–	0,7	–	V
Subcarrier mixer					
629 kHz input voltage; sine-wave (peak-to-peak value)	$V_{13\text{-}15(p\text{-}p)}$	220	–	–	mV
Input resistance	$R_{13\text{-}15}$	1	–	–	kΩ
D.C. output voltage	$V_{12\text{-}15}$	–	7,9	–	V
4,21 MHz output voltage selective** (peak-to-peak value)	$V_{12\text{-}15(p\text{-}p)}$	–	800	–	mV
Signal suppression at output**					
for f = 3,58 MHz	α_{12}	20	–	–	dB
for f = 4,84 MHz	α_{12}	30	–	–	dB
Subcarrier input					
4,21 MHz input voltage (peak-to-peak value)	$V_{6,15(p\text{-}p)}$	250	–	–	mV
Input resistance	$R_{6\text{-}15}$	1,9	–	–	kΩ
Input capacitance	$C_{6\text{-}15}$	–	–	5	pF
3,58 MHz voltage controlled oscillator (VCO)					
Input resistance	$R_{10\text{-}15}$	–	430	–	Ω
Input capacitance	$C_{10\text{-}15}$	–	–	10	pF
Output resistance	$R_{11\text{-}15}$	–	–	200	Ω
PLL-controlled oscillator catching range	Δf	± 500	–	–	Hz
Phase difference between oscillator and burst signals for ± 400 Hz deviation of crystal frequency	φ	–	–	± 7	deg

* Chrominance signal values hold for a 75% saturated colour bar signal.

** Measured with a 0,32 V (peak-to-peak), 629 kHz input signal on pin 13 ($-I_{12}$ = 1 mA).

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
3,58 MHz fixed oscillator					
Oscillator temperature coefficient*	TC	–	–	–3	Hz/K
Record/playback selector (pin 21)					
Input voltage for record**	$V_{21\text{-}15}$	–	–	4	V
Input current with $V_{21\text{-}15}$ = 4 V	I_{21}	–	–	130	μA
Input voltage for playback	$V_{21\text{-}15}$	8	–	–	V
Input current with $V_{21\text{-}15}$ = 8 V	I_{21}	–	–	430	μA
Input resistance	$R_{21\text{-}15}$	7	–	–	kΩ
Colour (on/off) killer delay					
Delay for chrominance signal OFF at AV = 1 V; C = 1 μF; PNP emitter follower with internal current of 0,1 mA	t_d	–	10	–	ms
Input voltage (pin 18)					
for forced colour ON	$V_{18\text{-}15}$	–	–	4	V
for forced colour OFF	$V_{18\text{-}15}$	5,5	–	9	V
Voltage stabilizer (pin 8)					
Range of external reference voltage	$V_{8\text{-}15}$	5,3	–	5,8	V
Input current	$-I_8$	–	–	120	μA
Sandcastle pulse input (pin 16)					
Input voltage for burst keying	$V_{16\text{-}15}$	7,1	–	–	V
Input current	I_{16}	–	–	5	μA
Delay time of BK	t_d	–	0,55	–	μs
Input voltage for triggering of flip-flop	$V_{16\text{-}15}$	2	–	–	V
Fast phase correction					
Input voltage▲ (peak-to-peak value)	$V_{19\text{-}15(p\text{-}p)}$	200	–	400	mV
Input resistance	$R_{19\text{-}15}$	3,3	–	–	kΩ
Output voltage					
without correction					
below phase differences of ± 50°					
at $I_{20} < \pm 20$ μA and $V_{17\text{-}15} = < 6{,}5$ V	$V_{20\text{-}15}$	–	–	5,2	V
with correction					
above phase differences of ± 65°					
at $I_{20} < \pm 20$ μA and $V_{17\text{-}15} = > 7{,}1$ V	$V_{20\text{-}15}$	9	–	–	V
Output resistance	$R_{20\text{-}15}$	–	35	–	kΩ

* Not considering the effects of external components.

** Pin open: record.

▲ Phase difference between output pin 14 and input pin 19 should be $\varphi = 90°$.

parameter	symbol	min.	typ.	max.	unit
Burst emphasis selector (pin 17)					
Input voltage active emphasis	V_{17-15}		open connection		
Input voltage inactive emphasis	V_{17-15}	–	–	0,5	V
Burst pre-emphasis at REC chroma output pin 26		–	6	–	dB
Burst de-emphasis at PB chroma output pin 27		–	5,3	–	dB

APPLICATION INFORMATION

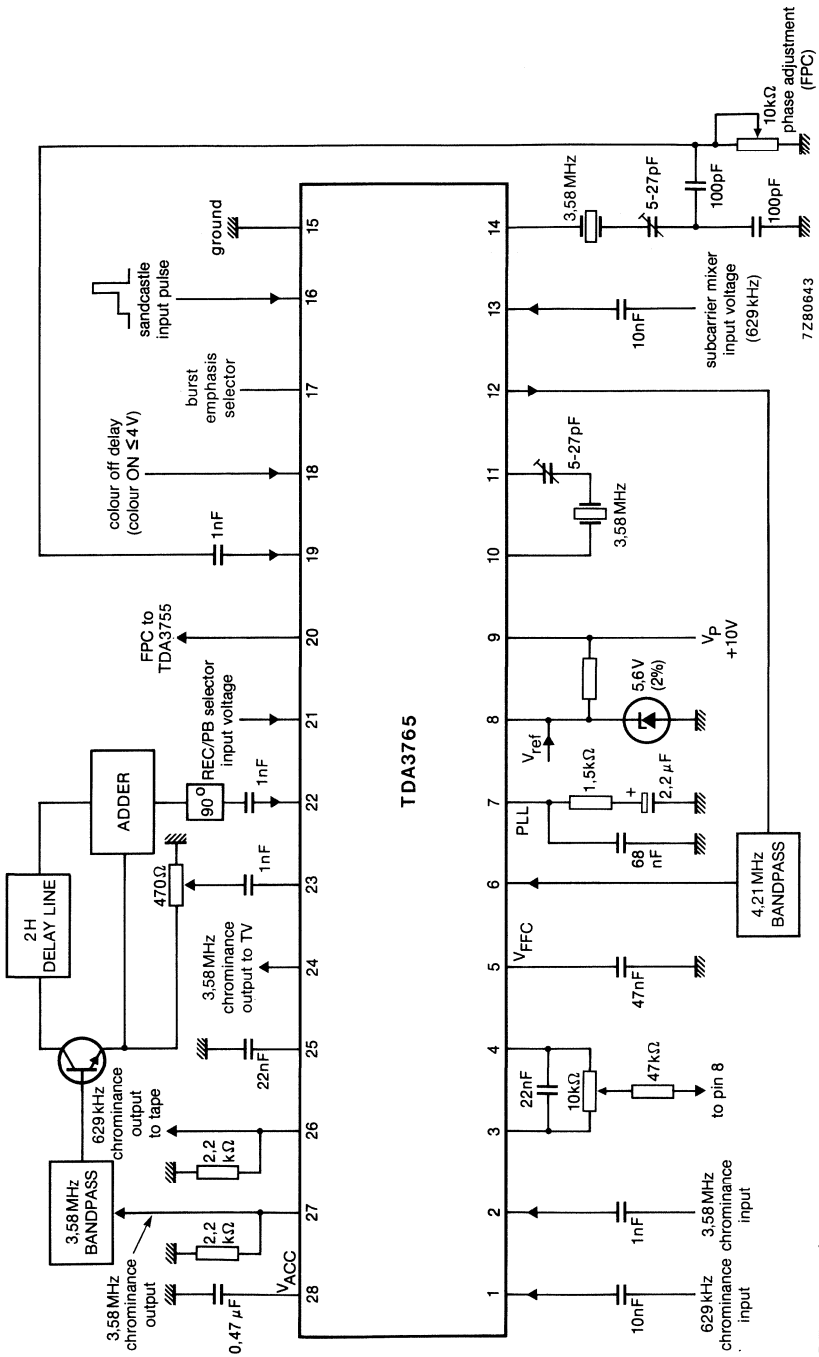


Fig. 2 Application diagram.

REC = record
PB = playback
FPC = fast phase correction
FFC = flip-flop correction

BAND SELECTOR AND WINDOW DETECTOR

GENERAL DESCRIPTION

The TDA3791 is a monolithic integrated circuit intended for application in search-tuning systems for video recorders. It is designed to select one out of four tuners, each representing a particular band. Band selection tuning is indicated by a variable voltage V_{AFC}.

Features

- Voltage window detector
- Band switch selector
- 4 short-circuit protected band switches
- Muting circuit
- Delay circuit
- Short-circuit protection circuit
- Power-on reset

QUICK REFERENCE DATA

Supply voltage (pin 8)	$V_P = V_{8\text{-}16}$	typ.	12	V
Supply current (pin 8)	$I_P = I_8$			
unloaded band switches ON		typ.	25	mA
all band switches OFF		typ.	12	mA
Power dissipation	P_{tot}	max.	1,8	W
Storage temperature range	T_{stg}	−65 to +	150	°C
Operating ambient temperature range	T_{amb}	0 to	70	°C

PACKAGE OUTLINE

16-lead DIL; plastic with internal heat spreader (SOT38).

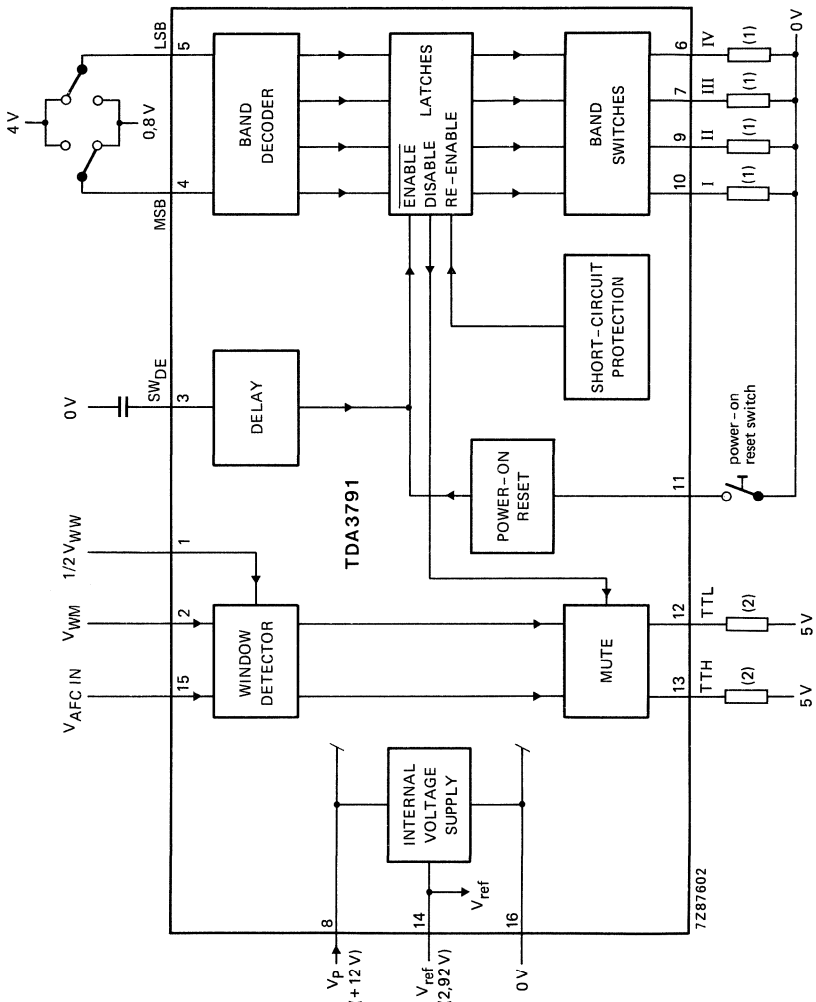


Fig. 1 Block diagram.

(1) $R = \frac{10\ V}{35\ mA}$. (2) $R = \frac{5\ V}{2\ mA}$.

FUNCTIONAL DESCRIPTION

Voltage window detector (see Table 1)

The voltage window is dependent upon two inputs; V_{WM} (pin 2) and $1/2V_{WW}$ (pin 1), which represent the centre of the window and the (window width)/2 respectively.

The voltage window range is from $V_{WM} - 1/2V_{WW}$ to $V_{WM} + 1/2V_{WW}$. A variable input voltage $V_{AFC\ IN}$ (pin 15) is compared with these window edges.

Table 1 Truth table; window detector

inputs	outputs	
$V_{AFC\ IN} = V_{15-16}$; $V_{WM} = V_{2-16}$; $V_{WW} = V_{1-16}$	V_{12-16}	V_{13-16}
$V_{AFC\ IN} < V_{WM} - 1/2V_{WW}$	HIGH	LOW
$V_{WM} - 1/2V_{WW} < V_{AFC\ IN} < V_{WM} + 1/2V_{WW}$	HIGH	HIGH
$V_{AFC\ IN} > V_{WM} + 1/2V_{WW}$	LOW	HIGH

Where: V_{12-16} = tuning too low (TTL); V_{13-16} = tuning too high (TTH).

During transitions of the outputs (V_{12-16} and V_{13-16}), a hysteresis value of approximately 20 mV is applied at the window edges.

Band-switch selector (see Table 2)

Selection of the band switches is determined by the input voltage levels of MSB (pin 4) and LSB (pin 5).

- If MSB or LSB > 4 V, the input is HIGH
- If MSB or LSB < 0,8 V, the input is LOW.

The band switches are selected as confirmed by Table 2.

Table 2 Truth table; band switch selector

MSB (V_{4-16})	LSB (V_{5-16})	switch	HIGH output
HIGH	HIGH	I	V_{10-16}
HIGH	LOW	II	V_{9-16}
LOW	HIGH	III	V_{7-16}
LOW	LOW	IV	V_{6-16}

Short-circuit protected band switches

A selected band switch has a minimum output voltage of $V_P - 0,3$ V provided the current is not more than 35 mA (I_{10}, I_9, I_7, I_6). If the output voltage at pins 10, 9, 7 or 6 is less than 9 V a short-circuit condition exists, and the output current will not be more than 80 mA. In this event the band switch is switched off, after an externally determined delay.

Muting

The muting circuit is active when a selected band switch is switched off. Both outputs TTL (pin 12) and TTH (pin 13) will then be LOW.

FUNCTIONAL DESCRIPTION (continued)

Delay circuit

After selection of a band switch, it will be in a conducting state. If after selection and a delay, the output voltage has not reached 9 V, the band is switched off. This delay is determined by an external capacitor on output SW_{DE} (pin 3).

Short-circuit protection

The short-circuit protection of each switch is provided by a flip-flop. If the condition of a band switch $V_o < 9$ V is detected, its flip-flop will be set and the band switch is switched off.

In the event of an incidental short-circuit to a band switch output, the band switch can be reset by applying 0 V to the power-on reset input (pin 11) or 0 V to the switch delay output SW_{DE} (pin 3).

Power-on reset

Before the voltage supply reaches 9,6 V, the short-circuit protection flip-flops are reset to enable the selection of a band switch.

The power-on reset circuit also supplies the voltage level for short-circuit detection.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 8)	$V_P = V_{8\text{-}16}$	max. 13,2 V
Total power dissipation	P_{tot}	see Fig. 2
Storage temperature range	T_{stg}	−65 to +150 °C
Operating ambient temperature range	T_{amb}	0 to +70 °C

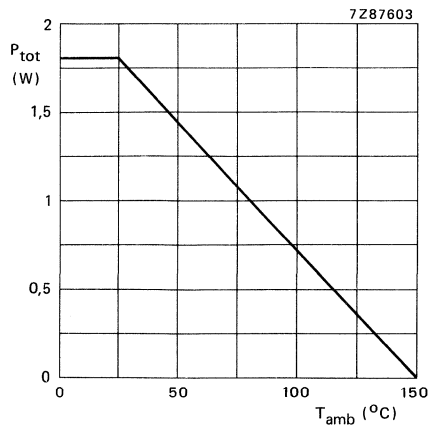


Fig. 2 Power derating curve.

CHARACTERISTICS

$V_P = V_{8-16} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pin 8)	$V_P = V_{8-16}$	10	12	13,2	V
Supply current (pin 8)					
unloaded band switches ON	$I_P = I_8$	18	25	38	mA
all band switches OFF	$I_P = I_8$	9	12	16	mA
Voltage range					
$1/2V_{WW}$ (pin 1)	V_{1-16}	0,1	–	4,5	V
V_{WM} (pin 2)	V_{2-16}	1,8	–	10,5	V
$V_{WM} + 1/2V_{WW}$ at $V_{8-16} - 1,4$ V	$V_{2-16} \pm V_{1-16}$	1,7	–	10,6	V
$V_{AFC\ IN}$ (pin 15)	V_{15-16}	0,5	–	11,5	V
Input current					
$1/2V_{WW}$ (pin 1)	$-I_1$	–	–	2	μA
V_{WM} (pin 2)	I_2	–	–	0,2	μA
$V_{AFC\ IN}$ (pin 15)	I_{15}	–	0,2	0,4	μA
Hysteresis voltage V_{AFC}*	ΔV_{15-16}	–	20	50	mV
Delta current at $V_{AFC\ IN}$*	ΔI_{15}	–	–	25	nA
Temperature coefficient $I_{AFC\ IN}$	$TC(I_{15})$	–	–0,42	–	nA/°C
Temperature coefficient I_{WM}	$TC(I_2)$	–	–0,27	–	nA/°C
Deviation of applied voltage (pin 1)					
at $V_{1-16} = 100$ mV	ΔV_{1-16}	–35	–	+35	mV
at $V_{1-16} = 4,0$ V; $V_{2-16} = 6$ V	ΔV_{1-16}	–200	–	+200	mV
Input current (pin 4)					
at MSB $< 0,8$ V	I_4	–	–	0,1	μA
at MSB > 4 V	I_4	–	–	1,0	μA
Input current (pin 5)					
at LSB > 4 V	I_5	–	–	1,0	μA
at LSB $< 0,8$ V	I_5	–	–	0,1	μA
Voltage level (pin 4)					
at MSB HIGH	V_{4-16}	4	–	–	V
at MSB LOW	V_{4-16}	–	–	0,8	V
Voltage level (pin 5)					
at LSB HIGH	V_{5-16}	4	–	–	V
at LSB LOW	V_{5-16}	–	–	0,8	V
Short-circuit current of band switches I, II, III, IV (pins 10, 9, 7, 6)	$-I_{10, 9, 7, 6}$	35	50	80	mA
Voltage drop of band switches I, II, III, IV (pins 10, 9, 7, 6) at $I_{o(max)} = 35$ mA; $V_P = 10$ V	$V_{10, 9, 7, 6-16}$	–	–	0,3	V

* During switching of outputs V_{12-16} and/or V_{13-16}.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Voltage level short-circuit detection at $0{,}75V_P$	$V_{10,\,9,\,7,\,6\text{-}16}$	8,0	9,0	9,5	V
Output voltage (pin 13) TTH at I_{13} = 2 mA (LOW)	$V_{13\text{-}16}$	–	–	0,3	V
Output voltage (pin 12) TTL at I_{12} = 2 mA (LOW)	$V_{12\text{-}16}$	–	–	0,3	V
Leakage current (pin 13) TTH at $V_{13\text{-}16}$ = 13,2 V	I_{13}	–	–	10	μA
Leakage current (pin 12) TTH at $V_{12\text{-}16}$ = 13,2 V	I_{12}	–	–	10	μA
Output current (pin 3) SW_{DE} at $V_{3\text{-}16}$ = 6 V	$-I_3$	5	12	20	μA
Maximum value of delay capacitor	C_3	–	–	40	nF
Maximum delay time at ± C_3 (nF)/(I_3/10) ms	t_d	–	–	50	ms
Power-on-reset voltage	$V_{8\text{-}16}$	6	–	9,6	V
Leakage current unswitched band switches at $V_{10,\,9,\,7,\,6\text{-}16}$ = −12 V	$I_{10,\,9,\,7,\,6}$	–	–	5	μA

STEREO/DUAL TV SOUND PROCESSING CIRCUITS

GENERAL DESCRIPTION

The TDA3800G; GS are stereo/dual TV sound decoder circuits for processing an a.f. and a sound i.f. signal in TV and VCR equipment, using active filters in selective frequency processing.

In deviation of our standard terms and conditions of sale the supply of the TDA3800 (ABS) does not imply any patent indemnity whatsoever with respect to the stereo-tone patent rights of I.G.R. Germany.

Features

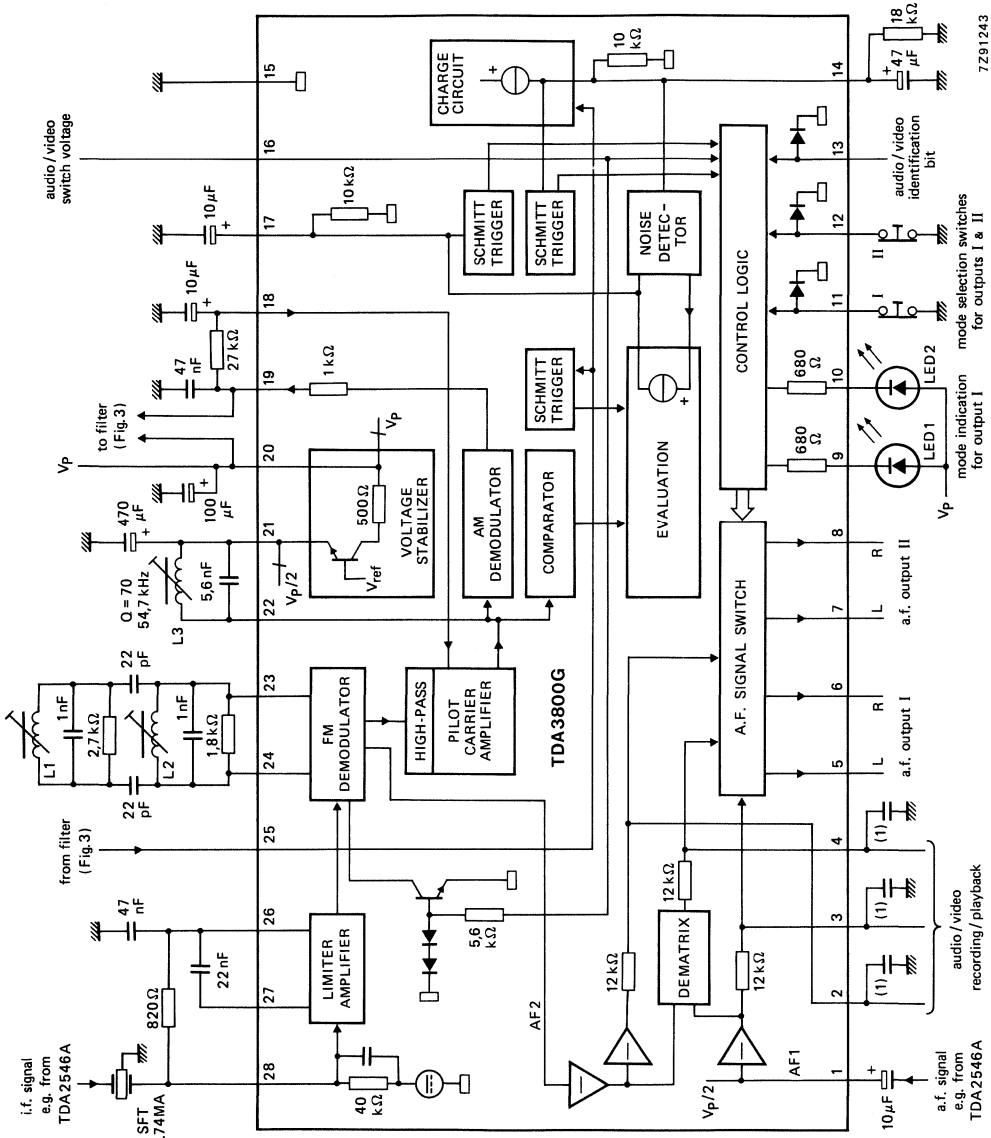
- Signal processing of one a.f. signal and one i.f. signal
- 2nd i.f. limiter/amplifier and FM demodulator (5,742 MHz) for the second sound channel
- Pilot carrier processing with digital identification, hysteresis and short switching times
- De-matrixing of the signals for the two audio channels
- De-emphasis
- Two dual channel, independently controllable a.f. outputs
- Low-resistance a.f. outputs (short-circuit protected); can be used for headphone
- Standardized switched output for controlling external audio/video equipment
- Signal path control by an identification bit (also in audio/video mode)
- LED indication of selected mode (also in audio/video mode)
- Possibility to apply a.f. signals from external equipment via the de-emphasis inputs (audio/video mode)
- Mode selection of stereo/mono or sound I/sound II
  TDA3800G dynamic selection with internal storage
  TDA3800GS static selection

QUICK REFERENCE DATA

Supply voltage (pin 20)	$V_P = V_{20\text{-}15}$	typ.	12 V
2nd sound i.f. input voltage for start of limiting (r.m.s. value)	$V_{i(rms)}$	typ.	50 μV
Pilot carrier amplifier control range	ΔG_v	min.	20 dB
A.F. input voltage (r.m.s. value)	$V_{i(rms)}$	typ.	1 V
A.F. demodulator output voltage (r.m.s. value)	$V_{o(rms)}$	typ.	0,6 V
LED output current	I_{LED}	typ.	15 mA
Signal-to-noise ratio of the a.f. signal switches	S/N	typ.	80 dB
Crosstalk in stereo mode	α_S	min.	40 dB
Crosstalk in dual sound mode	α_{DS}	min.	60 dB

PACKAGE OUTLINES

28-lead DIL; plastic (SOT117).



(1) De-emphasis 3,9 nF.
(2) TDA3800G application using active filters.

Coil data

L1 and L2: TOKO 7 k;
$Q = 25$, $f_o = 5{,}74$ MHz.

Fig. 1 TDA3800G block diagram and test circuit in accordance with Fig. 3.

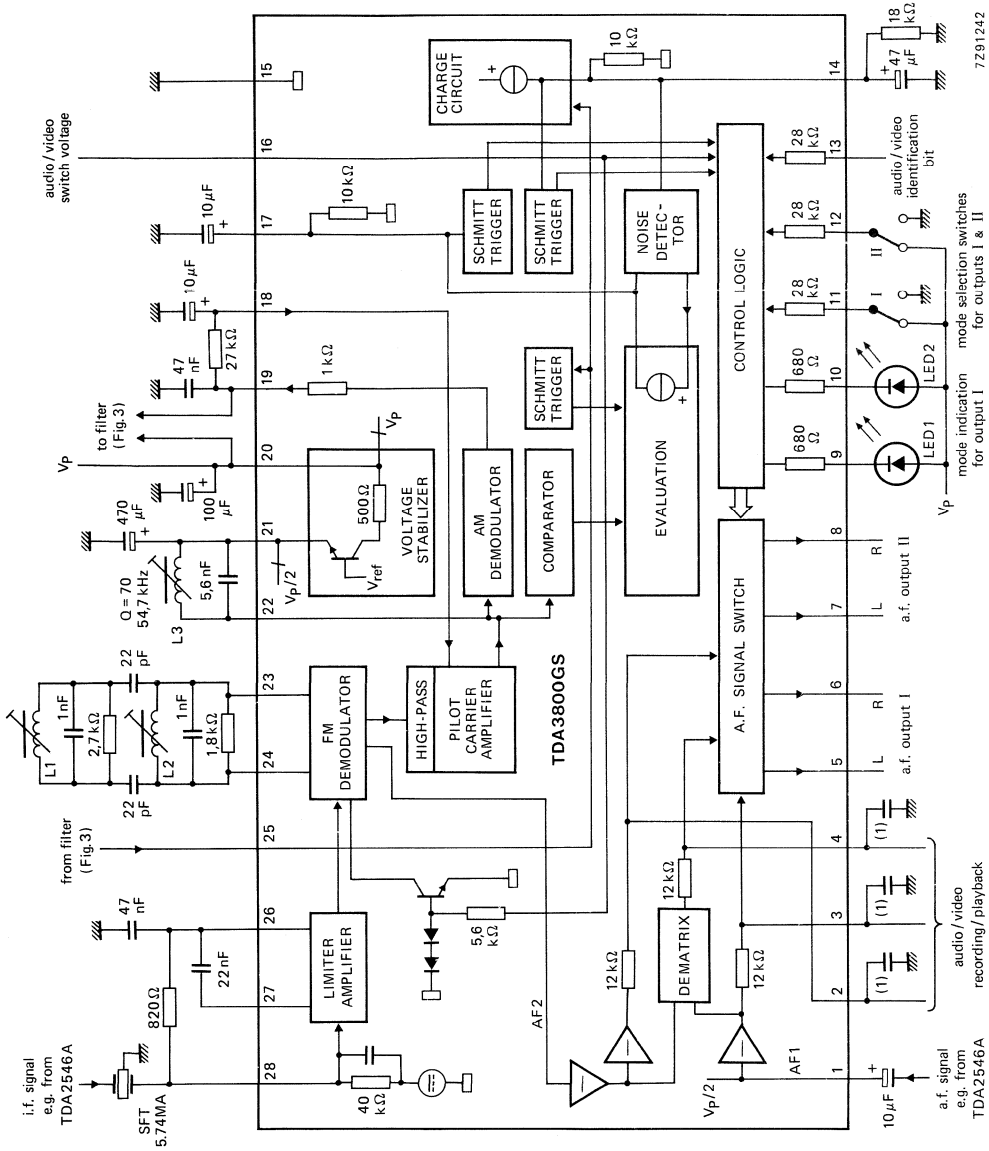


Fig. 2 TDA3800GS block diagram and test circuit in accordance with Fig. 3.

(1) De-emphasis 3,9 nF.
(2) TDA3800GS application using active filters.

Coil data

L1 and L2: TOKO 7 k;
Q = 25, f_o = 5,74 MHz.

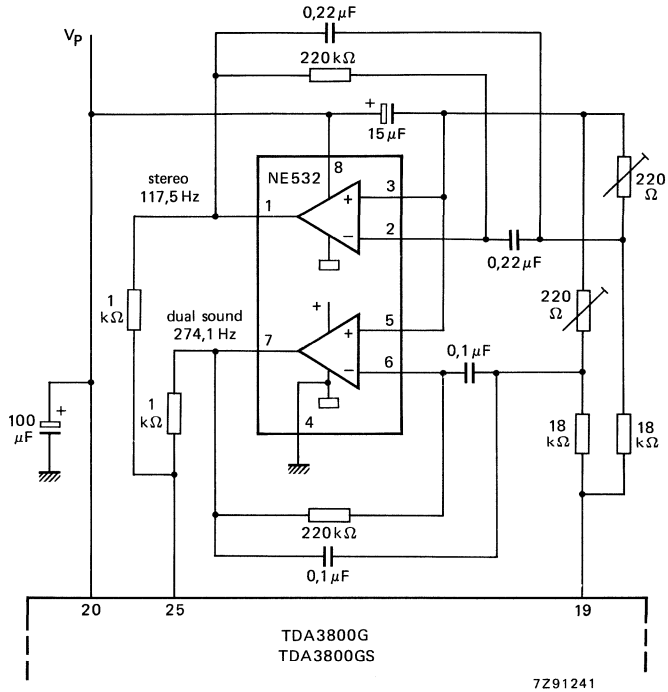


Fig. 3 External filter circuit for the identification frequencies 117,5 Hz and 247,1 Hz.

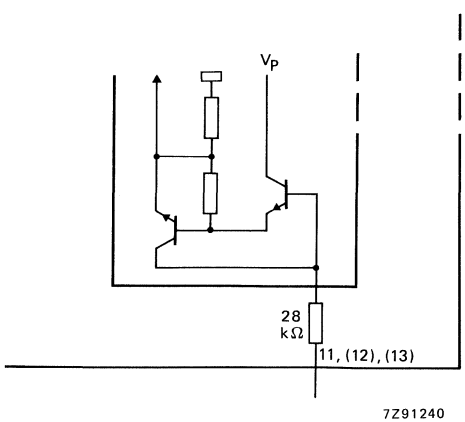


Fig. 4 TDA3800GS internal circuit for the control input leads 11, 12 and 13.

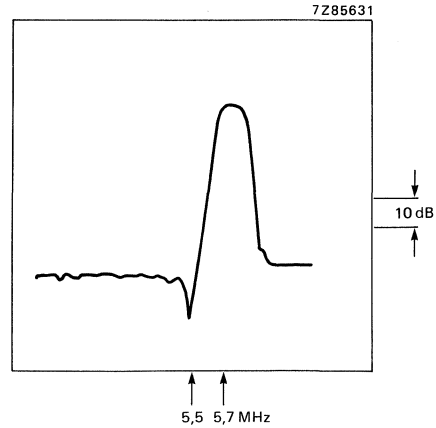


Fig. 5 IF2 filter selection.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 20)	$V_P = V_{20-15}$	max.	14 V
Voltage			
at pins 1; 9; 10; 16 and 25	V_{n-15}	max.	V_P
at pins 11; 12 and 13*	$V_{11;12;13-15}$	max.	V_P
Current			
at pins 11; 12 and 13**	$I_{11;12;13}$	max.	1 mA
at pin 21	short-circuit protected		
Total power dissipation	P_{tot}	max.	1,5 W
Storage temperature range	T_{stg}	−25 to +150	°C
Operating ambient temperature range	T_{amb}	0 to +70	°C

* TDA3800GS only.
** TDA3800G only.

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; measured in Fig. 1/Fig. 2 with a 1 kHz signal. $V_{1\text{-}15(rms)}$ = 0,5 V, an i.f. signal $V_{28\text{-}15(rms)}$ = 5 mV (VC/2SC = 20 dB, Δf = ± 50 kHz, f_m = 400 Hz) and with adjusted de-matrix circuit; i.f. filter selection at input pin 28 as in Fig. 5; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply (pin 20)					
Supply voltage range	$V_P = V_{20\text{-}15}$	10,8	12	13,2	V
Supply current (without LED current; mono)	$I_P = I_{20}$	40	–	87	mA
FM limiter/amplifier and demodulator					
Start of limiting	$V_{28\text{-}15(rms)}$	–	–	60	μV
Input resistance	$R_{28\text{-}15}$	–	40	–	kΩ
Input capacitance (Fig. 5)	$C_{28\text{-}15}$	–	4,5	–	pF
AM suppression at V_i = 0,5 mV; Δf = ± 30 kHz	α_{AMS}	50	–	–	dB
Pilot carrier processing					
D.C. input voltage	$V_{18\text{-}15}$	–	7,2	–	V
D.C. voltage (reference via tuning coil)	$V_{22\text{-}15}$	–	6,0	–	V
AM demodulator output voltage	$V_{19\text{-}15}$	–	7,3	–	V
Controlled pilot carrier output voltage (peak-to-peak value)	$V_{22\text{-}21(p\text{-}p)}$	–	250	–	mV
Output resistance	$R_{22\text{-}15}$	50	–	–	kΩ
Identification frequency evaluation					
No identification signal (lower threshold)	$V_{14\text{-}15}$	–	–	2	V
Identification signal (upper threshold)	$V_{14\text{-}15}$	4	–	–	V
Stereo transmission	$V_{17\text{-}15}$	–	–	2	V
Dual sound transmission	$V_{17\text{-}15}$	4	–	–	V
De-matrixing					
Output voltages	$V_{2;3;4\text{-}15}$	–	5,3	–	V
De-emphasis output resistances	$R_{2;3;4\text{-}15}$	–	12	–	kΩ
A.F. output signal of 2nd i.f. (r.m.s. value)	$V_{2\text{-}15(rms)}$	–	0,6	–	V
Attenuation of the demodulator output signal AF2 at audio/video mode	α_{AF2}	75	–	–	dB
Distortion of the AF2 signal $V_{o2\text{-}15}$	d_{tot}	–	0,4	–	%

parameter	symbol	min.	typ.	max.	unit
AF1 input					
D.C. input voltage	$V_{1\text{-}15}$	–	6	–	V
Input resistance	$R_{1\text{-}15}$	–	14	–	kΩ
Maximum input signal (r.m.s. value)	$V_{1\text{-}15(rms)}$	–	2	–	V
A.F. signal switches					
D.C. output voltages	$V_{5;6;7;8\text{-}15}$	–	5,3	–	V
Output resistances	$R_{5;6;7;8\text{-}15}$	–	200	–	Ω*
Maximum a.f. output signals (r.m.s. value)					
for $V_{AFI(rms)}$	$V_{5;6\text{-}15(rms)}$	–	2	–	V
for $V_{AFII(rms)}$	$V_{7;8\text{-}15(rms)}$	–	2	–	V
Total distortion when applying a signal at $V_{2;3;4\text{-}15(rms)} = 0{,}5$ V	d_{tot}	–	–	0,1	%
Signal plus noise-to-noise ratio	S + S/N	–	80	–	dB
Crosstalk attenuation					
in stereo mode (f = 1 kHz at pin 2)	α_S	40	–	–	dB
in dual sound mode (f = 20 Hz to 20 kHz)	α_{DS}	60	–	–	dB
Audio/video switch					
Audio/video switch voltage					
for playback (HIGH)	$V_{16\text{-}15}$	7	–	V_P	V
for recording (LOW)	$V_{16\text{-}15}$	0	–	2,5	V
Audio/video identification bit (TDA3800G)					
for stereo mode (LOW)	$V_{13\text{-}15}$	0	–	0,2	V
for dual sound mode (HIGH) at $V_{13\text{-}15} \approx 0{,}7$ V	I_{13}	–	0	–	mA
Audio/video switch voltage (TDA3800GS) (stereo/dual sound)					
for stereo mode (LOW)	$V_{13\text{-}15}$	–	–	0,8	V
for dual sound mode (HIGH)	$V_{13\text{-}15}$	2,4	–	–	V
Mode selection switches for outputs I and II					
Active LOW (TDA3800G)					
input voltage LOW	$V_{11;12\text{-}15}$	0	–	0,2	V
switch open condition at $V_{11;12\text{-}15} \approx 0{,}7$ V	$I_{11;12}$	–	0	–	mA
Pulse duration	t_p	1	–	–	μs

* Connection of high-impedance headphones is possible.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Switching voltage (TDA3800GS)					
Mono transmission both equals I and II mono					
Dual sound transmission switching voltage to pin 11 (pin 12 not affected)					
a.f. output II sound I and a.f. output I sound II	$V_{11\text{-}15}$	–	–	0,8	V
a.f. output I sound I and a.f. output II and II	$V_{11\text{-}15}$	2,4	–	–	V
Stereo transmission switching voltage to pin 12 (pin 11 not affected)					
a.f. outputs I and II mono	$V_{12\text{-}15}$	–	–	0,8	V
a.f. outputs I and II stereo	$V_{12\text{-}15}$	2,4	–	–	V
Mode indication (pins 9 and 10; see also Table 1)					
Only the mode for output I is indicated					
Maximum output current	$I_{9;10}$	–	15	–	mA
Voltage stabilizer (pin 21)					
Output voltage	$V_{21\text{-}15}$	–	6	–	V
Maximum d.c. output current short-circuit protected	$\pm I_{21}$	–	0,5	–	mA

Notes to the characteristics (TDA3800G only)

1. Serial commands for stereo/mono or sound I/sound II selection are determined by the identification bit of the transmission.
2. The pushbuttons at pins 11 and 12 are assigned to the a.f. outputs I and II respectively.
3. When a transmitter changes its identification from dual sound to stereo and then back to dual sound again, the last selected dual sound signal is available automatically because of the internal storage of the choice. This is also applicable for mono/stereo selection.
4. Power-on reset: when applying the supply voltage, the stereo or the AF1 signal appears at both outputs I and II depending on the type of transmission.

Table 1 Mode indication possibilities

LED 1	LED 2	selected reception mode
OFF	OFF	mono at mono or stereo transmission
ON	ON	stereo at stereo transmission
OFF	ON	AF1 signal at dual sound transmission
ON	OFF	AF2 signal at dual sound transmission

STEREO/DUAL TV SOUND DECODER CIRCUIT

GENERAL DESCRIPTION

The TDA3803A is a stereo/dual TV sound decoder circuit with static switching for processing two AF signals in TV and VCR equipment. The LOW/HIGH static switching signals control the AF output selector. Two operational amplifiers perform bandpass filtering of the identification signals.

Features

- Amplification of the two AF input signals by integrated operational amplifiers
- Low distortion stereo de-matrix
- All operational amplifiers offset compensated
- De-emphasis with operational amplifiers, preferably applied to the output terminals
- Two output ports each with two channels for headphones and loudspeakers
- Dual sound information at one port, each port individually switchable from sound I to sound II and sound II to sound I
- Mute function; while mute is active, it is possible to connect an external mono AF input signal to pin 10 appearing at pins 20 to 23.
- Identification without additional signals (horizontal etc.)

QUICK REFERENCE DATA

Supply voltage (pin 13)	$V_P = V_{13\text{-}12}$	typ.	12 V
Supply current (pin 13)	$I_P = I_{13}$	typ.	28 mA
Pilot carrier amplifier gain control range	ΔG_v	>	40 dB
AF input signals; at G_v = 0 dB (r.m.s. value)	$V_{i(rms)}$	=	1 V
LED output current	I_{LED}	typ.	12 mA
Weighted signal-to-noise ratio of the a.f. signal switches (CCIR468/2)	(S+N)/N	⩾	60 dB
Crosstalk in stereo mode	α_S	>	40 dB
Crosstalk in dual sound mode	α_{DS}	>	60 dB

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

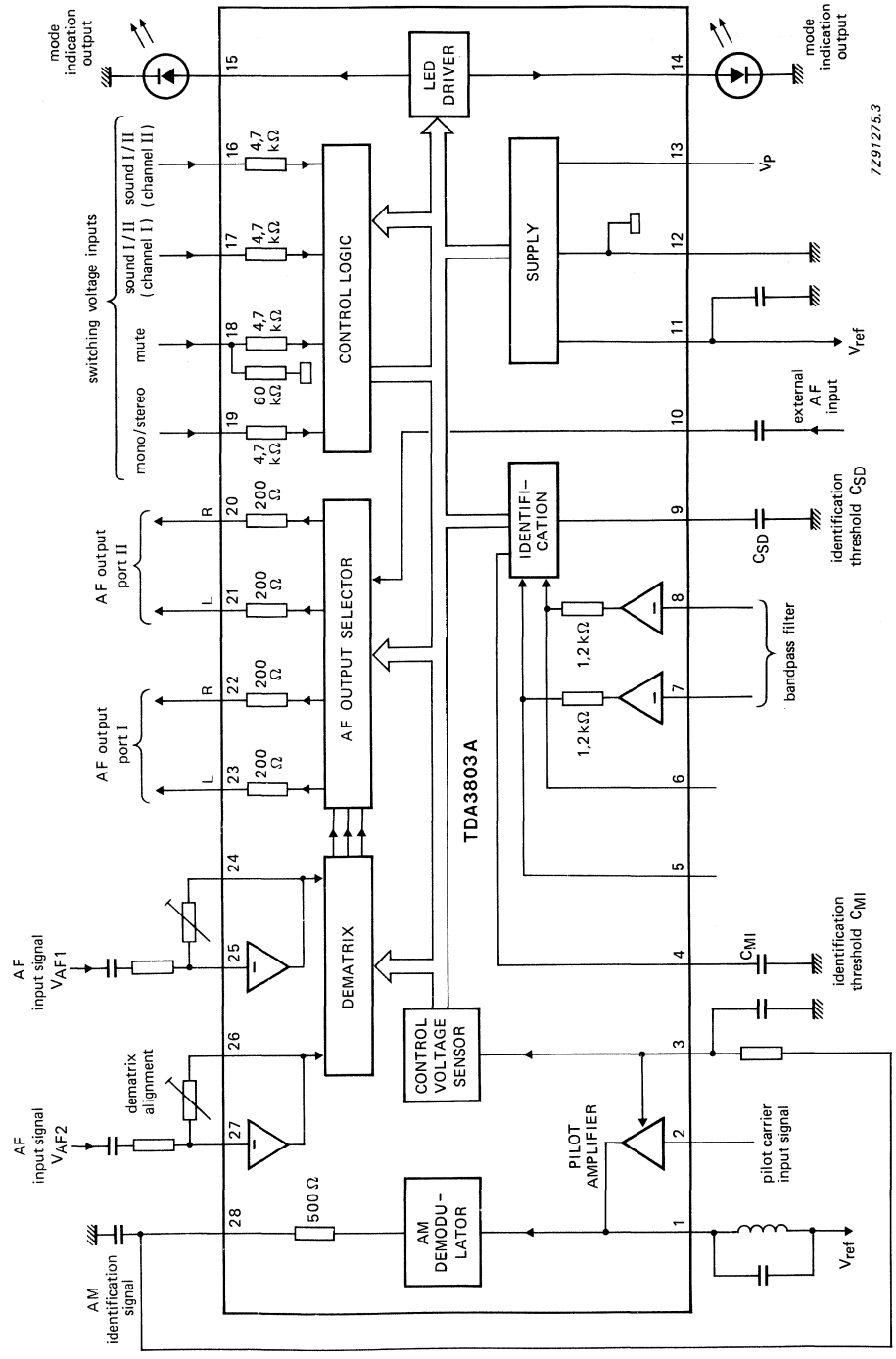


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 13)	$V_P = V_{13-12}$	max.	14 V
Voltages with respect to pin 12 (ground)			
pins 25; 27 and 28	$V_{25;27;28-12}$	max.	V_P
Voltages			
pin 1 to pin 10	V_{n-12}	max.	V_P
pin 14 to pin 19	V_{n-12}	max.	V_P
Currents			
pin 11	I_{11}	max.	3 mA
pins 20; 21; 22; 23	$I_{20;21;22;23}$	max.	10 mA
pin 28	$-I_{28}$	max.	3 mA
Total power dissipation	P_{tot}	max.	1,5 W
Storage temperature range	T_{stg}		−25 to +125 °C
Operating ambient temperature range	T_{amb}		0 to +70 °C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; overall voltage gain (G_v) = 1; ($R_S = R_R$); measured in Fig. 2 with a 1 kHz signal. AF input AF2 = AF1 = 0,5 V, pilot carrier input signal $V_{2\text{-}12(rms)}$ = 16 mV, m = 0,5 and with adjusted de-matrix circuit; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 13)					
Supply voltage range	$V_P = V_{13\text{-}12}$	10,8	12	13,2	V
Supply current (without LED current)	$I_P = I_{13}$	–	28	35	mA
Reference voltage (pin 11)	V_{ref}	–	6	–	V
Input resistance (dynamic)	$R_{11\text{-}12}$	–	4	–	kΩ
AF part					
Amplification	G_v	–40	–	18	dB
Input signal at G_v = 1	$V_{AF1} = V_{AF2}$	–	–	1	V
Mono AF input signal (pin 10)*					
Input signal	$V_{10\text{-}12}$	–	–	2	V
DC input voltage level	$V_{10\text{-}12}$	–	6	–	V
Input resistance	$R_{10\text{-}12}$		16	–	kΩ
Stereo mode AF output port I pin 22: right pin 23: left					
AF output port II pin 20: right pin 21: left					
Output signal (THD ⩽ 0,5%)					
port I ($V_{23\text{-}12} = V_{22\text{-}12}$)	V_{oI}	–	–	2	V
port II ($V_{21\text{-}12} = V_{20\text{-}12}$)	V_{oII}	–	–	2	V
Weighted signal-to-noise ratio of the AF signal switches (in accordance with CCIR468/2)	(S+N)/N		65	–	dB
Unweighted signal-to-noise	(S+N)/N	60	–	–	dB
Total harmonic distortion ($V_{20;21;22;23\text{-}12}$ = 0,5 V; G_v = 1)	THD	–	0,05	–	%
Crosstalk attenuation (selective)					
stereo mode (f_1 = 1 kHz; f_2 = 400 Hz)	α_S	40	–	–	dB
dual sound mode (f = 250 Hz to 12,5 kHz)	α_{DS}	60	–	–	dB

* An input signal at pin 10 appears at pins 20 to 23 if the mute input (pin 18) is activated ($V_{18\text{-}12} \geqslant 2$ V).

parameter	symbol	min.	typ.	max.	unit
DC input voltage level at pins 25 and 27	$V_{25;27-12}$	–	6	–	V
DC output voltage level at pins 20; 21; 22 and 23	V_{n-12}	–	6	–	V
Output resistance at pins 20; 21; 22 and 23	V_{n-12}	–	200	–	Ω
Identification part					
Pilot carrier amplifier input signal (pin 2)	V_{2-12}	5	–	–	mV
gain control range	ΔG_v	40	–	–	dB
controlled output signal (pin 1) (peak-to-peak value)	$V_{1-12(p-p)}$	–	300	–	mV
Input resistance (pin 2)	R_{2-12}	–	60	–	kΩ
Output resistance (pin 1)	R_{1-12}	1	–	–	MΩ
DC input voltage level (pin 2) applied externally (see Fig. 2)	V_{2-12}	–	6	–	V
DC output voltage level (pin 28) without gain control	V_{28-12}	–	6	–	V
with gain control	V_{28-12}	–	7,9	–	V
Identification signal (pin 28) (peak-to-peak value)	$V_{28-12(p-p)}$	–	2,0	–	V
Filter operational amplifiers open loop gain	G_o	78	–	–	dB
Identification frequency evaluation					
No identification signal (lower threshold)	V_{4-12}	–	–	2,5	V
Identification signal (upper threshold)	V_{4-12}	4,7	–	–	V
Stereo transmission (lower threshold)	V_{9-12}	–	–	2,5	V
Dual sound transmission (upper threshold)	V_{9-12}	4,7	–	–	V
Control logic part					
Mute input voltage (pin 18) mute OFF	V_{18-12}	–	–	0,8	V
mute ON (see the remarks to pin 10)	V_{18-12}	2	–	–	V
Switching stereo/mono and sound I/sound II					
Stereo transmission switching voltage to pin 19 (pin 17 and 16 not affected)					
output ports I and II mono	V_{19-12}	–	–	0,8	V
output ports I and II stereo	V_{19-12}	2	–	–	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Control logic part (continued)					
Mono transmission both output ports I and II mono					
Dual sound transmission					
switching voltage to pin 16 (pin 19 and 17 not affected)					
output port II sound I	V_{16-12}	2	–	–	V
output port II sound II	V_{16-12}	–	–	0,8	V
switching voltage to pin 17 (pin 16 and 19 not affected)					
output port I sound I	V_{17-12}	–	–	0,8	V
output port I sound II	V_{17-12}	2	–	–	V
Mode indication (pins 14 and 15; see also Table 1)					
Output current	$-I_{14;\ 15}$	9	12	15	mA
Output voltage (note 2)	$V_{14;\ 15-12}$	0	–	8	V
Stereo/mono transmission: LED indication is valid for the transmission mode					
Dual sound transmission: LED indication is valid for port I					

Table 1 Mode indication (note 1)

transmission mode	LED pin 15	LED pin 14
mono	OFF	OFF
stereo:		
stereo selection; $V_{19-12} \geqslant 2$ V	ON	ON
mono selection; $V_{19-12} \leqslant 0{,}8$ V	ON	ON
dual sound:		
sound I selection; $V_{17-12} \leqslant 0{,}8$ V	ON	OFF
sound II selection; $V_{17-12} \geqslant 2$ V	OFF	ON

Notes to the characteristics

1. With mute (pin 18) ON both LEDs (pin 14 and 15) are switched OFF.
2. Pin 14 and 15 are also suitable as output switches to control TDA3810. At LED OFF and $I_{14,\ 15} \leqslant 100\ \mu A$, then $V_{14,\ 15-12} \leqslant 200$ mV.

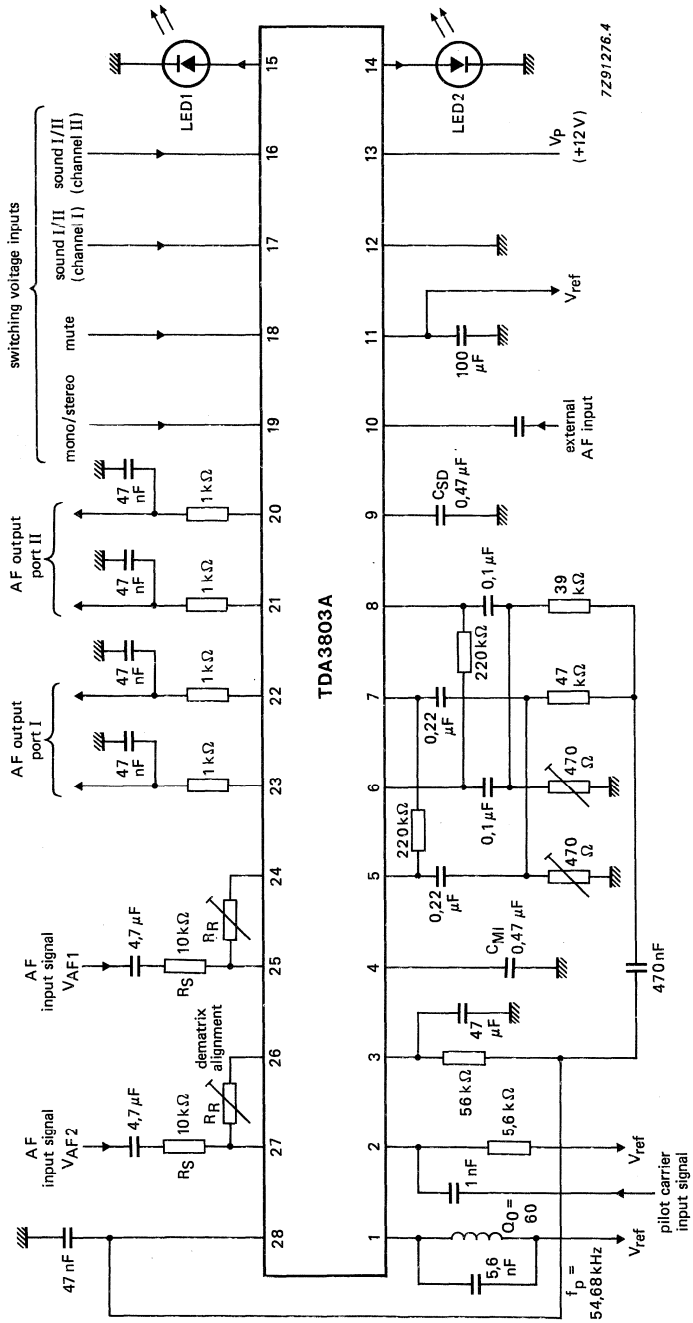


Fig. 2a Application diagram and test circuit; external components.

APPLICATION INFORMATION (continued)

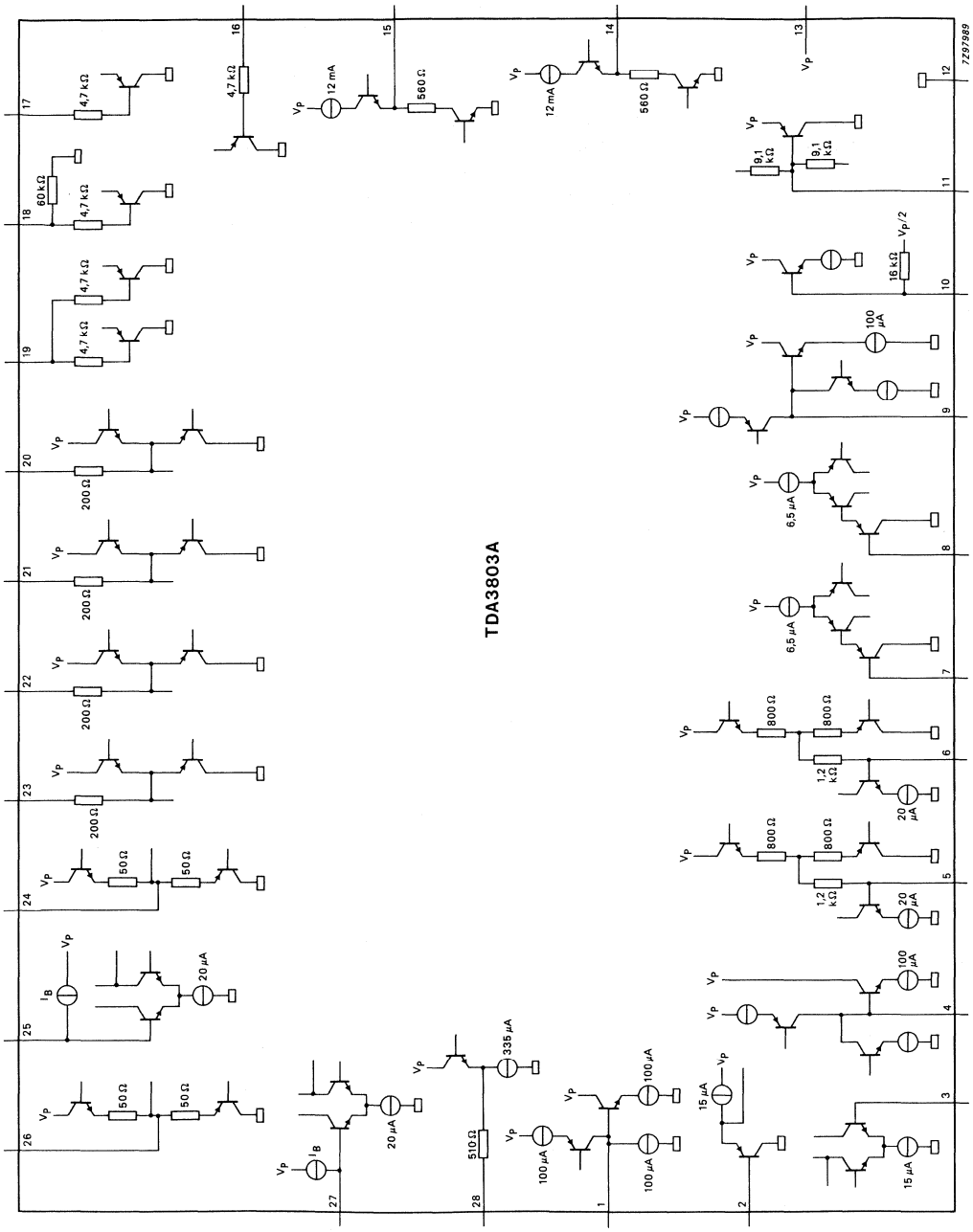


Fig. 2b Application diagram and test circuit; part of internal circuitry.

MULTIPLEX PLL STEREO DECODER

The TDA3806 is a phase-locked loop (PLL) stereo decoder for decoding the stereo multiplex signal. The decoding signal is generated by a phase-locked loop system. Second audio program (SAP) and adjacent channel interference (ACI) are suppressed by the internal circuitry. The decoder has a main signal and a sub-signal output. It is possible to apply a separate noise reduction system to the sub-signal. Main signal and noise reduced sub-signal have to be combined at an external matrix to both L and R.

Features

- Adjustable gain by external resistors (separate for main and sub-signal)
- D.C. input for smooth mono-stereo takeover control (without influencing the pilot indicator)
- Pilot dependent mono-stereo switch
- Pilot indicator driver
- PLL oscillator switch-off facility
- Buffered oscillator frequency measuring facility
- Internal suppression of Second Audio Program (SAP) distortion (5th harmonic of pilot)
- Suppression of Adjacent Channel Interference (ACI) distortion (3rd harmonic of sub carrier)
- Electronic hum filtering

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range (pin 8)	V_P	7,5	12	15	V
Supply current at V_P = 12 V	I_P	15	22	30	mA
D.C. output voltage range	$V_{15,\ 16\text{-}7}$	1	–	11	V
A.C. output voltage (r.m.s. value)	$V_{15,\ 16\text{-}7(rms)}$	–	1,25	–	
Voltage gain sub-signal	V_{15}/V_{sub}	–	13,5	–	dB
Voltage gain main signal	V_{16}/V_{main}	–	19,5	–	dB
Total harmonic distortion	THD	–	0,1	0,5	%
Operating ambient temperature range	T_{amb}	0	–	+70	°C
Storage temperature range	T_{stg}	–25	–	+150	°C

PACKAGE OUTLINE

18-lead dual in-line; plastic (SOT102).

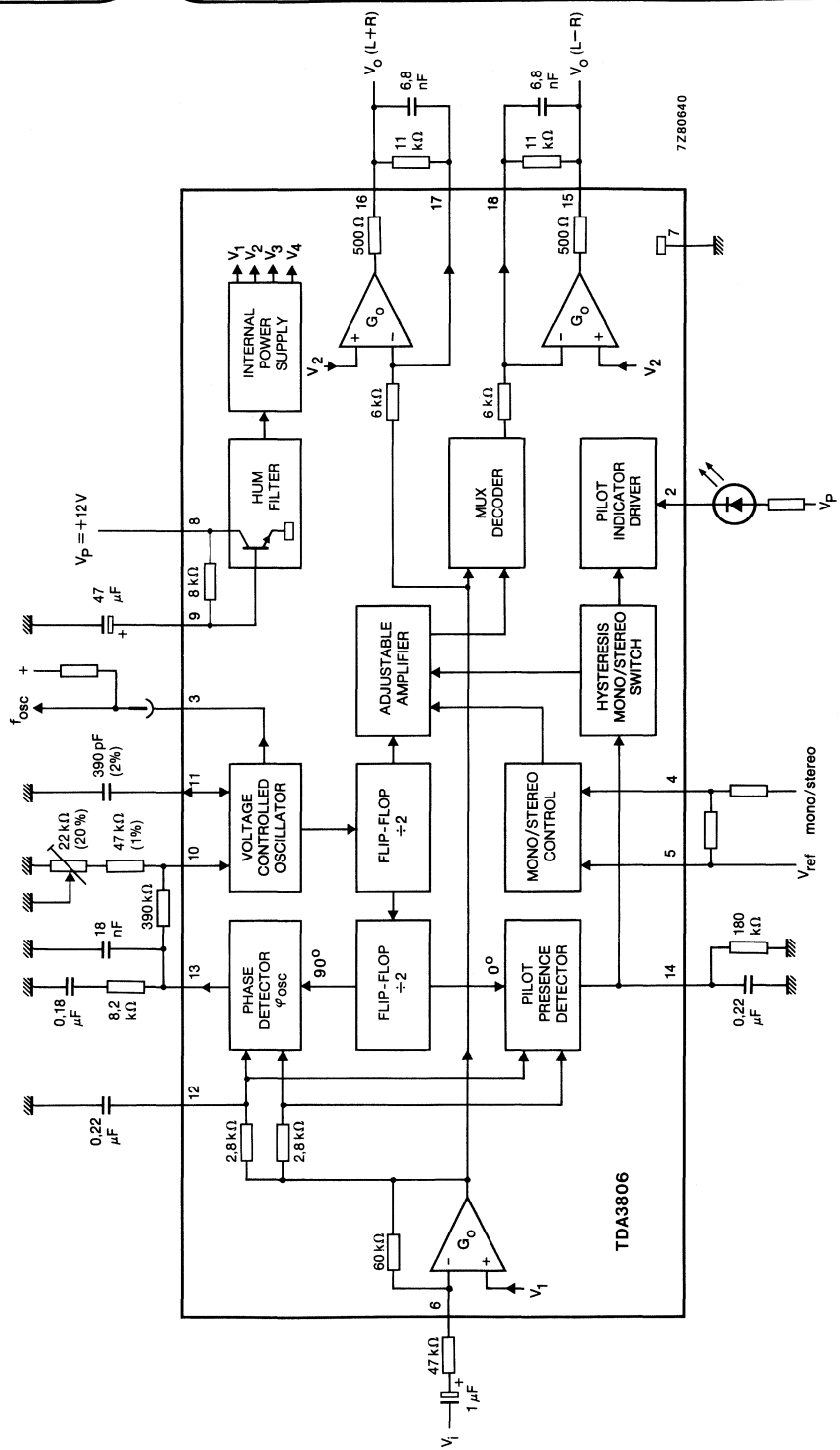


Fig. 1 Block diagram and test circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{8-7}	–	–	16	V
Input voltage (d.c.)	$V_{4,\ 5-7}$	0	–	12	V
Input voltage osc. frequency	V_{3-7}	0	–	V_P	V
Indicator driver voltage	V_{2-7}	–	–	16	V
Indicator driver output current	I_2	–	–	20	mA
Total power dissipation at T_{amb} = 25 °C (see Fig. 2)	P_{tot}	–	–	1200	mW
Storage temperature	T_{stg}	−25	–	+150	°C
Operating ambient temperature	T_{amb}	0	–	+70	°C

D.C. CHARACTERISTICS

Supply voltage (V_P) = 12 V; T_{amb} = 25 °C; unless otherwise specified.
See Fig. 1.

parameter	symbol	min.	typ.	max.	unit
Supply voltage range V_P	V_{8-7}	7,5	12	15	V
Supply current without indicator current	I_8	15	22	30	mA
Bias input voltage	V_{6-7}	–	5	–	V
Bias voltage output stages	$V_{17,\ 18-7}$	–	6,7	–	V
Offset current via ext. feedback resistors	I_{17-16} I_{18-15}	–	30	–	μA
Output voltage range	$V_{15,\ 16-7}$	1	–	V_P−1	V
Oscillator frequency voltage range	V_{3-7}	0	–	12	V
Voltage range M/St control	V_{4-7}	0	–	4	V
Reference voltage	V_{5-7}	0	–	4	V
Saturation voltage pilot indicator; I_2 = 20 mA	$V_{2-7(sat)}$	–	0,5	–	V

A.C. CHARACTERISTICS

Multiplex input voltage $V_{6-7(p-p)}$ = 0,85 V inclusive 9 % pilot
(m = 100 % ≙ Δf = ±55 kHz, f_{mod} = 1 kHz), circuit as Fig. 1, unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Input impedance (to be selected)	R_i	–	47	–	kΩ
Output current	$\pm I_{15,16}$	–	4	–	mA
Output voltage (r.m.s. value)	$V_{15,\ 16-7(rms)}$	–	1,25	–	V
Voltage gain sub-signal					
sub-signal	V_{out15}/V_{sub}	–	13,5	–	dB
main signal	V_{out16}/V_{main}	–	19,5	–	dB

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Difference of gain	G_{16}/G_{15}	5	6	7	dB
Total harmonic distortion $V_{15, 16-7}$ = 1,25 V	THD	–	0,1	0,5	%
Electronic hum filter					
Ripple rejection $V_{P\ ripple(rms)}$ = 200 mV f = 100 Hz	RR	32	35	–	dB
Carrier suppression V_o = 1,25 V pilot suppression					
1st harmonic	α 1	30	32	–	dB
2nd harmonic	α 2	40	50	–	dB
3rd harmonic	α 3	–	45	–	dB
4th harmonic	α 4	–	55	–	dB
Suppression of frequencies generated by interference SAP suppression	α_{SAP}	60	75	–	dB
Unweighted output noise voltage r.m.s. value, b = 20 Hz to 16 kHz	$V_{N(15)}$	–	30	–	μV
	$V_{N(16)}$	–	50	–	μV
Weighted output noise voltage according to CCIR 468; peak value	$V_{N(15)}$	–	90	–	μV
	$V_{N(16)}$	–	150	–	μV
Voltage controlled oscillator (VCO)					
Nominal frequency *	f_{osc}	–	63,4	–	kHz
Capture range	$\pm\Delta f/f$	2	–	–	%
Temperature coefficient	$\pm TK_{osc}$	–	1	–	10^{-4}/K
Mono-stereo switch					
Pilot threshold "stereo on" voltage (peak-to-peak)	$V_{pilot\ on}$	–	–	50	mV
Pilot threshold "stereo off" voltage (peak-to-peak)	$V_{pilot\ off}$	8	–	–	mV
Hysteresis	α	–	2,5	–	dB

* The oscillator frequency can be measured at pin 3 (low impedance output), when a resistor of 10 kΩ is switched from pin 3 to the supply voltage ($V_{3-7} > 6$ V).

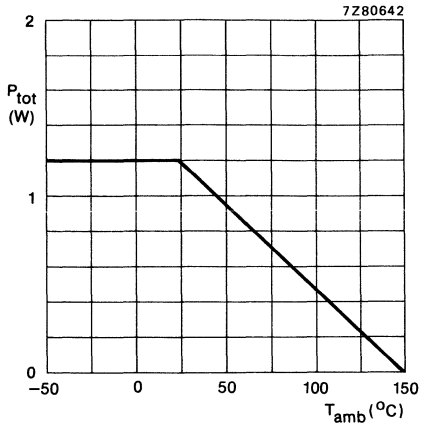


Fig. 2 Power derating curve.

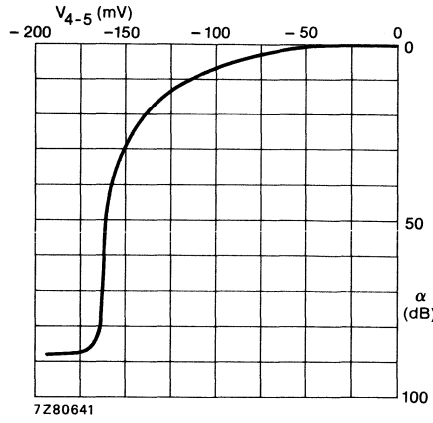


Fig. 3 Sub-signal attenuation as a function of the control voltage (V_{4-5}).

DEVELOPMENT DATA

SECOND AUDIO PROGRAMME (SAP) SIGNAL PROCESSOR

GENERAL DESCRIPTION

The circuit provides amplification, limiting, demodulation, indication and "no-signal" muting for processing the SAP facility of the multi-channel television sound system.
The main selectivity is done by a four pole bandpass filter in front of the integrated circuit.

Features

- Selective amplifier
- Limiter
- Phase demodulator
- Level detector

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_P	1,8	–	6,0	V
Supply current at V_P = 4,5 V	I_P	–	7	–	mA
Signal handling (e.m.f.)	V_i	–	200	–	mV
A.F. output voltage	V_o	–	160	–	mV

PACKAGE OUTLINE

16-lead dual in-line; plastic (SOT38).

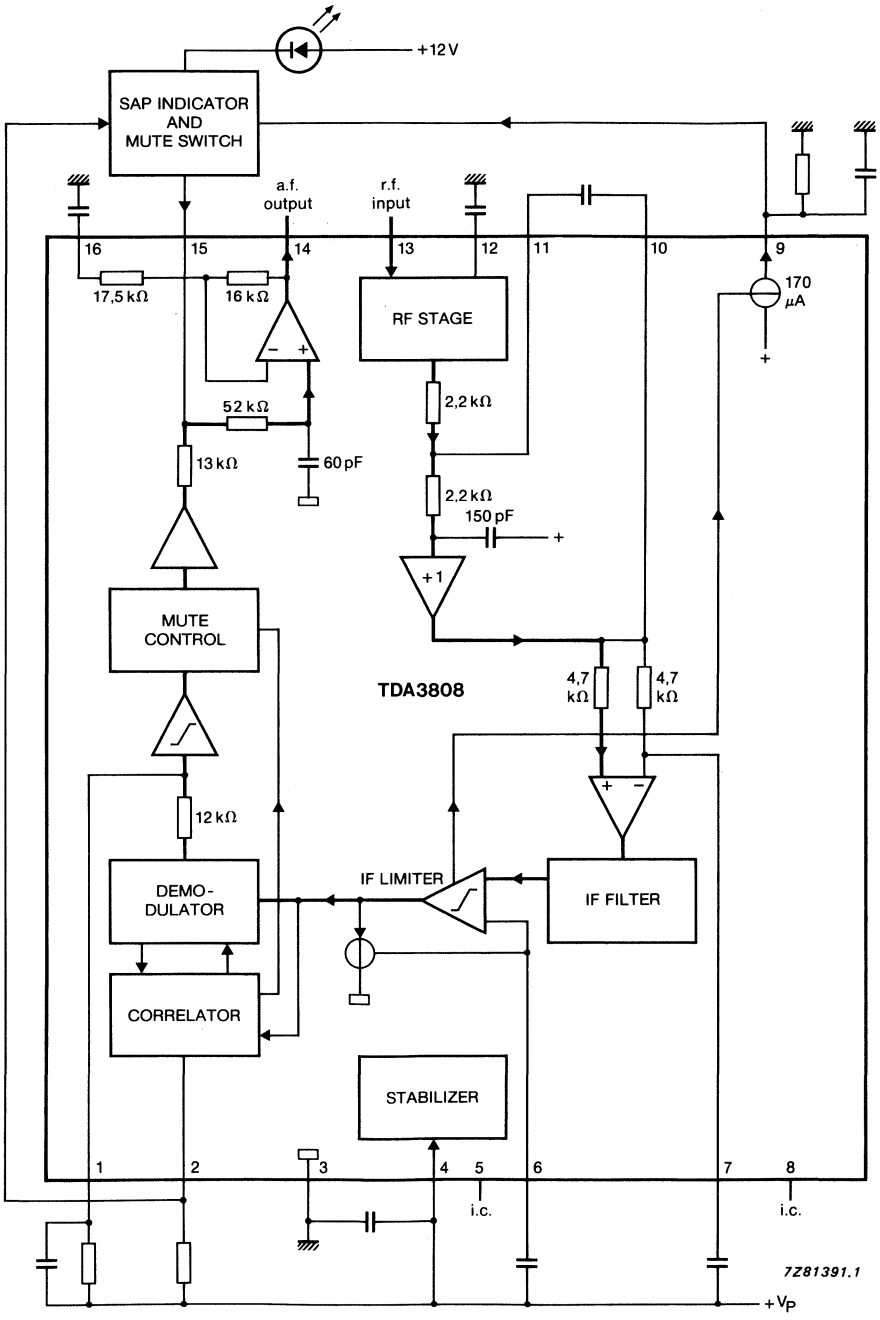


Fig. 1 Block diagram.

Pins 5 and 8 are internally connected and no external loading is permitted.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_P	–	–	7	V
Storage temperature	T_{stg}	−55	–	+ 150	°C
Operating ambient temperature range	T_{amb}	0	–	+ 70	°C

THERMAL RESISTANCE

from crystal to ambient	$R_{th\ c\text{-}a}$	–	75	–	K/W

D.C. CHARACTERISTICS

V_P = 4,5 V; T_{amb} = 25 °C; measured in Fig. 2 unless otherwise specified

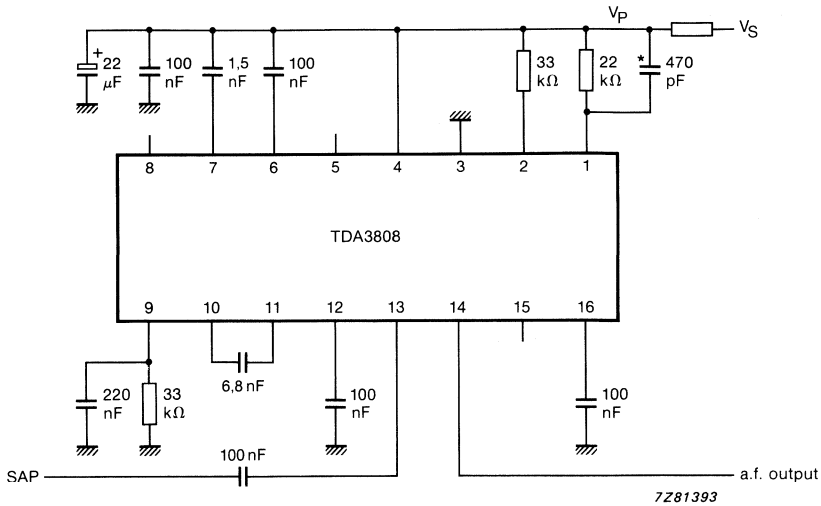
parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_P	1,8	–	6	V
Supply current					
V_P = 3 V	I_P	–	6,3	–	mA
R.F. input voltage	$V_{13\text{-}3}$	–	0,9	–	V
Output voltage	$V_{14\text{-}3}$	–	1,3	–	V
Output current					
maximum d.c. load	I_{14}	−100	–	+ 100	μA
maximum a.c. load	I_{14}	−3	–	+ 3	mA

A.C. CHARACTERISTICS

V_P = 4,5 V; T_{amb} = 25 °C; measured in Fig. 4; f_{rf} = 78,67 kHz modulated with Δf = ± 10 kHz; f_m = 0,4 kHz; V_i = 4 mV (e.m.f. at a source impedance of 75 Ω); r.m.s. noise voltage measured unweighted in the range f = 300 Hz to 20 kHz; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Input voltage					
for indication start (f_{rf} = 78,67 kHz)	V_i	–	320	–	μV
A.F. output voltage	$V_o = V_{14\text{-}3}$	–	160	–	mV
Signal to noise ratio	S/(S+N)	–	60	–	dB
AM suppression	∝	–	56	–	dB
Total harmonic distortion	THD	–	1,1	–	%
A.F. bandwidth	B	–	9	–	kHz
Noise level					
V_{ref} = 4 mV; V_i < 1 μV	N	–	58	–	dB

DEVELOPMENT DATA



* 6,8 nF for 75 µs de-emphasis

Fig. 2 Test circuit.

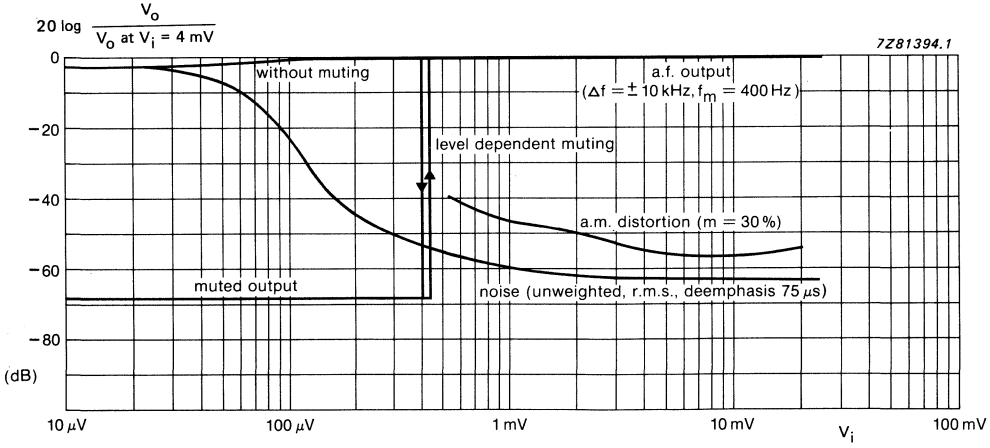


Fig. 3 Signal performance of TDA3808.

DEVELOPMENT DATA

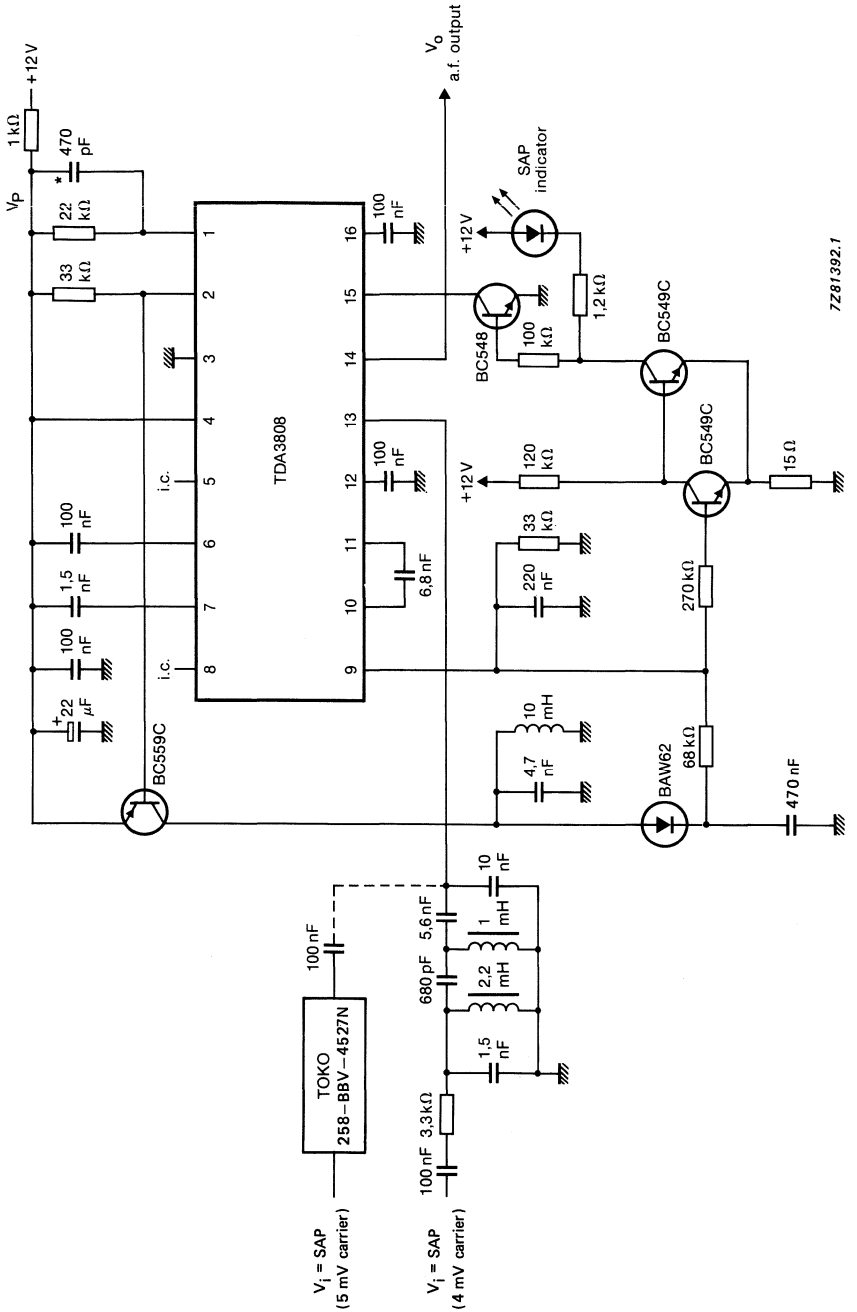


Fig. 4 Application diagram.

* 6,8 nF for 75 µs de-emphasis

SPATIAL, STEREO AND PSEUDO-STEREO SOUND CIRCUIT

The TDA3810 integrated circuit provides spatial, stereo and pseudo-stereo sound for radio and television equipment.

Features

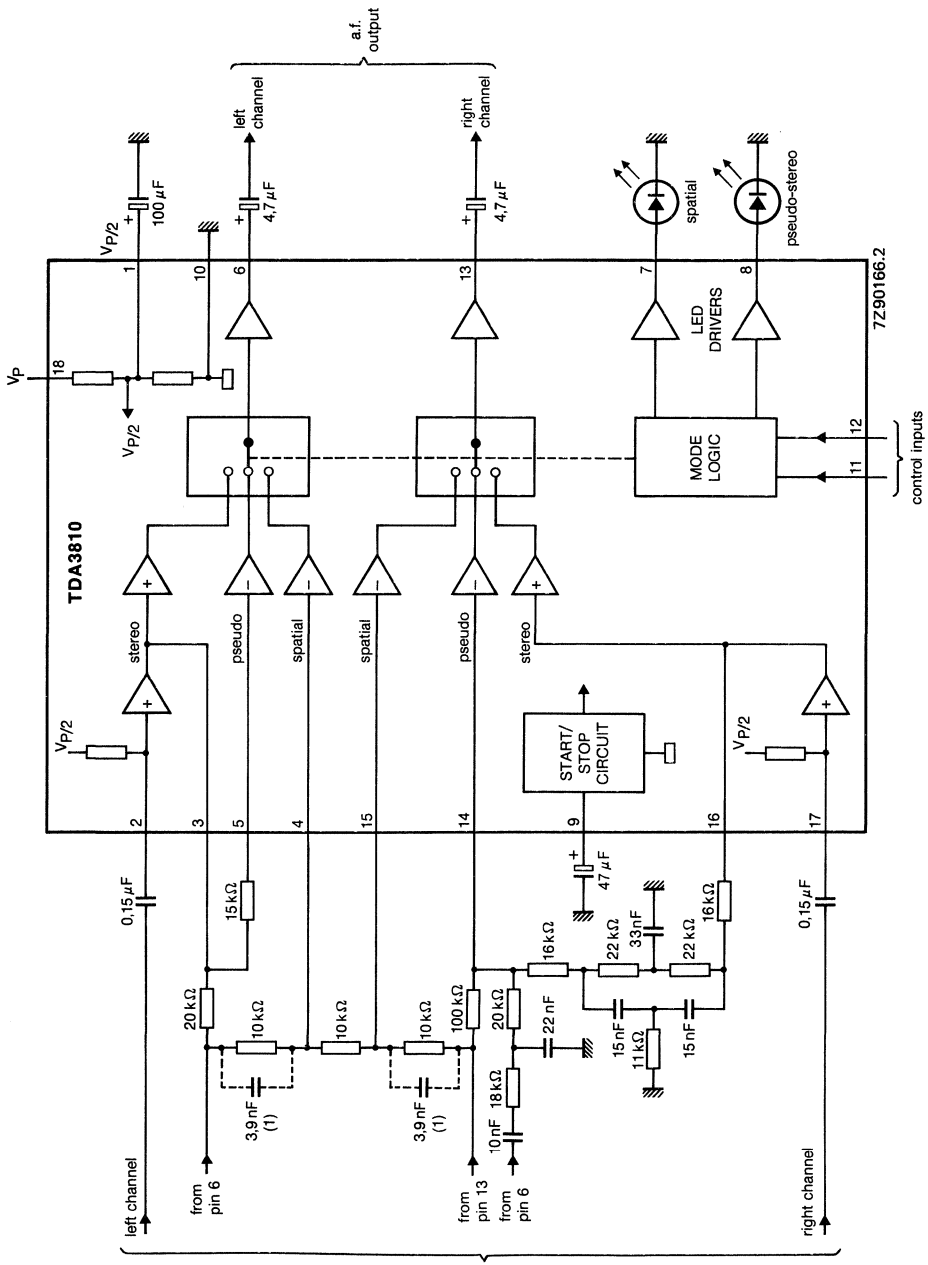
- Three switched functions: spatial (widened stereo image)
  stereo
  pseudo-stereo (artificial stereo from a mono source)
- Offset compensated operational amplifiers to reduce switch noise
- LED driver outputs to facilitate indication of selected operating mode
- Start/stop circuit to reduce switch noise and to prevent LED-flicker
- TTL-compatible control inputs

QUICK REFERENCE DATA

Supply voltage (pin 18)	V_P	typ.	12	V
Supply current (LEDs off)	I_P	typ.	6	mA
Operating ambient temperature range	T_{amb}	0 to	+ 70	°C
Input signal (r.m.s. value)	$V_{i(rms)}$	<	2	V
Total harmonic distortion (stereo)	THD	typ.	0,1	%
Channel separation (stereo)	α	typ.	70	dB
Gain (stereo)	G_v	typ.	0	dB

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



(1) Used in spatial mode for correction of high frequency only (optimal performance).

Fig. 1 Block diagram/test circuit showing external components; for control inputs to pins 11 and 12 see truth table.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 18)	V_P	max.	18 V
Storage temperature range	T_{stg}	−25 to + 150	°C
Operating ambient temperature range	T_{amb}	0 to + 70	°C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\ cr\text{-}a}$	=	80 K/W

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; test circuit Fig. 1 stereo mode (pin 11 to ground) unless otherwise specified. Output load: $R_{6\text{-}10,13\text{-}10} \geqslant 4{,}7$ kΩ; $C_{6\text{-}10,13\text{-}10} \leqslant 150$ pF.

parameter	symbol	min.	typ.	max.	unit
Supply voltage range (pin 18)	V_P	4,5	–	16,5	V
Supply current	I_P	–	6	12	mA
Reference voltage	V_S	5,3	6	6,7	V
Input voltage (pin 2 or 17) THD = 0,2% (stereo mode)	$V_{i(rms)}$	–	–	2	V
Input resistance (pin 2 or 17)	R_i	50	75	–	kΩ
Voltage gain V_o/V_i	G_v	–	0	–	dB
Channel separation (R/L)	α	60	70	–	dB
Total harmonic distortion f = 40 to 16 000 Hz; $V_{o(rms)}$ = 1 V	THD	–	0,1	–	%
Power supply ripple rejection	RR	–	50	–	dB
Noise output voltage (unweighted) left and right output	$V_{n(rms)}$	–	10	–	μV
SPATIAL MODE (pins 11 and 12 HIGH) Antiphase crosstalk	α	–	50	–	%
Voltage gain	G_v	1,4	2,4	3,4	dB

PSEUDO-STEREO MODE

The quality and strength of the pseudo-stereo effect is determined by external filter components.

parameter	symbol	min.	typ.	max.	unit
CONTROL INPUTS (pins 11 and 12)					
Input resistance	R_i	70	120	–	kΩ
Switching current	$-I_i$	–	35	100	μA
LED DRIVERS (pins 7 and 8)					
Output current for LED	$-I_o$	10	12	15	mA
Forward voltage	V_F	–	–	6	V

Truth table

mode	control input state		LED spatial pin 7	LED pseudo pin 8
	pin 11	pin 12		
Mono pseudo-stereo	HIGH	LOW	off	on
Spatial stereo	HIGH	HIGH	on	off
Stereo	LOW	X	off	off

LOW = 0 to 0,8 V (the less positive voltage)
HIGH = 2 V to 5,5 V (the more positive voltage)
X = don't care

SINGLE FM TV-SOUND DEMODULATOR CIRCUIT

GENERAL DESCRIPTION

The TDA3825 is a single FM demodulator system with external AF input and mute.

Features

- Supply voltage range from 4.5 V to 13.2 V
- AC coupled AF stage
- Multiple input AF operational amplifier with offset compensation
- External AF input
- High AF output voltage with low distortion
- AF gain of 0 dB without external components
- Frequency response can be determined by external components
- High ripple rejection
- Low switching noise between AF and mute

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 11)		V_P	4.5	5.0	13.2	V
Supply current (pin 11)						
	V_P = 5.0 V	I_P	–	16	–	mA
	V_P = 12 V	I_P	–	18	–	mA
FM demodulator						
AF output voltage (pin 5) (RMS value)	Δf = 50 kHz; Q_B = 11	V_{5-1}	–	0.5	–	V
Signal plus weighted-noise to weighted-noise ratio		(S + W)/W	65	70	–	dB
Total harmonic distortion		THD	–	0.3	0.5	%
Source selector						
AF output voltage (pin 12) (RMS value)	THD $\leqslant$ 0.1%; G_V = 6 dB	V_{12-1}	–	1.0	–	V

PACKAGE OUTLINE

14-lead DIL; plastic (SOT27).

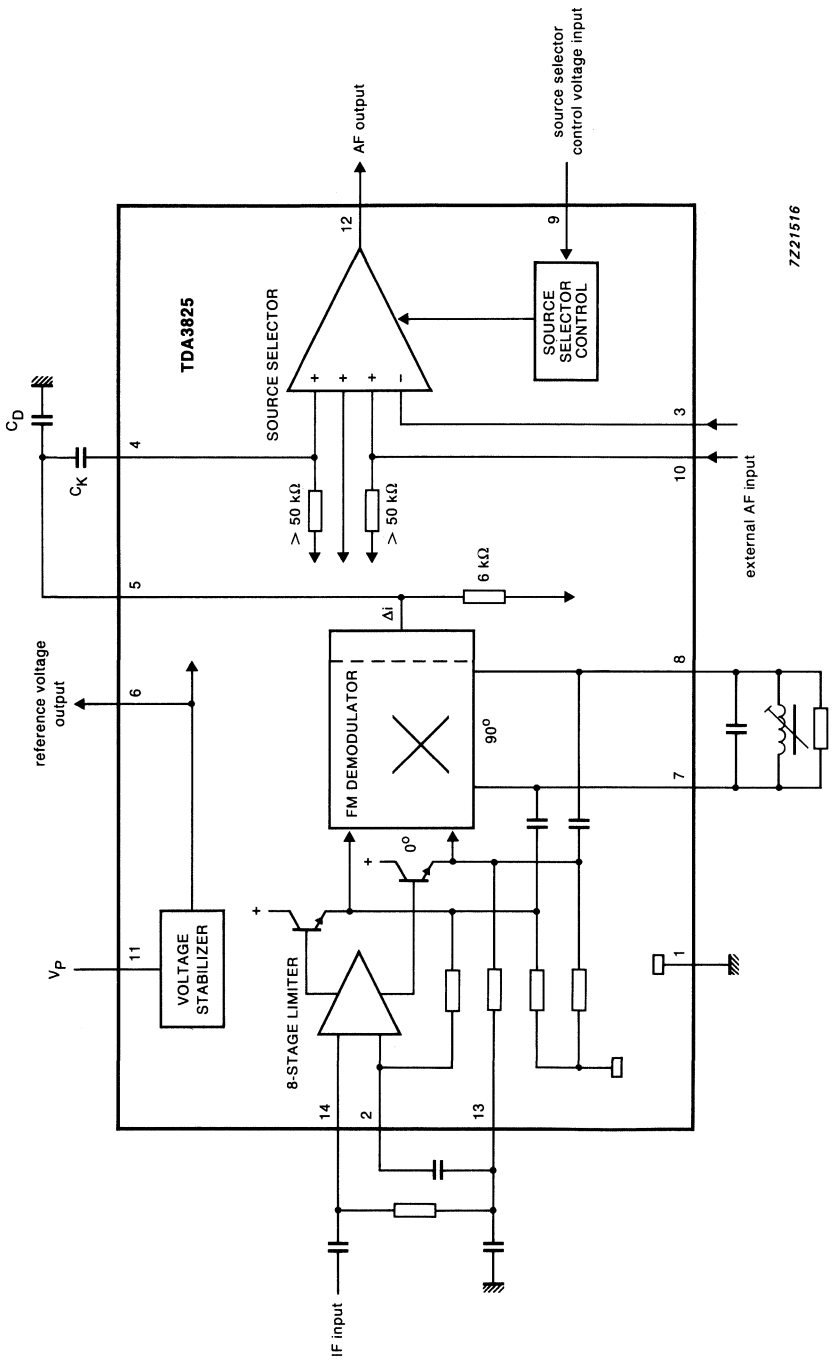


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 11)		V_P	4.5	13.2	V
External DC load resistance		R_L	5	–	kΩ
Total power dissipation		P_{tot}	–	400	mW
Storage temperature range		T_{stg}	−25	+125	°C
Operating ambient temperature range		T_{amb}	0	+70	°C

DEVELOPMENT DATA

CHARACTERISTICS

V_P = 5 V; T_{amb} = 25 °C; V_i = 10 mV; f_o = 5.5 MHz; f_{AF} = 1 kHz; Δf = 50 kHz; all parameters were measured with the test circuit of Fig. 2; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 11)		V_P	4.5	5.0	13.2	V
Total current consumption		I_{tot}	–	16	20	mA
Limiting amplifier						
Input voltage (pin 14) (RMS value)		V_{14-1}	–	–	200	mV
	3 dB signal reduction	V_{14-1}	–	–	50	μV
DC voltages						
pin 2		V_{2-1}	–	2	–	V
pin 13		V_{13-1}	–	2	–	V
pin 14		V_{14-1}	–	2	–	V
Input resistance		R_{14-13}	15	–	–	kΩ
Input capacitance		C_{14-13}	–	–	6	pF
FM demodulator						
DC voltages						
pin 7		V_{7-1}	–	3.2	–	V
pin 8		V_{8-1}	–	3.2	–	V
AF output voltage (pin 5) (RMS value)	Q_B = 11	V_{5-1}	–	0.5	–	V
AM suppression	f_{AM} = 400 Hz; m = 0.3; V_i = 500 μV(rms)	α_{AM}	50	–	–	dB
Total harmonic distortion		THD	–	0.3	0.5	%
Output impedance (pin 5)		$\lvert Z_{5-1}\rvert$	–	6	–	kΩ
Signal plus weighted-noise to weighted-noise ratio	in accordance with DIN4505; CCIR468-3	(S + W)/W	65	70	–	dB
Signal plus noise-to-noise ratio	B_{noise} = 20 kHz	(S + N)/N	75	80	–	dB
Residual RF signal (pin 5) (RMS value)	2 x f_o without de-emphasis	V_{5-1}	–	30	–	mV
Ripple rejection	f_R = 70 Hz, V_R = 100 mV(p-p)	α_R	40	45	–	dB

parameter	conditions	symbol	min.	typ.	max.	unit
Source selector (pin 12)						
Open loop gain		G_{ol}	50	60	–	dB
Noise output voltage (RMS value)	B_{noise} = 20 kHz	V_{12-1}	–	20	–	μV
Slew rate		$\frac{\Delta V_{12-1}}{\Delta t}$	2	–	–	V/μs
Maximum AF output voltage (RMS value)	THD ≤ 0.1%; G_v = 6 dB	V_{12-1}	1.1	–	–	V
Input impedance (pin 4)		$\|Z_{4-1}\|$	50	–	–	kΩ
(pin 10)		$\|Z_{10-1}\|$	50	–	–	kΩ
−1 dB small signal bandwidth		B_{af}	100	–	–	kHz
DC output current		I_{12}	–	–	1	mA
Output load capacitance		C_L	–	–	500	pF
Feedback resistor (pin 3 to pin 6)		R_{3-6}	–	–	10	kΩ
(pin 3 to pin 12)		R_{3-12}	0	–	–	Ω
DC output voltage		V_{12-1}	–	2.27	–	V
AF suppression for mute		α_{mute}	70	76	–	dB
Crosstalk attenuation		$\alpha_{4/10}$	64	70	–	dB
Offset voltage between any two source selector positions		V_{12-6}	–	–	50	mV
Source selector control	see Fig.3					
Source coltrol voltage (pin 9)						
Mute active input voltage		V_{9-1}	0	–	1/3 V_P−1	V
input current		I_9	10	–	500	μA
Input 1 active (pin 4) input voltage		V_{9-1}	1/3 V_P	–	2/3 V_P−0.7	V
input current		I_9	−200	–	+200	μA
Input 2 active (pin 10) input voltage		V_{9-1}	2/3 V_P + 0.7	–	V_P	V
input current		I_9	−600	–	−40	μA
Input voltage at pin 9 for I_9 = 0 μA		V_{9-1}	–	$\frac{V_P-0.7}{2}$	–	V
Reference source (pin 6)						
Reference voltage input		V_{ref}	2.17	2.27	2.37	V
Output current		$\|I_6\|$	–	250	–	μA

DEVELOPMENT DATA

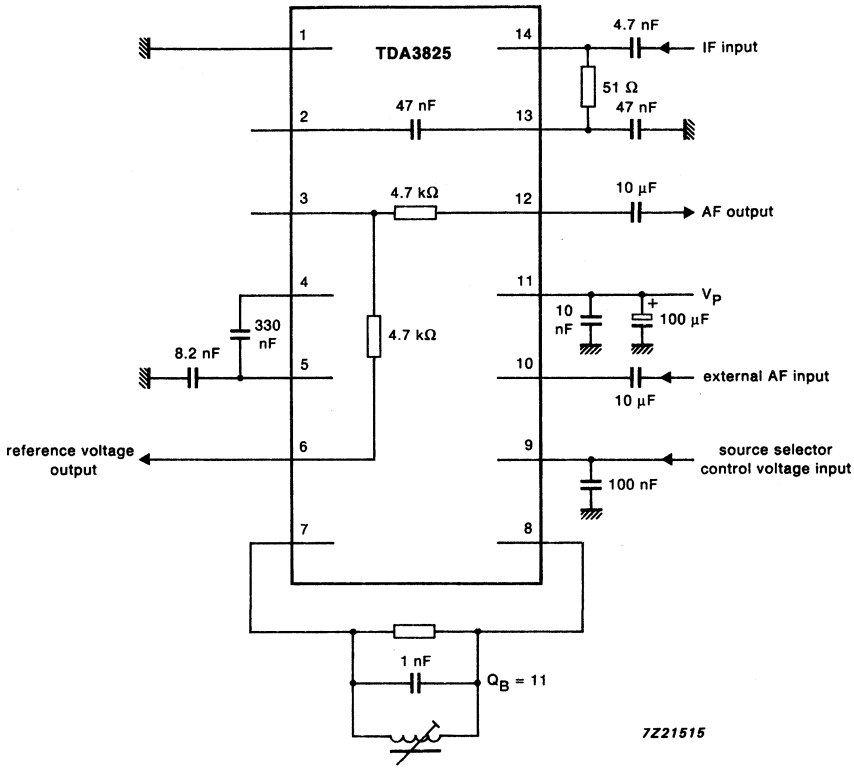


Fig. 2 Test circuit.

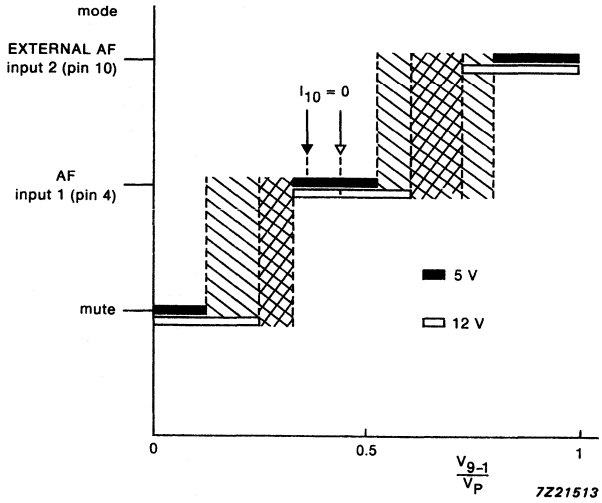


Fig. 3 Source selector logic diagram.

DEVELOPMENT DATA

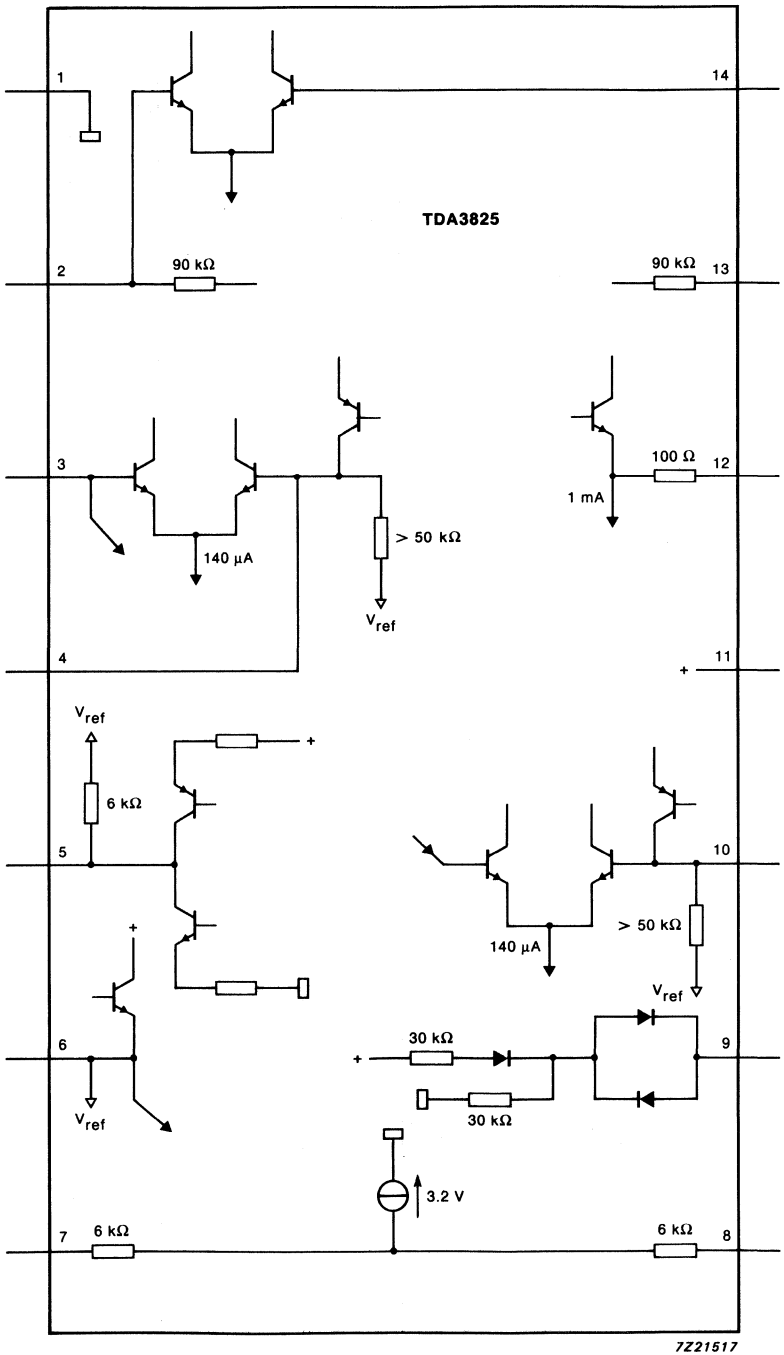


Fig. 4 Input/output loading diagram.

APPLICATION INFORMATION

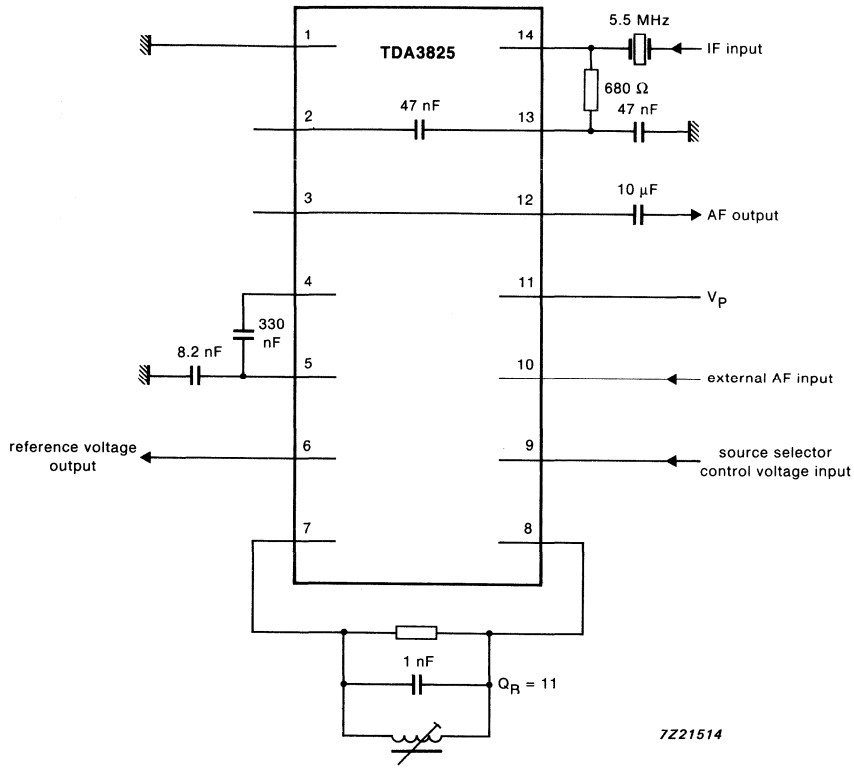


Fig. 5 Application diagram.

DEVELOPMENT DATA

SINGLE FM TV-SOUND DEMODULATOR CIRCUIT

GENERAL DESCRIPTION

The TDA3826 is a single FM demodulator system with mute and 6 dB AF amplifier.

Features

- Supply voltage range from 4.5 V to 13.2 V
- AC coupled AF stage
- AF operational amplifier output with offset compensated input stage
- High AF output voltage with low distortion
- High ripple rejection
- Low switching noise between AF and mute

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 11)		V_P	4.5	5.0	13.2	V
Supply current (pin 11)						
	V_P = 5.0 V	I_P	–	16	–	mA
	V_P = 12 V	I_P	–	18	–	mA
FM demodulator						
AF output voltage (pin 5) (RMS value)	Δf = 50 kHz; Q_B = 11	V_{5-1}	–	0.5	–	V
Signal plus weighted-noise to weighted-noise ratio		(S + W)/W	65	70	–	dB
Total harmonic distortion		THD	–	0.3	–	%
AF switch						
AF output voltage (pin 12) (RMS value)	THD $\leqslant$ 0.1%; G_V = 6 dB	V_{12-1}	–	1.0	–	V

PACKAGE OUTLINE

14-lead DIL; plastic (SOT27).

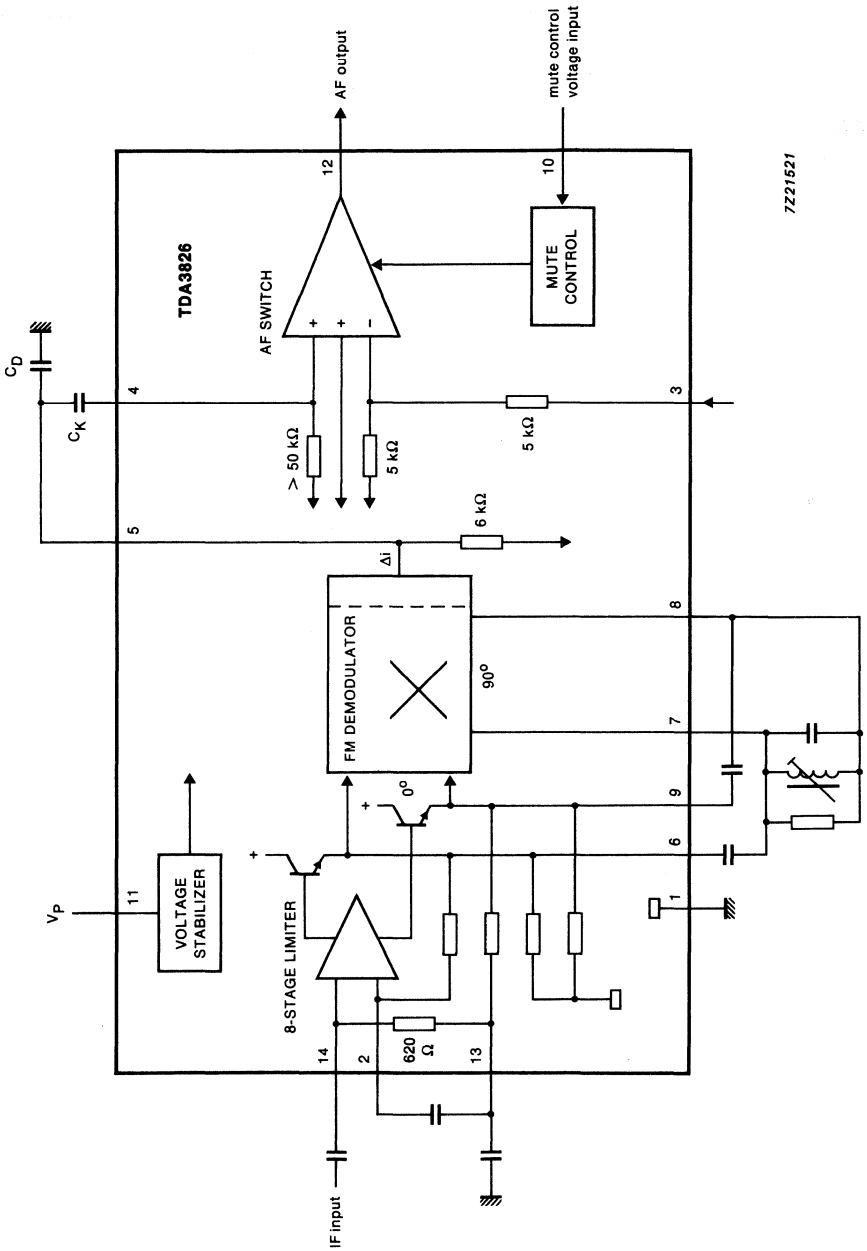


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 11)		V_P	4.5	13.2	V
External DC load resistance		R_L	5	–	kΩ
Total power dissipation		P_{tot}	–	400	mW
Storage temperature range		T_{stg}	−25	+125	°C
Operating ambient temperature range		T_{amb}	0	+70	°C

DEVELOPMENT DATA

CHARACTERISTICS

V_P = 5 V; T_{amb} = 25 °C; V_i = 10 mV; f_o = 5.5 MHz; f_{AF} = 1 kHz; Δf = 50 kHz; all parameters were measured with the test circuit of Fig. 2; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 11)		V_P	4.5	5.0	13.2	V
Total current consumption		I_{tot}	–	16	20	mA
Limiting amplifier						
Input voltage (pin 14) (RMS value)		V_{14-1}	–	–	200	mV
	3 dB signal reduction	V_{14-1}	–	–	50	μV
DC voltages						
pin 2		V_{2-1}	–	2	–	V
pin 13		V_{13-1}	–	2	–	V
pin 14		V_{14-1}	–	2	–	V
Input resistance		R_{14-13}	–	620	–	Ω
FM demodulator						
DC voltages						
pin 7		V_{7-1}	–	3.2	–	V
pin 8		V_{8-1}	–	3.2	–	V
AF output voltage (pin 5) (RMS value)	Q_B = 11	V_{5-1}	–	0.5	–	V
AM suppression	f_{AM} = 400 Hz; m = 0.3; V_i = 500 μV(rms)	α_{AM}	50	–	–	dB
Total harmonic distortion		THD	–	0.3	–	%
Output impedance (pin 5)		$\lvert Z_{5-1}\rvert$	–	6	–	kΩ
Signal plus weighted-noise to weighted-noise ratio	in accordance with DIN4505; CCIR468-3	(S + W)/W	65	70	–	dB
Signal plus noise-to-noise ratio	B_{noise} = 20 kHz	(S + N)/N	75	80	–	dB
Residual RF signal (pin 5) (RMS value)	2 x f_o without de-emphasis	V_{5-1}	–	30	–	mV
Ripple rejection	f_R = 70 Hz; V_R = 100 mV(p-p)	α_R	40	45	–	dB

parameter	conditions	symbol	min.	typ.	max.	unit
AF switch (pin 12)						
Open loop gain		G_{ol}	50	60	–	dB
Noise output voltage (RMS value)	B_{noise} = 20 kHz	V_{12-1}	–	20	–	μV
Slew rate		$\frac{\Delta V_{12-1}}{\Delta t}$	2	–	–	V/μs
Maximum AF output voltage (RMS value)	THD ⩽ 0.1%; G_v = 6 dB	V_{12-1}	1.1	–	–	V
Input impedance (pin 4)		$\|Z_{4-1}\|$	50	–	–	kΩ
(pin 10)		$\|Z_{10-1}\|$	50	–	–	kΩ
−1 dB small signal bandwidth		B_{af}	100	–	–	kHz
DC output current		I_{12}	–	–	1	mA
Output load capacitance		C_L	–	–	500	pF
Feedback resistor (pin 3 to pin 12)		R_{3-12}	0	–	–	Ω
DC output voltage		V_{12-1}	–	2.27	–	V
AF suppression in case of mute		α_{mute}	70	76	–	dB
Mute control	see Fig. 3					
Mute control voltage (pin 10)						
Input (pin 4) active						
input voltage		V_{10-1}	1/3 V_P	–	2/3 V_P−0.7	V
input current		I_{10}	−200	–	+200	μA
Mute active						
input voltage		V_{10-1}	0	–	1/3 V_P−1	V
input current		I_{10}	10	–	500	μA
input voltage		V_{10-1}	2/3 V_P + 0.7	–	V_P	V
input current		I_{10}	−600	–	−40	μA
Input voltage at pin 10 for I_{10} = 0 μA		V_{10-1}	–	$\frac{V_p-0.7}{2}$	–	V

DEVELOPMENT DATA

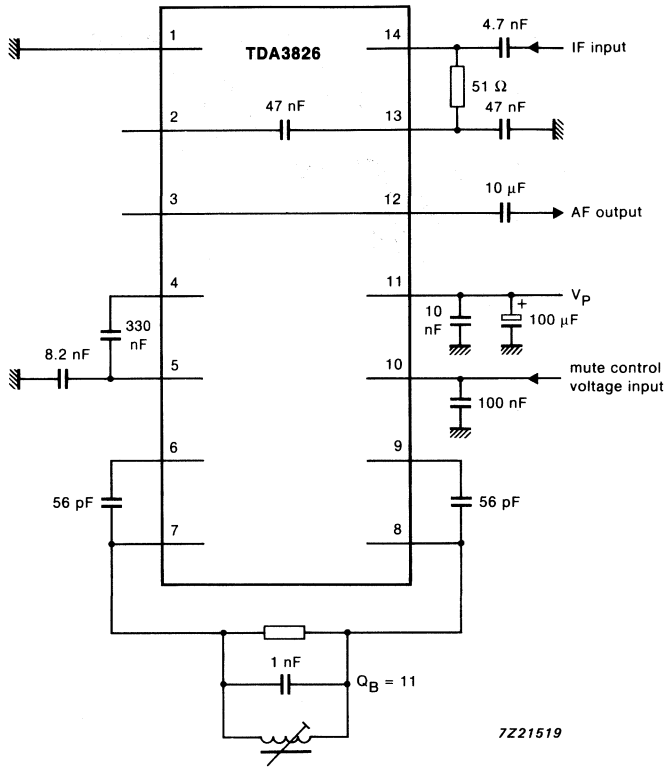


Fig. 2 Test circuit.

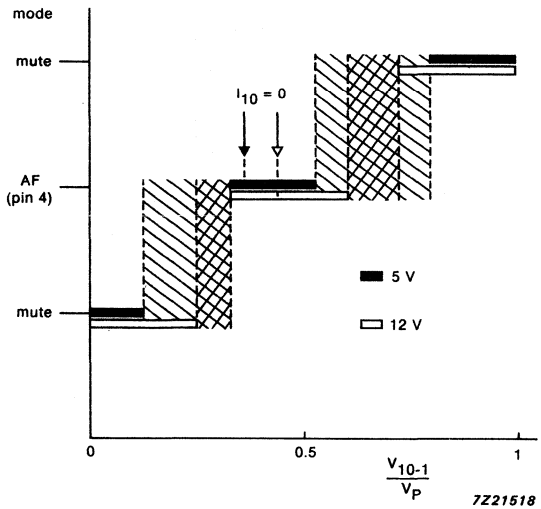


Fig. 3 Mute control logic diagram.

DEVELOPMENT DATA

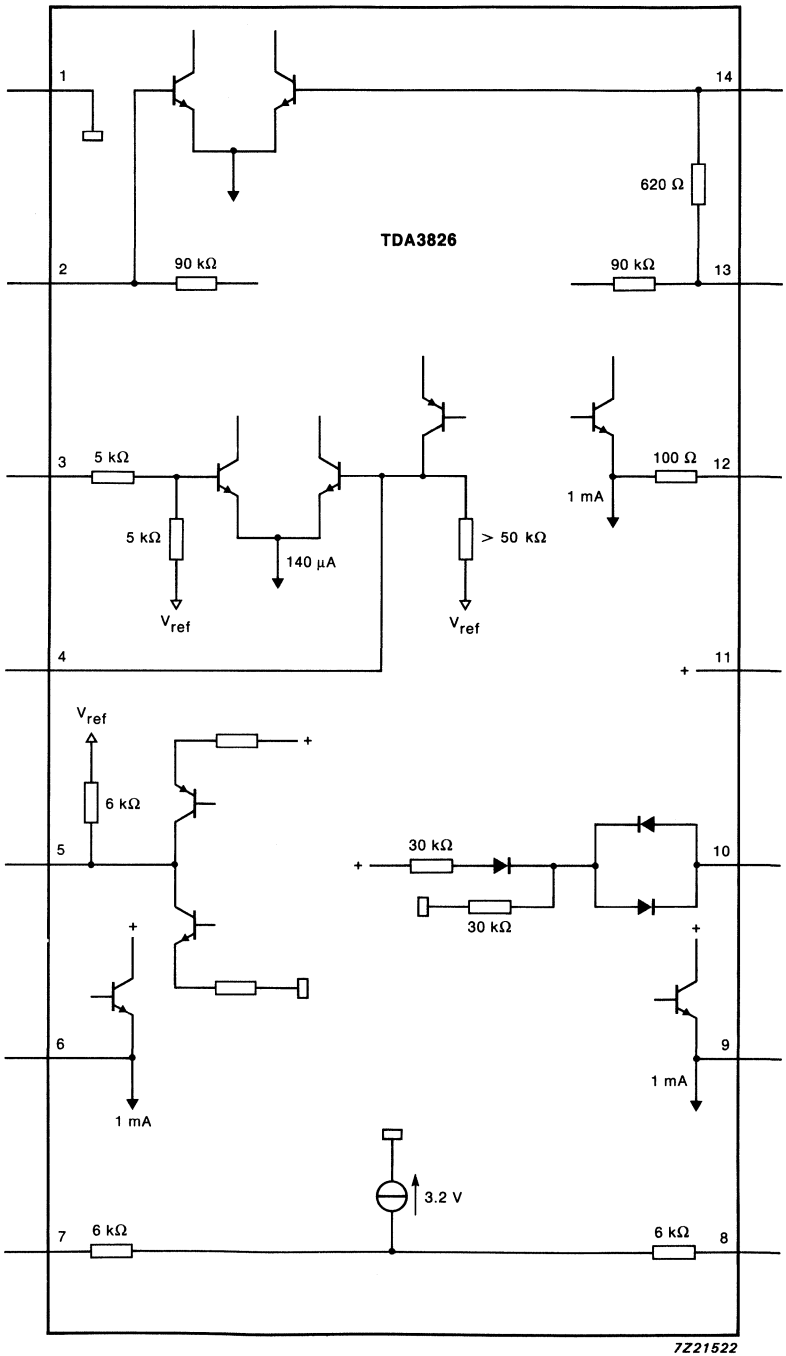


Fig. 4 Input/output loading diagram.

APPLICATION INFORMATION

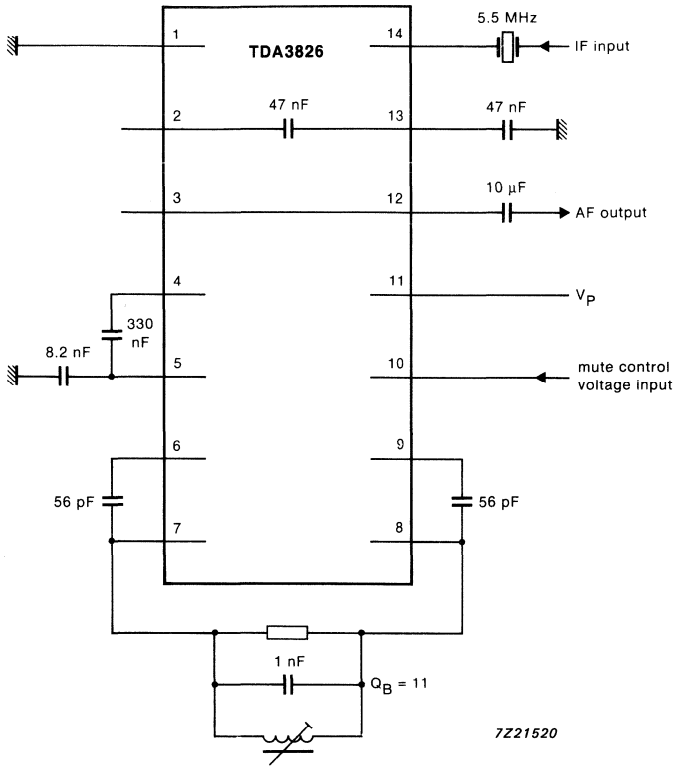


Fig. 5 Application diagram.

DEVELOPMENT DATA

QUASI-SPLIT-SOUND CIRCUIT AND AM DEMODULATOR

The TDA3845 is a quasi-split-sound IF circuit which is designed to give high performance television FM/AM sound.

Features

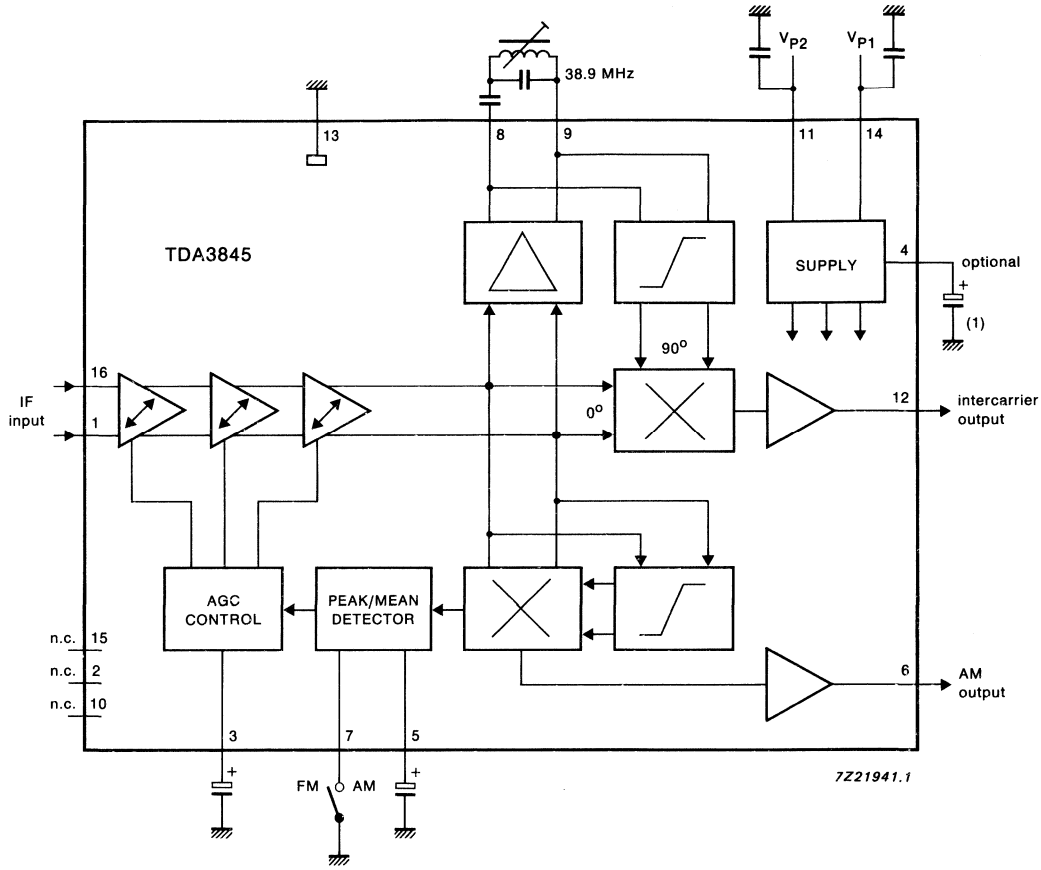
- Power supply from 5 V (200 mW) to 8 V source as well as an alternative 12 V source
- Gain controlled wideband IF amplifier (AC coupled with three stages)
- High precision internal 90° phase shifter for quadrature demodulator
- Amplitude detector for gain control which operates as a peak detector for FM sound and as a mean level detector for AM sound (switchable)
- Inphase wideband synchronous demodulator for AM detection
- Stabilizer circuit for ripple rejection and constant output signals
- ESD protection for all pins
- Suitable for all FM standards and L standard
- NICAM compatible

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage pin 14 or pin 11		 V_{P1} V_{P2}	 4.5 10.8	 5.0 12.0	 8.8 13.2	 V V
Supply current		I_P	–	40	–	mA
Minimum IF input voltage (RMS value)		$V_{1\text{-}16(rms)}$	–	70	100	μV
IF control range			60	63	–	dB
Intercarrier output voltage 5.5 MHz (RMS value)		$V_{12\text{-}13(rms)}$	70	100	–	mV
Signal-to-weighted-noise ratio (relative to 1 kHz; 50 kHz deviation)						
at 5.5 MHz for 2T/20T		(S + W)/W	–	60	–	dB
at 5.742 MHz for 2T/20T		(S + W)/W	–	58	–	dB
AF output voltage AM (RMS value)		$V_{6\text{-}13(rms)}$	440	550	660	mV
Signal-to-weighted-noise ratio; AM mode		(S + W)/W	–	56	–	dB
Total harmonic distortion (AM mode)		THD	–	1	2	%

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).



(1) See note 10 to the characteristics.

Fig.1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
pin 14		V_{P1}	4.5	8.8	V
or pin 11		V_{P2}	10.8	13.2	V
Storage temperature range		T_{stg}	−25	+125	°C
Operating ambient temperature range		T_{amb}	0	+70	°C
Total power dissipation at V_{P2}		P_{tot}	−	635	mW

CHARACTERISTICS

T_{amb} = 25 °C; V_{P1} = 5 V (see note 11); all measurements are with respect to ground (pin 13) unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage						
pin 14		V_{P1}	4.5	5.0	8.8	V
or pin 11		V_{P2}	10.8	12.0	13.2	V
Total current consumption		I_{tot}	−	40	48	mA
IF amplifier						
Input resistance		$R_{1\text{-}16}$	−	2	−	kΩ
Input capacitance		$C_{1\text{-}16}$	−	2.5	−	pF
Minimum IF input voltage (RMS value)	note 1	$V_{1\text{-}16(rms)}$	−	70	100	μV
Maximum IF input voltage (RMS value)	note 2	$V_{1\text{-}16(rms)}$	70	100	−	mV
Gain control range		ΔG	60	63	−	dB
Gain control voltage range		$G_{v3\text{-}16}$	1.5	−	3.0	V
IF bandwidth	−3 dB	B_{IF}	50	70	−	MHz
DC potential		$V_{1\text{-}16}$	−	1.7	−	V

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Intercarrier mode (FM mode; standard B/G)	notes 3, 4 and 5					
Reference amplifier						
Picture carrier amplitude (peak-to-peak value)		$V_{8\text{-}9(p\text{-}p)}$	–	270	–	mV
Operating resistance		$R_{8\text{-}9}$	–	4	–	kΩ
DC potential		$V_{8\text{-}9}$	–	3.9	–	V
Intercarrier mixer and output stage						
Output signal (RMS value) at 5.5 MHz		$V_{12(rms)}$	70	100	–	mV
at 5.74 MHz		$V_{12(rms)}$	32	45	–	mV
Intercarrier bandwidth at −1 dB		B_{12}	–	8	–	MHz
at −3 dB		B_{12}	–	9	–	MHz
Residual video AM on intercarrier signal	note 6		–	3	10	%
Output resistance		R_{12}	–	30	–	Ω
DC potential		V_{12}	–	1,8	–	V
Allowable AC output current (peak value)	note 7	$\pm I_{12(peak)}$	–	–	0.7	mA
Allowable DC output current		$-I_{12}$	–	–	2	mA
AF signal performance	note 8					
Black picture		(S + W)/W	60/58	68/64	–	dB
2T/20T pulses with white bars		(S + W)/W	57/55	60/58	–	dB
6 kHz sinewave (black-to-white modulation)		(S + W)/W	53/51	57/55	–	dB
250 kHz square wave (black-to-white modulation)		(S + W)/W	50/44	56/50	–	dB
AM mode (standard L)	notes 4 and 9					
S/N weighted in accordance with CCIR 468-2						
AF output signal (RMS value)		$V_{6(rms)}$	440	550	660	mV
AF bandwidth	−3 dB; note 12	B_{AF}	0.02	–	120	kHz
Total harmonic distortion		THD	–	1	3	%

parameter	conditions	symbol	min.	typ.	max.	unit
Signal-to-weighted-noise	note 10	(S + W)/W	50	56	–	dB
DC potential		V_6	–	1.8	–	V
Output resistance		R_6	–	200	–	Ω
Allowable AC output current (peak value)	note 7	$\pm I_{6(peak)}$	–	–	0.3	mA
Allowable DC output current		$-I_6$	–	–	1	mA
Standard switch	note 4					
Peak signal AGC (FM mode)	V_{P1}	V_7	1.8	–	V_{P1}	V
or switch open-circuit	V_{P2}	V_7	1.8	–	5.5	V
Mean signal AGC (AM mode)		V_7	–	–	0.8	V
Switch current						
at 0 V		$-I_7$	–	–	200	μA
at V_{P1}		I_7	–	–	10	μA
at V_{P2} (via a 2.2 kΩ series resistor)		I_7	–	–	2.5	mA
Ripple rejection						
Voltage ripple < 200 mV (peak-to-peak value) at 70 Hz						
AM/AF signal						
αRR = voltage ripple on Vp/voltage ripple on output signal		αRR	30	40	–	dB
FM phase noise						
Δf_{rms} intercarrier signal		$\Delta f_{(rms)}$	–	10	20	Hz

DEVELOPMENT DATA

Notes to the characteristics

1. Start of gain control (LOW IF input signal) at –3 dB intercarrier signal reduction at pin 12, AGC mode set to FM or –3 dB AF signal reduction at pin 6, AGC mode set to AM.
2. End of gain control (HIGH IF input signal) at + 1 dB intercarrier signal expansion at pin 12, AGC mode set to FM or + 1 dB AF signal expansion at pin 6, AGC mode set to AM.
3. Picture carrier (38.9 MHz) to sound carriers (33.4 MHz/33.158 MHz) ratio: 13/20 dB.
   IF input signal (picture carrier at sync pulse); $V_{1\text{-}16}$ = 10 mV (RMS value), Transmitter mode: DSB.
   Reference for the (S + W)/W ratio (0 dB) corresponds to the sound modulation where f = 1 kHz and frequency deviation Δf = ± 50 kHz.
   With reduced frequency deviation Δf = ± 30 kHz and the (S + W)/W figures will decrease by 4.5 dB.
4. If the device is used only for the B/G standard (no AM), the capacitor at pin 5 can be omitted (pin 5 has to be disconnected). In this instance the AGC will always operate as a peak-signal AGC and is independent of the voltage at pin 7.

Notes to the characteristics (continued)

The AM mode can also be used for the B/G standard, consequently standard switching is not required. However, the intercarrier level depends on the video modulation and the AF performance may decrease.
When the IC is operated from a 12 V power supply pin 7 can be connected to a 12 V logic level via a 2.2 kΩ series resistor.

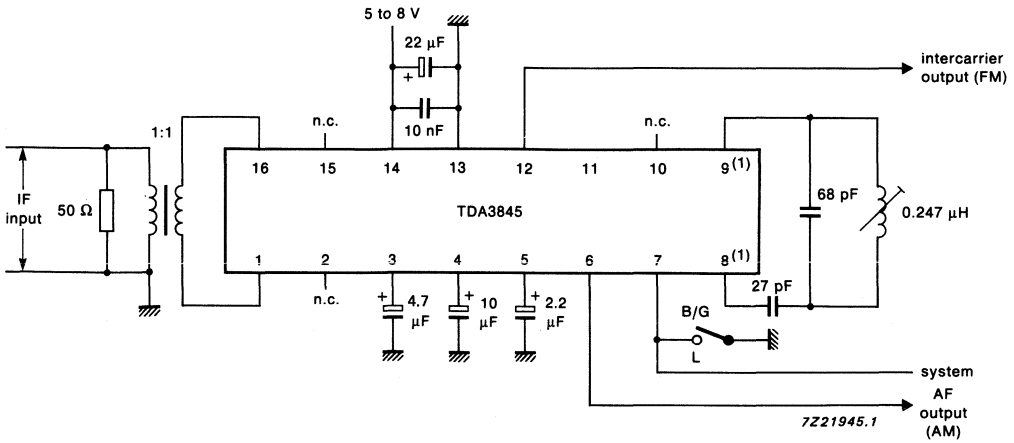
5. LC reference circuit for the picture carrier (pins 8 and 9); 68 pF//0.247 μH; in series with 27 pF: Q-loaded = 40 (Qo = 90); tuned to 38.9 MHz yields quadrature demodulation for the picture carrier which gives optimal video suppression at the intercarrier output (e.g. black-to-white jump of the video modulation).
The series capacitor provides a notch at the sound carrier frequency in order to produce more attenuation for the sound carrier in the PC reference channel. The ratio of parallel to series capacitance depends on the ratio of picture to sound carrier frequency which has to be adapted to other TV transmission standards, if required, in accordance with the formula:

$$C_S = C_P(F_{PC}/F_{SC})^2 - C_P$$

where:
C_S = series capacitor
C_P = parallel capacitor
F_{PC} = picture carrier frequency
F_{SC} = sound carrier frequency

The result is an improved 'intercarrier buzz' in the stereo system B/G, particularly with 250 kHz video modulation (up to 10 dB improvement in sound channel 2), or to suppress 350 kHz video modulated beat in the digitally modulated NICAM subcarrier.
In order to optimize the AF signal performance, fine tuning to the optimal S/W at the sound channel 2 may be achieved by a 250 kHz video modulated squarewave.

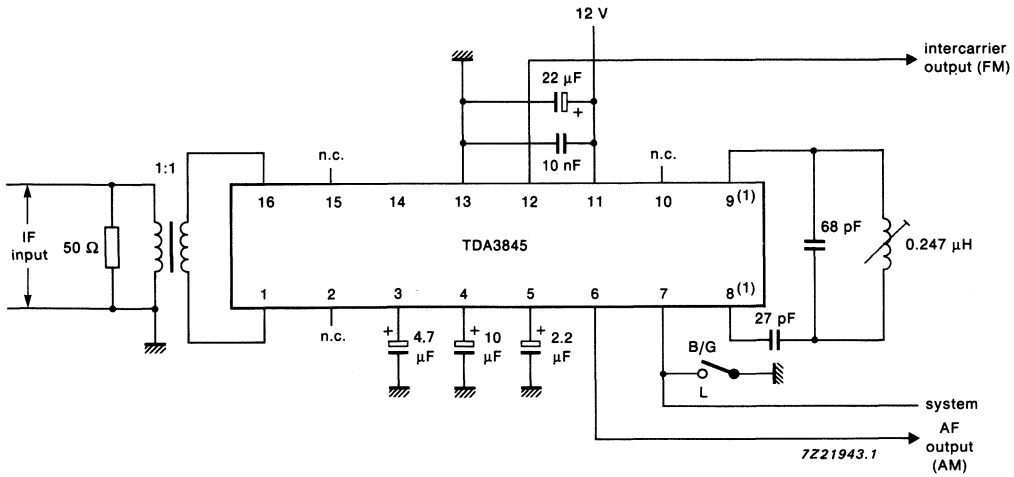
6. Residual video AM is defined as:
   m = (A-B)/A
   A = intercarrier level at sync pulse
   B = intercarrier level at 100% white video modulation
7. If higher AC output current is required an external resistor must be connected between the output pin and ground in order to increase the bias current of the emitter follower. The allowable maximum DC output current must not be exceeded.
8. For all S/N measurements the used vision IF modulator must conform to the following:
   Incidental phase modulation for black-to-white jump should be less than 0.5 degrees.
   Intercarrier performance, measured with the television demodulator AMF2 (intercarrier mode weighted S/N ratio) better than 60 dB for 6 kHz sinewave black-to-white video modulation.
   Weighted S/N ratio of the demodulated intercarrier signals in accordance with CCIR 468-2, measured with deemphasis of 50 μs.
   The indicated (S + W)/W ratio X/Y concerns the sound channels 1 and 2 that means demodulated intercarrier signals of 5.5 and 5.74 MHz respectively.
9. Sound carrier frequency = 32.4 MHz modulated with f = 1 kHz and a modulation depth of 80%. IF input signal (sound carrier) $V_{1\text{-}16}$ = 10 mV (RMS value).
10. The capacitor at pin 4 can be omitted, however, the (S + W)/W figure for the AM sound (standard L) will be up to 8 dB worse in the IF voltage range 1 mV to 100 mV.
11. When the supply at V_{P2} = 12 V the performance will be comparable with the performance when V_{P1} = 5 to 8 V.
    The power supply pin that is not in use should be disconnected.
12. The maximum value is given as minimum 120 kHz and typical 700 kHz.



(1) See note 5 to the characteristics.

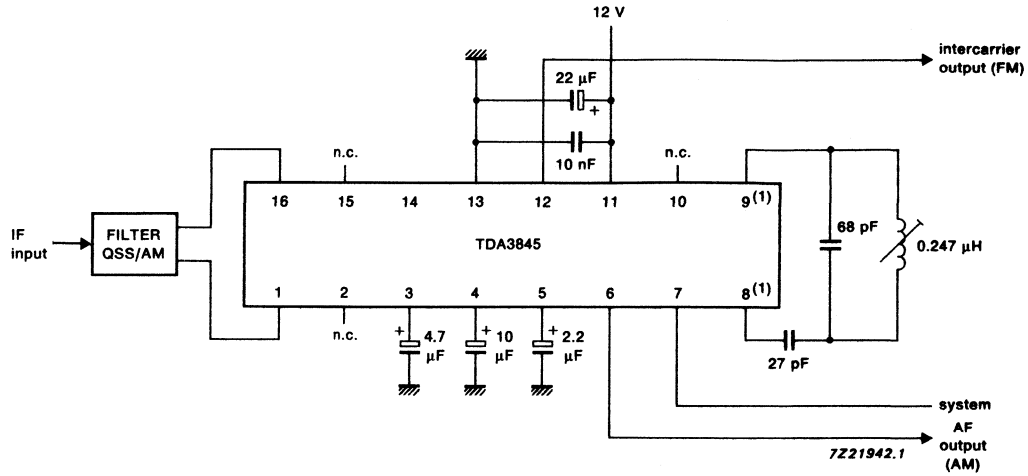
Fig.2 Test circuit for the + 5 V supply.

DEVELOPMENT DATA



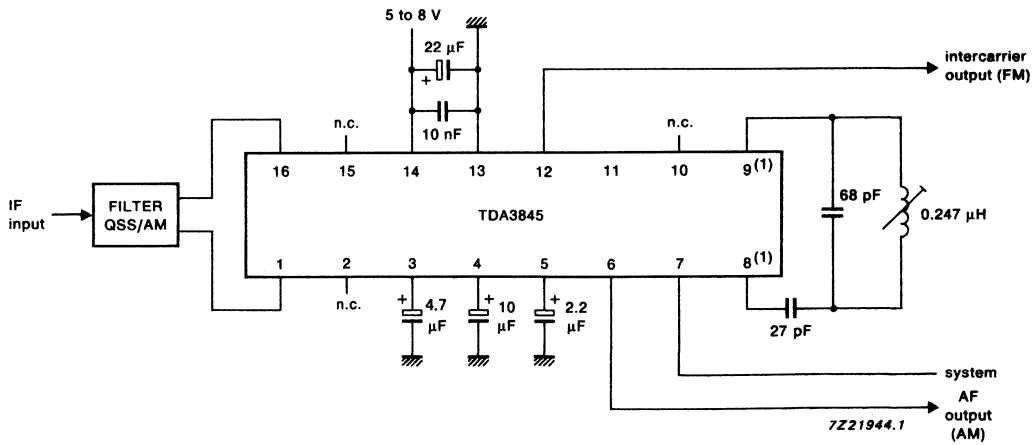
(1) See note 5 to the characteristics.

Fig.3 Test circuit for the + 12 V supply.



(1) See note 5 to the characteristics.

Fig.4 Application diagram for the + 12 V supply.



(1) See note 5 to the characteristics.

Fig.5 Application diagram for the + 5 V supply.

DEVELOPMENT DATA

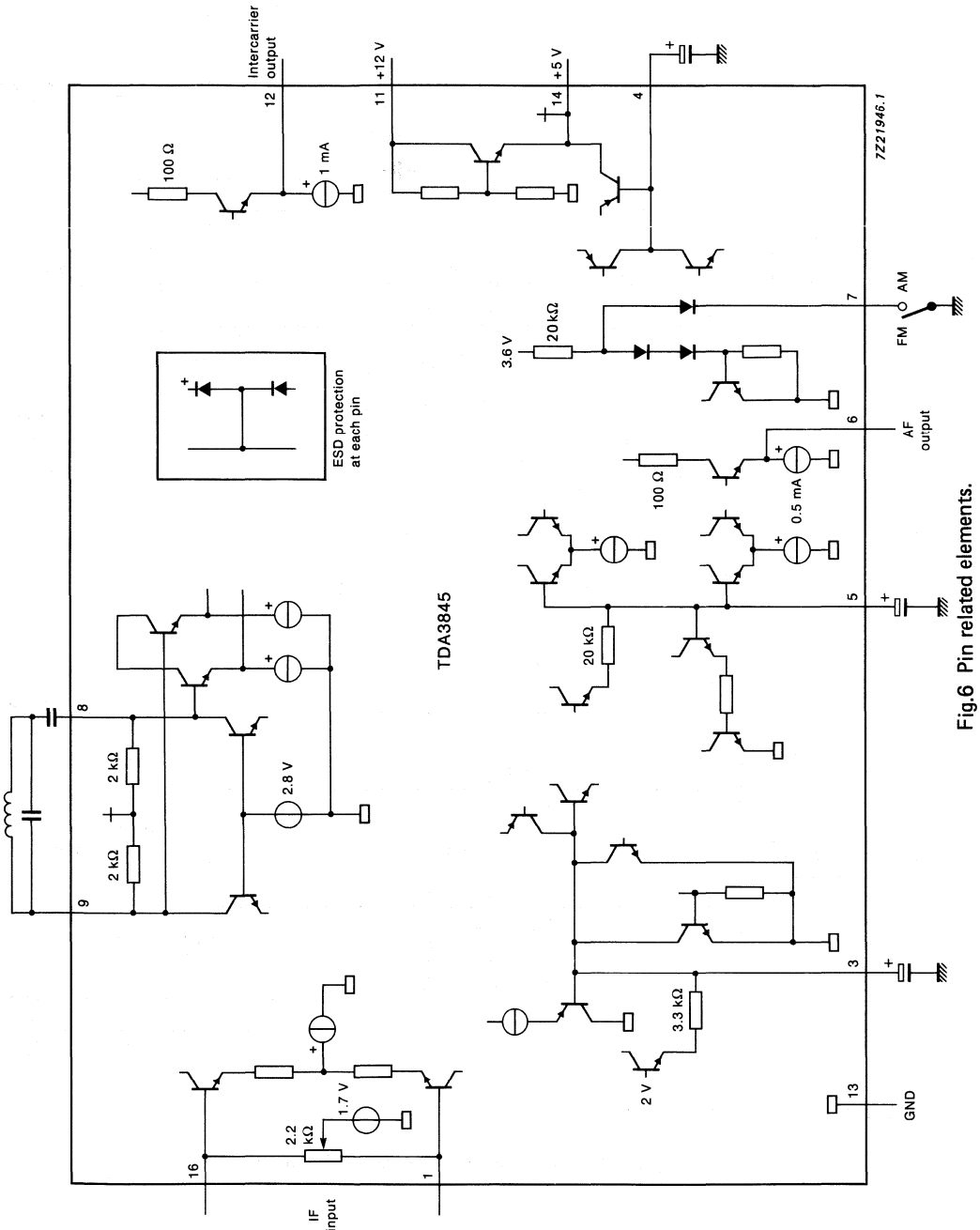
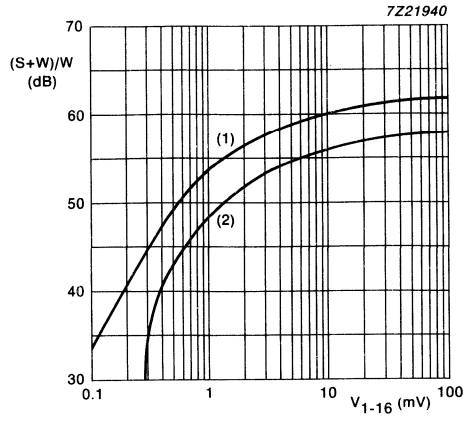


Fig.6 Pin related elements.



Picture modulation; 6 kHz sinewave.
Intercarrier signal; sound channel 1 = 5.5 MHz
sound channel 2 = 5.74 MHz.

Fig.7 Response curve of the signal-to-weighted-noise ratio of the demodulated intercarrier signal.

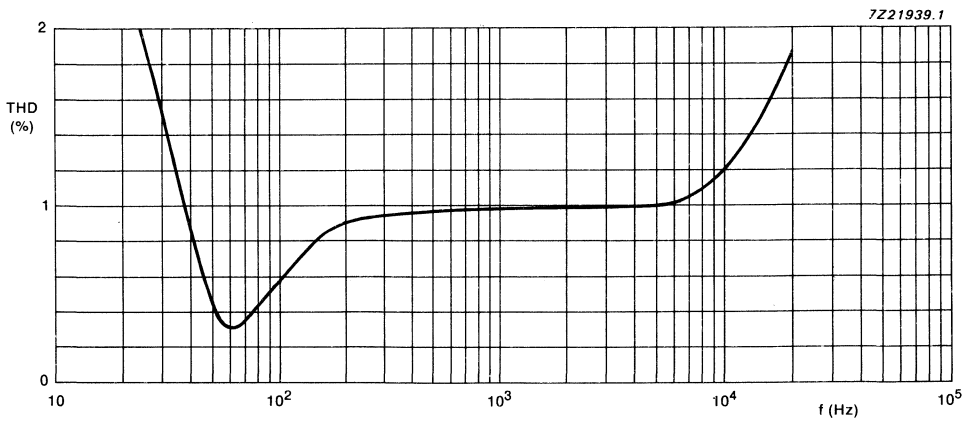


Fig.8 Response curve for the total harmonic distortion of the AM signal.

VERTICAL DRIVER

GENERAL DESCRIPTION

The TDA4301 is an integrated circuit which acts as an inverting buffer between the pulse pattern generator SAD1019 (LOCMOS technology) and the NXA1011 to NXA1041 frame-transfer sensors. The circuit consists of four drivers either for all vertical transfer clocks for image part (1A to 4A), or all vertical transfer clocks for storage part (1B to 4B) electrodes, and one driver for a transfer gate (TG) electrode.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltages						
pin 13		$V_{13\text{-}16}$	4.5	5.0	5.5	V
pin 1		$V_{1\text{-}16}$	11.0	11.25	11.5	V
Supply current	$V_{13\text{-}16} = 5$ V	I_{13}	–	14	–	mA
Operating current	$V_{1\text{-}16} = 11.25$ V	I_1	–	9.25	–	mA
Storage temperature range		T_{stg}	−25	–	+150	°C
Operating ambient temperature range		T_{amb}	−20	–	+70	°C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

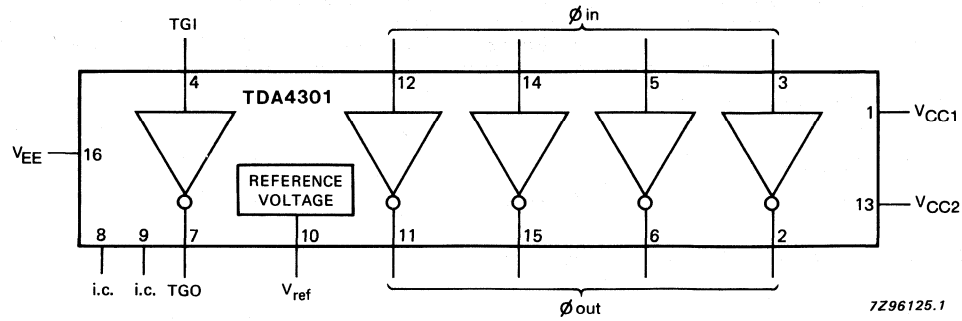


Fig.1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltages					
pin 1		V_{CC1}	–	12	V
pin 13		V_{CC2}	–	12	V
DC output current	$t < 1$ s				
pins 2, 6, 11 and 13		I_O	–	250	mA
pin 7		I_{TGO}	–	10	mA
Total power dissipation		P_{tot}	–	550	mW
Operating ambient temperature range		T_{amb}	–20	+70	°C
Storage temperature range		T_{stg}	–25	+150	°C

DC CHARACTERISTICS

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 13)	V_{CC2}	4.5	5.0	5.5	V
Supply voltage (pin 1)	V_{CC1}	11.20	11.25	11.30	V
Reference voltage (pin 10)	V_{ref}	3.60	3.75	3.90	V
Supply current (pin 13)	I_{CC2}	–	14.0	–	mA
Operating current (pin 1)	I_{CC1}	–	9.25	–	mA

DEVELOPMENT DATA

AC CHARACTERISTICS

$V_{CC1} = V_{1-16} = 11.25$ V; $V_{CC2} = V_{13-16} = 5.0$ V; $T_{amb} = 25$ °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs (pins 3, 4, 5, 12 and 14)						
Input voltage range		V_ϕ	0	–	5	V
Input threshold voltage		$V_\phi TH$	0.9	1.1	1.3	V
Input current	$V_\phi = 5$ V	I_ϕ	–	10	30	μA
Outputs (pins 2, 6, 11 and 15)	$C_L = 2000$ pF					
Output voltage swing (peak-to-peak value)		$V_{\phi(p-p)}$	–	10	–	V
Timing	see Fig.2					
Negative slope delay		t_{d1}	–	–	100	ns
Negative slope (fall time)		t_{d5}	50	70	90	ns
Positive slope delay		t_{d3}	–	–	100	ns
Positive slope (rise time)		t_{d6}	30	50	70	ns
Output (pin 7)	$C_L = 68$ pF					
Output voltage swing (peak-to-peak value)		$V_{TGO(p-p)}$	–	10	–	V
Timing	see Fig.2					
Negative slope delay		t_{d1}	–	–	100	ns
Negative slope (fall time)		t_{d5}	70	100	120	ns
Positive slope delay		t_{d3}	–	–	100	ns
Positive slope (rise time)		t_{d6}	50	70	90	ns

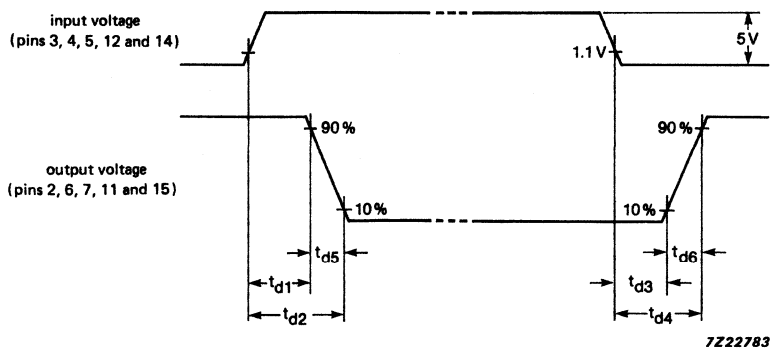


Fig.2 Timing diagram.

Load output (ϕ out) $C_L = 2000$ pF; load output (TGO) $C_L = 68$ pF. At the specified load only one switching may be done at a time.

APPLICATION INFORMATION

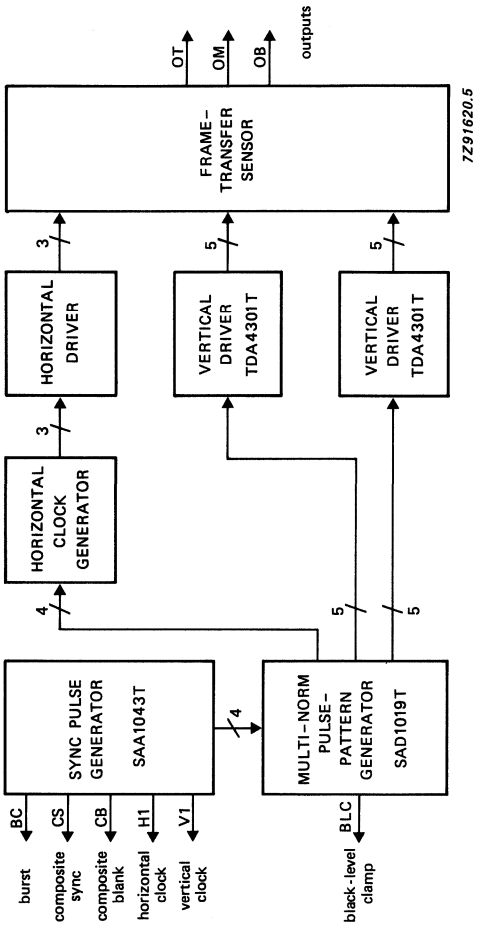


Fig.3 Control circuitry for driving the NXA1011 to NXA1041 frame-transfer sensors.

VERTICAL DRIVER

GENERAL DESCRIPTION

The TDA4301T is an integrated circuit which acts as an inverting buffer between the pulse pattern generator SAD1019 (LOCMOS technology) and the NXA1011 to NXA1041 frame transfer sensors. The circuit consists of four drivers either for all vertical transfer clocks for image part (1A to 4A), or all vertical transfer clocks for storage part (1B to 4B) electrodes, and one driver for a transfer gate (TG) electrode.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltages						
pin 11		V_{11-14}	4.5	5.0	5.5	V
pin 1		V_{1-14}	11.0	11.25	11.5	V
Supply current	V_{11-14} = 5 V	I_{11}	–	14	–	mA
Operating current	V_{1-14} = 11.25 V	I_1	–	9.25	–	mA
Storage temperature range		T_{stg}	−25	–	+150	°C
Operating ambient temperature range		T_{amb}	−20	–	+70	°C

PACKAGE OUTLINE

14-lead mini-pack; plastic (SO14; SOT108A).

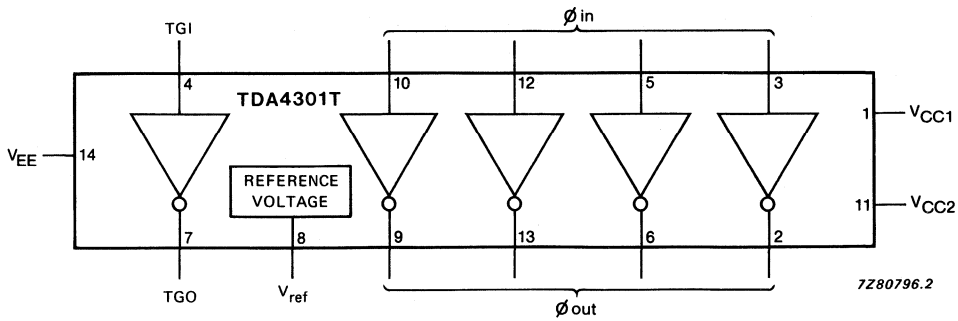


Fig.1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltages					
pin 1		V_{CC1}	–	12	V
pin 11		V_{CC2}	–	12	V
DC output current	$t < 1$ s				
pins 2, 6, 9 and 13		I_O	–	250	mA
pin 7		I_{TGO}	–	10	mA
Total power dissipation		P_{tot}	–	550	mW
Operating ambient temperature range		T_{amb}	−20	+70	°C
Storage temperature range		T_{stg}	−25	+150	°C

DC CHARACTERISTICS

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 11)	V_{CC2}	4.5	5.0	5.5	V
Supply voltage (pin 1)	V_{CC1}	11.20	11.25	11.30	V
Reference voltage (pin 8)	V_{ref}	3.60	3.75	3.90	V
Supply current (pin 11)	I_{CC2}	–	14.0	–	mA
Operating current (pin 1)	I_{CC1}	–	9.25	–	mA

DEVELOPMENT DATA

AC CHARACTERISTICS

$V_{CC1} = V_{1-14} = 11.25$ V; $V_{CC2} = V_{11-14} = 5.0$ V; $T_{amb} = 25$ °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs (pins 3, 4, 5, 10 and 12)						
Input voltage range		V_ϕ	0	–	5	V
Input threshold voltage		$V_\phi TH$	0.9	1.1	1.3	V
Input current	$V_\phi = 5$ V	I_ϕ	–	10	30	μA
Outputs (pins 2, 6, 9 and 13)	$C_L = 2000$ pF					
Output voltage swing (peak-to-peak value)		$V_{\phi(p-p)}$	–	10	–	V
Timing	see Fig.2					
Negative slope delay		t_{d1}	–	–	100	ns
Negative slope (fall time)		t_{d5}	50	70	90	ns
Positive slope delay		t_{d3}	–	–	100	ns
Positive slope (rise time)		t_{d6}	30	50	70	ns
Output (pin 7)	$C_L = 68$ pF					
Output voltage swing (peak-to-peak value)		$V_{TGO(p-p)}$	–	10	–	V
Timing	see Fig.2					
Negative slope delay		t_{d1}	–	–	100	ns
Negative slope (fall time)		t_{d5}	70	100	120	ns
Positive slope delay		t_{d3}	–	–	100	ns
Positive slope (rise time)		t_{d6}	50	70	90	ns

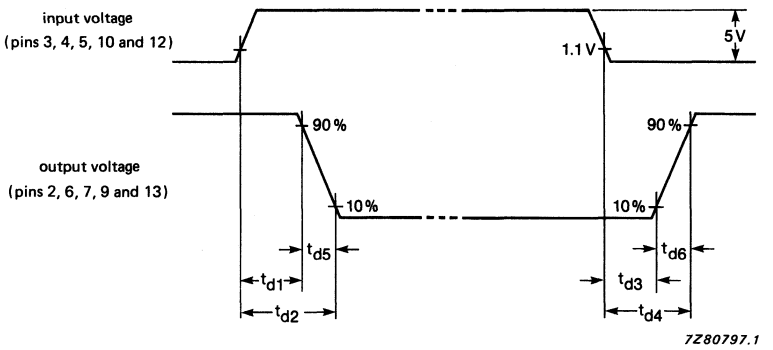


Fig.2 Timing diagram.

Load output (ϕ out) $C_L = 2000$ pF; load output (TGO) $C_L = 68$ pF. At the specified load switching only one may be done at a time.

APPLICATION INFORMATION

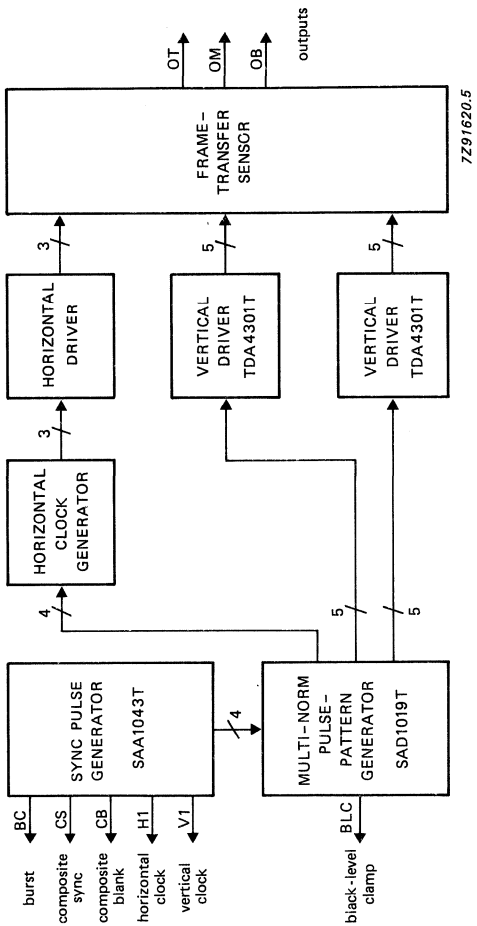


Fig.3 Control circuitry for driving the NXA1011 to NXA1041 frame-transfer sensors.

MASTER GAIN

GENERAL DESCRIPTION

The TDA4306 is an integrated circuit which controls the amplification of the four output signals (White, Yellow, Green and Cyan) from the frame transfer sensors (NXA1021 to NXA1041). The matching of the four channels is excellent over the whole control and temperature range. An on-chip white clipping circuit protects the white processor (TDA4303) from output signals that are too large. If white clipping occurs, a pulse is available to kill the colour information. Highlights will always be white, not coloured.

Features

- Four variable gain amplifiers
- White clipping circuit
- Blanking switch
- 2.1 V reference voltage

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 20)	$V_P = V_{20\text{-}10}$	4.75	5.0	5.25	V
Reference voltage (pin 6)	V_{ref}	1.9	2.1	2.3	V
Total power dissipation	P_{tot}	90	140	200	mW
Storage temperature range	T_{stg}	−25	–	+ 150	°C
Operating ambient temperature range	T_{amb}	−20	–	+ 70	°C

PACKAGE OUTLINES

TDA4306 : 20-lead DIL; plastic (SOT146).
TDA4306T: 20-lead mini-pack; plastic (SO20; SOT163A).

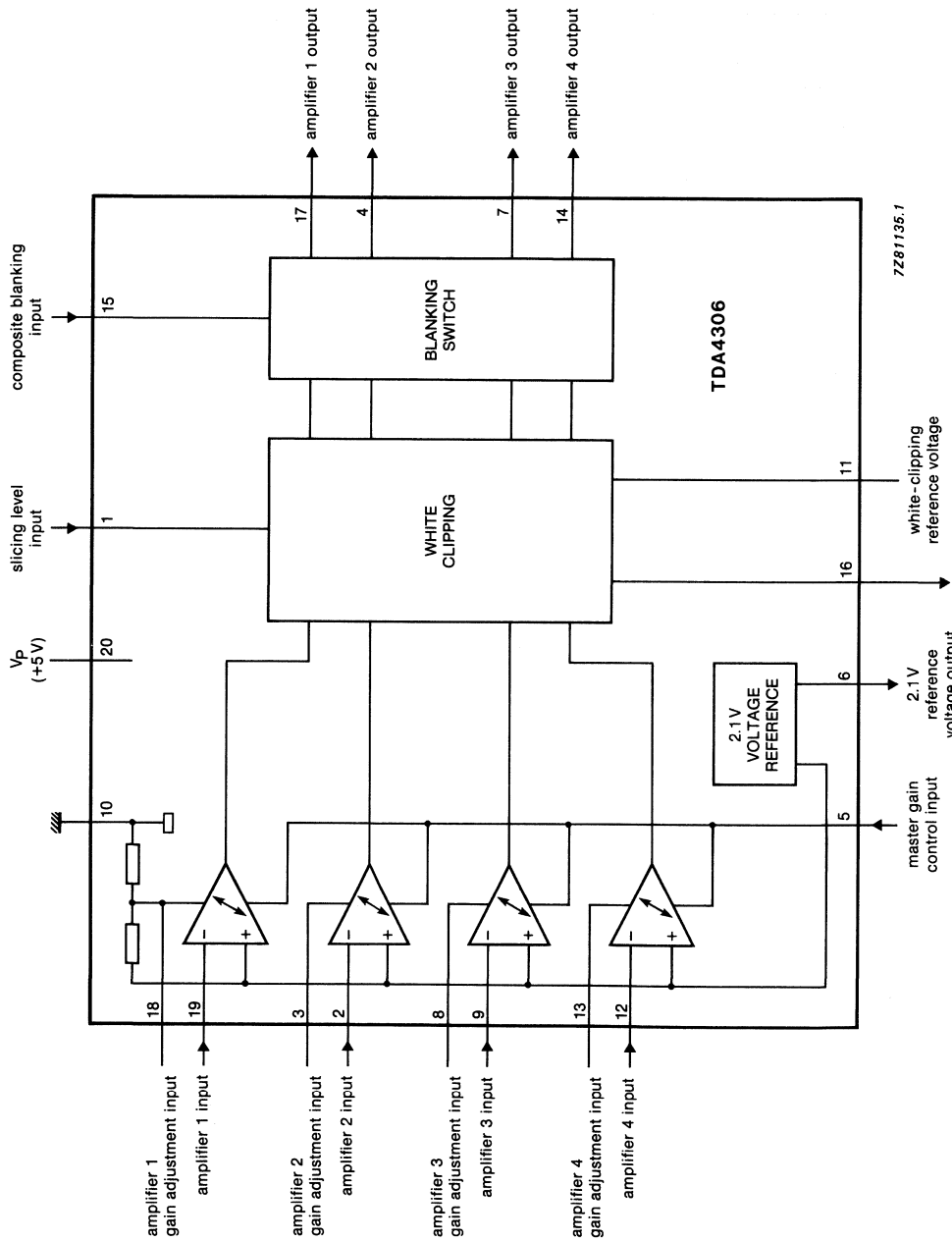


Fig.1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 20)	V_P	–	12	V
Input voltage (pins 1, 2, 3, 5, 8, 9 12, 13, 15, 18 and 19)	V_I	–	5	V
Output current (pins 17, 4, 7 and 14) $t < 1$ s	I_O	–	100	mA
Total power dissipation				
SO package*	P_{tot}	–	370	mW
DIL package	P_{tot}	–	1000	mW
Operating ambient temperature range	T_{amb}	–20	+ 70	°C
Storage temperature range	T_{stg}	–25	+ 150	°C

DEVELOPMENT DATA

* Mounted on a printed-circuit board.

CHARACTERISTICS

$V_P = V_{20-10} = 5$ V; $T_{amb} = 25\,^{o}C$ unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pin 20)	V_P	4.75	5.0	5.25	V
Reference voltage (pin 6)	V_{ref}	1.9	2.1	2.3	V
Temperature drift of V_{ref}	ΔV_{ref}	–	0.18	–	mV/°C
External load current	$I_{L(ext.)}$	–	–	10	mA
Total power dissipation	P_{tot}	90	140	200	mW
Variable gain amplifiers					
Inputs (pins 2, 9, 12 and 19; note 1)					
Input voltage (peak-to-peak value)					
negative video	$V_{n-10(p-p)}$	–	–	−1100	mV
positive video (gain = 1)	$V_{n-10(p-p)}$	–	–	400	mV
Input bias current at $V_I = 2.6$ V	$I_{n(bias)}$	–	2.2	5	μA
Input resistance	$R_{2, 9, 12, 19}$	–	300	–	kΩ
Outputs (pins 17, 4, 7 and 14)					
DC offset voltage of input to output (output = V_{ref})		–	–	−220	mV
DC offset voltage of input to output (output = V_{ref})		–	–	100	mV
Offset voltage between blanked output and V_{ref}		–	–	2	mV
Drift of blanked output voltages	ΔV_O	10	–	–	μV/°C
Output sink current	I_{OS}	–	–	100	μA
Resistive load of output to ground	R_L	1.5	–	–	kΩ
Output voltage swing at $V_{ref} = 2.1$ V		–	V_{ref}−500 mV	–	
Output voltage swing at $V_{ref} = 2.1$ V		–	V_{ref}+ 1200 mV	–	
Output impedance	$\|Z_O\|$	–	100	–	Ω
Power supply rejection ratio (1 kHz)	RR	–	30	–	dB
Bandwidth	B	6	–	–	MHz

parameter	symbol	min.	typ.	max.	unit
Master gain control input (pin 5)					
Gain control range			see Fig. 2		
Input current at V_{5-10} = 0 V	I_5	–	–	30	μA
Matching of gain (note 2) between the 4 channels ($f_{temp.\ range}$ and as $f_{gain\ range\ 2\ to\ x\ 8}$)		–	–	1	%
Gain stability = $f_{temp.range}$ $-20 < t < 60$ °C		–	3	–	%
Differential gain	dG	–	–	1	%
Differential phase	dϕ	–	–	2	deg.
Gain adjustment inputs (pins 18, 3, 8, 13)					
Input voltage range	V_{adj}	0.9	–	1.9	V
Overall gain (MG = 2) at V_{adj} = 0.9 V	G	–	–	2.2	
at V_{adj} = 1.9 V	G	1.5	–	–	
Input current (pins 3, 8 and 13) at V_I = 1,6 V	I_I	–	–	2	μA
Input resistance (pin 18)	R_{18}	–	3.25	–	kΩ
Input voltage (pin 18; open-circuit)	V_I	–	1.2	–	V
White clipping circuit					
Slicing level (pin 1) input voltage range	V_{1-10}	0.5	–	1.8	V
input current at V_{1-10} = 1 V	I_1	–	–	2	μA
White clipping reference voltage (pin 11)	V_{11-10}	–	V_{1-10} x 2.5 V	–	V
Output pulse (pin 16) (peak-to-peak value)	$V_{16-10(p-p)}$	3.0	–	–	V
Output voltage (pin 16) LOW	V_{OL}	–	–	1	V
HIGH	V_{OH}	4	–	–	V
Output sink current (pin 16)	I_{OS}	–	–	0.1	mA
Delay of a variable gain amplifier input to white clipping output	t_d	–	–	100	ns

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Blanking switch (pin 15)					
Composite blanking input voltage					
active HIGH	$V_{15\text{-}10}$	2.4	–	V_P	V
active LOW	$V_{15\text{-}10}$	–	–	1.4	V
Input current at $V_{15\text{-}10} = 5$ V	I_{15}	–	–	2	μA
Input capacitance	C_I	–	–	5	pF
Delay between blanking input and one of the 4 amplifier outputs	t_d	–	40	100	ns

Notes to the characteristics

1. The maximum input voltage is permitted only if the input voltage minus the DC offset voltage = 2.1 V. If the input voltage minus the DC offset voltage = 1.6 V, the maximum input voltage is 1 V(p-p).
2. Over the range 2 to x 8, after that each channel is adjusted to 0. This is possible only if the blanking pulse is switched off and the DC input voltage is equal to V_{ref}.

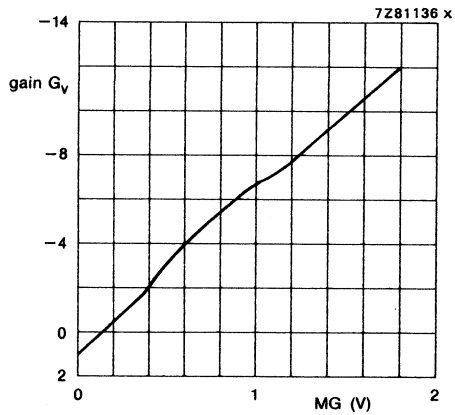


Fig.2 Gain as a function of V_{MG}.

SMALL SIGNAL COMBINATION IC FOR MONOCHROME TV

GENERAL DESCRIPTION

The TDA4500 combines all small signal functions (except the tuner) which are required for a monochrome television receiver.

For a complete monochrome television receiver only output stages are required to be added for horizontal and vertical deflection, video and sound. The TDA4500 can also be used in simple colour television receivers. In this application an external sandcastle pulse generator is required.

It incorporates the following functions:

- vertical sync separator/oscillator
- vertical output
- coincidence detector (sound mute)
- phase detector/frequency control
- a.g.c. detector
- sync separator
- horizontal oscillator
- synchronous demodulator
- vision i.f. amplifier
- tuner a.g.c.
- d.c. volume control
- a.f.c. detector
- video output
- sound demodulator
- audio output
- gate pulse generator
- sound limiter/feedback
- 90° phase shift
- overload detector
- horizontal output

QUICK REFERENCE DATA

Supply voltage	V_{7-10}, V_{22-10}	typ.	10,5	V
Supply current	I_7	typ.	75	mA
Supply current	I_{22}	typ.	4,5	mA
Operating ambient temperature range	T_{amb}		−25 to +65	°C
Storage temperature range	T_{stg}		−25 to +150	°C
Power dissipation	P_{tot}	max.	1,7	W

PACKAGE OUTLINE

28-lead DIL; plastic, with internal heat spreader (SOT117).

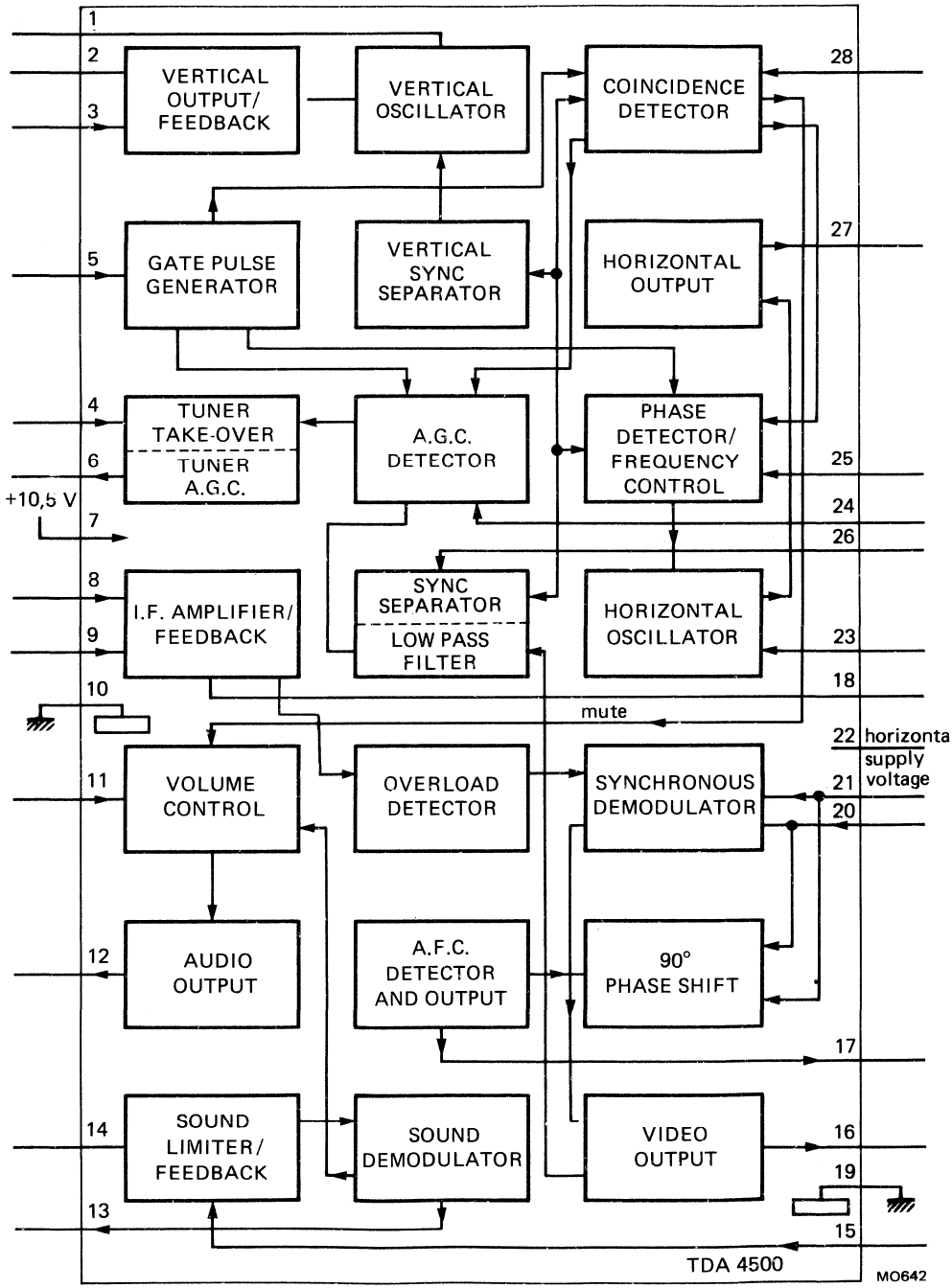


Fig. 1 Block diagram.

PINNING

Pin number	function	Pin number	function
1.	vertical oscillator	15.	sound i.f.
2.	vertical output	16.	video output
3.	vertical feedback	17.	a.f.c. output
4.	top linearity	18.	decoupling capacitor
5.	flyback pulse	19.	ground
6.	tuner a.g.c.	20.	38,5 MHz reference
7.	+10,5 V supply	21.	(38,9 MHz reference)
8.	i.f. input	22.	horizontal supply voltage
9.		23.	horizontal oscillator
10.	ground	24.	top sync detector
11.	volume control	25.	phase detector
12.	sound output	26.	sync separator
13.	6 MHz tuning (5,5 MHz tuning)	27.	horizontal output
14.	decoupling	28.	mute/coincidence detector

FUNCTIONAL DESCRIPTION (Fig. 1)

A complete black-and-white receiver can be built around this circuit by adding only the output stages for horizontal and vertical deflection with the video and sound output stages. The TDA4500 can also be used in simple colour television receivers using an external circuit to generate the sandcastle.

The block diagram (Fig. 1) depicts the various functions which are described briefly below.

The sensitivity of the i.f. amplifier is 70 μV for a peak-to-peak output voltage of 3 V (compare the TDA3541). This amplifier has a symmetrical input (pins 8 and 9) and is followed by a synchronous demodulator. The external tuned circuit is connected to pins 20 and 21. This circuit provides the information for the a.f.c. circuit, the 90° phase shift being supplied by internal RC-networks. An a.f.c. output with a voltage swing of about 9 V is obtained from pin 17 (V_{7-10} = 10,5 V).

The a.g.c. detector is gated to reduce sensitivity to external electrical noise and the a.g.c. time constant network is connected to pin 24. Gain control range of the i.f. amplifier is greater than 60 dB. Adjustments of the tuner take-over point is made at pin 4. When the voltage at pin 4 is approximately 3,5 V the direction of the tuner control voltage is positive-going. When the voltage at pin 4 is approximately 8 V the direction of the tuner control voltage is negative-going.

An output signal of 3 V (p-p) is obtained from the video amplifier (top sync level 1,5 V) with negative-going sync. Since the sound signal is derived from pin 16 (see Fig. 4) the video output is not blanked during the flyback period. As shown in the application circuit (Fig. 4) the band-pass filter for the sound must be connected between video output (pin 16) and sound i.f. input (pin 15). Sound information passes through a sound limiter network and a sound demodulator circuit with an external tuned circuit for this stage connected to pin 13. The demodulator is followed by a volume control stage with a control range of 80 dB and an output amplifier with an audio output signal of 170 mV (r.m.s.) for a Δf of 7,5 kHz and at maximum volume setting.

The slicing level of the sync separator is referred to the top sync and is determined by the values of external resistors, the recommended slicing level being 30%. Noise protection is provided for the sync separator stage. Separated sync pulses are supplied to the gated phase detector which compare the sync pulses with the sawtooth voltage obtained from the horizontal flyback pulse (pin 5). During catching the gating of the phase detector is switched off and the phase detector output current is increased.

The in-sync or out-of-sync condition is detected with the coincidence detector which is also used for transmitter identification. Sound output is suppressed when no input signal is available. Clamping the voltage on pin 28 to a level of 3,5 V sets the phase detector to a high output current, short time constant mode. This is appropriate for the reception of VCR signals.

Phase detector output voltage levels maintain the horizontal oscillator at its correct operating frequency. The push-pull output (pin 27) has a typical duty cycle of 40%.

Vertical sync pulses are obtained from an internal integrating network with the vertical sawtooth being generated in the vertical oscillator. This sawtooth voltage is compared with the feedback voltage from the deflection coil via pin 3. The comparator generates the drive voltage for the vertical deflection output stage.

The TDA4500 has four supply pins. Pin 7 and pin 10 are for the main positive supply and circuit ground respectively.

Critical circuits are grounded by pin 19. Pin 22 is the supply for the horizontal oscillator. A low current supply (5 mA minimum) can be used to start the oscillator from an external high voltage supply rail.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_{7-10}, V_{22-10}	max.	13,2	V
Total power dissipation	P_{tot}	max.	1,7	W
Storage temperature range	T_{stg}		−25 to +150	°C
Operating ambient temperature range	T_{amb}		−25 to +65	°C

CHARACTERISTICS

V_{7-10} = 10,5 V, V_{22-10} = 10,5 V and T_{amb} = 25 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{7-10}	9,5	10,5	13,2	V
Supply current	I_7	–	75	–	mA
Supply voltage (horizontal oscillator)	V_{22-10}	9,5	10,5	13,2	V
Supply current (horizontal oscillator, note 1)	I_{22}	–	4,5	–	mA
Power dissipation	P_{tot}	–	850	–	mW
Vision i.f. amplifier (pin 8)					
Input sensitivity (onset of a.g.c.) at 39,5 MHz (note 2)	$V_{i(rms)}$	–	70	–	μV
Differential input resistance (note 3)	R_i	–	800	–	Ω
Differential input capacitance (note 3)	C_i	–	6	–	pF
Gain control range	ΔG	–	56	–	dB
Output signal expansion for 50 dB input signal variation (note 4)	ΔV_o	–	1	–	dB
Maximum input signal	$V_{i\,max}$	–	50	–	mV
Video amplifier (note 5)					
Zero signal output level (note 6)	V_{16-10}	–	5	–	V
Top sync output level (note 7)	V_{16-10}	1,2	1,4	1,6	V
Video output signal amplitude (peak-to-peak value)	$V_{16-10(p-p)}$	2,75	3,0	3,25	V
Internal bias current of n-p-n emitter follower output transistor	I_B	1,4	2,0	–	mA
Bandwidth of demodulated output signal	B	5	6	–	MHz
Video non-linearity (note 8)		–	–	10	%

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Tuner a.g.c.					
Take-over voltage (pin 4) for positive-going tuner a.g.c. (n-p-n tuner)	V_{4-10}	–	3,5	–	V
Take-over voltage (pin 4) for negative-going tuner a.g.c. (p-n-p tuner)	V_{4-10}	–	8	–	V
Maximum tuner a.g.c. output swing	$I_{6\ max}$	2	3	–	mA
Output saturation voltage at I_6 = 2 mA	$V_{6-10(sat)}$	–	–	300	mV
Leakage current	I_6	–	–	1	μA
A.F.C. circuit (note 9)					
A.F.C. output voltage swing	V_{17-19}	9	–	10	V
Available output current	$\pm I_{17}$	–	1	–	mA
Output voltage at nominal tuning of the reference tuned circuit	V_{17-19}	–	5,25	–	V
Sound circuit					
Input limiting voltage when $V_O = V_{Omax} - 3$ dB (note 10)	$V_{14\ lim}$	–	400	–	μV
Input resistance at pin 15 (note 11)	R_i	–	3	–	kΩ
A.F. output signal at pin 12 (note 12) (r.m.s. value)	$V_{12-10(rms)}$	170	–	240	mV
Volume control (pin 11) (Fig. 3)					
Voltage with pin 11 disconnected	V_{11-10}	–	6,5	–	V
Current pin 11 short-circuited to ground	I_{11}	–	1	–	mA
Volume control characteristic (note 13)			See Fig. 3		
Value of external control resistor	R_{11-10}	–	5	–	kΩ

parameter	symbol	min.	typ.	max.	unit
Horizontal synchronization circuit					
Slicing level sync separator (note 14)		–	30	–	%
Holding range PLL		–	±1000	–	Hz
Catching range PLL		–	±600	–	Hz
Control sensitivity video to flyback (note 15)		–	2	–	kHz/μs
Horizontal oscillator					
Free running frequency	f_{osc}	–	15625	–	Hz
Spread with fixed external components	Δf_{osc}	–	–	4	%
Frequency variations due to supply voltage changes (note 16)	$\Delta f_{osc}/\Delta V$	–	0	–	%
Frequency variation with temperature	$\Delta f_{osc}/\Delta T$	–	–	1×10^{-4}	K^{-1}
Maximum frequency shift	Δf_{osc}	–	–	10	%
Maximum frequency deviation between starting point output and nominal condition	Δf_{osc}	–	–	10	%
Horizontal (push-pull) output					
Output current	I_{27}	10	–	–	mA
Output impedance	R_{27-10}	–	200	–	Ω
Voltage when I_{27} = 10 mA	V_{27-10}	–	2	–	V
	V_{27-22}	–	3	–	V
Duty cycle of output pulse (note 17)	δ	0,35	0,40	0,45	
Flyback input (note 18)					
Minimum required input amplitude (peak-to-peak value)	$V_{5-10(p-p)}$	–	4	–	V
Phase detector switching voltage		–	0	–	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Coincidence detector (mute) (note 19)					
Voltage in synchronized condition	V_{28-19}	–	9,5	–	V
Voltage in non-synchronized condition (no-signal)	V_{28-19}	–	1,0	1,5	V
Switching level to switch phase detector from slow to fast	V_{28-19}	4,5	5,0	5,5	V
Switching level to activate the 'mute' function (transmitter identification)	V_{28-19}	2,25	2,5	2,75	V
Output current; in-sync (peak-to-peak value)	$I_{28(p-p)}$	–	1	–	mA
Vertical oscillator					
Free running frequency	f_{osc}	–	47,5	–	Hz
Spread with fixed external components	Δf_{osc}	–	–	4	%
Holding range at nominal frequency		52,5	–	–	Hz
Temperature coefficient	TC	–	1×10^{-4}	–	K^{-1}
Frequency shift due to a supply voltage change from 9,5 to 12 V	$\Delta f_{osc}/\Delta V$	–	5	–	%
Vertical output (pin 2)					
Output current	I_2	1	1,3	–	mA
Output resistance	R_{2-10}	–	2	–	kΩ
Feedback input (pin 3)					
D.C. input voltage	V_{3-10}	4,75	5	5,25	V
A.C. input voltage (peak-to-peak value)	$V_{3-10(p-p)}$	–	1,2	–	V
Input current	I_3	–	–	10	μA
Non-linearity of deflection current at V_P = 10,5 V		–	–	2,5	%

Notes to characteristics

1. It is possible to start the horizontal oscillator by supplying a current of 5 mA which can be taken from the mains rectifier, to pin 22. The main supply (pin 7) can then be derived from the horizontal output stage.
2. I.F. input voltage (r.m.s.) – value at top sync level at which the video amplitude has dropped 0,5 dB compared with the amplitude at an input signal of 10 mV.
3. The input impedance has been chosen such that a SAW-filter can be applied. 800 Ω is an acceptable compromise between the requirements for triple transient suppression and power loss.
4. Measured with 0 dB = 150 μV.
5. Measured at 10 mV(r.m.s.) top sync input signal.
6. With switched demodulator.
7. Signal with negative-going sync with top white being 10% of the top sync amplitude (Fig. 2).
8. This figure is valid for the complete video signal amplitude (peak-white to top sync).
9. Measured with an input signal (V_{8-9}) of 10 mV(r.m.s.); the a.f.c. output (pin 7) loaded with 2 x 100 kΩ between the supply and ground. The Q factor of the reference tuned circuit is 50.
10. Voltage at pin 15 is the r.m.s. value. Q_L of the demodulator tuned circuit is 20. Audio frequency is 1 kHz and the carrier frequency is 5,5 MHz.
11. Measured with an input signal of 1 mV(r.m.s.)
12. The tuned demodulator circuit must give an output level equal to that given in the "mute" condition.
13. Volume can be controlled using a variable resistor connected to ground (nominal 5 kΩ) or by means of a variable d.c. voltage. In this latter case the rather low impedance at pin 11 must be taken into account.

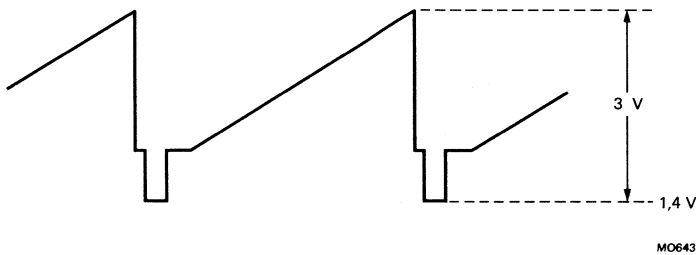


Fig. 2 Video output signal.

Notes to characteristics (continued)

14. The sync separator is noise gated. The slicing level is referred to top sync level and is independent of the video information. The value given is a percentage of the sync pulse amplitude. The slicing depends on the values of external resistors connected to pin 26.
15. Phase detector current increases by a factor of 7 during "catching" and when phase detector operates in the 'FAST' mode (pin 28). This ensures a high catching range and a higher dynamic loop gain.
16. Supply voltage variation in the range 8 to 12 V.
17. The negative-going edge of this pulse initiates the switch-off of the horizontal output transistor (simultaneous driver).
18. The circuit requires an integrated flyback pulse. The gate pulses for a.g.c. and the coincidence detector are obtained from the sawtooth.
19. The functions of in-sync/out-of-sync and transmitter identification have been combined on pin 28. For reception of VCR-signals the voltage on this pin must be fixed between 3 V and 4,5 V so that the time constant is fast and the sound is still available.

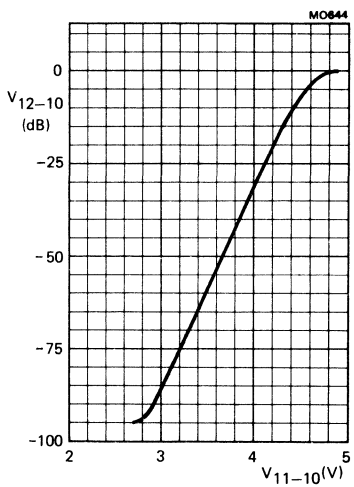


Fig. 3 Volume control characteristic at f = 1 kHz.

APPLICATION INFORMATION

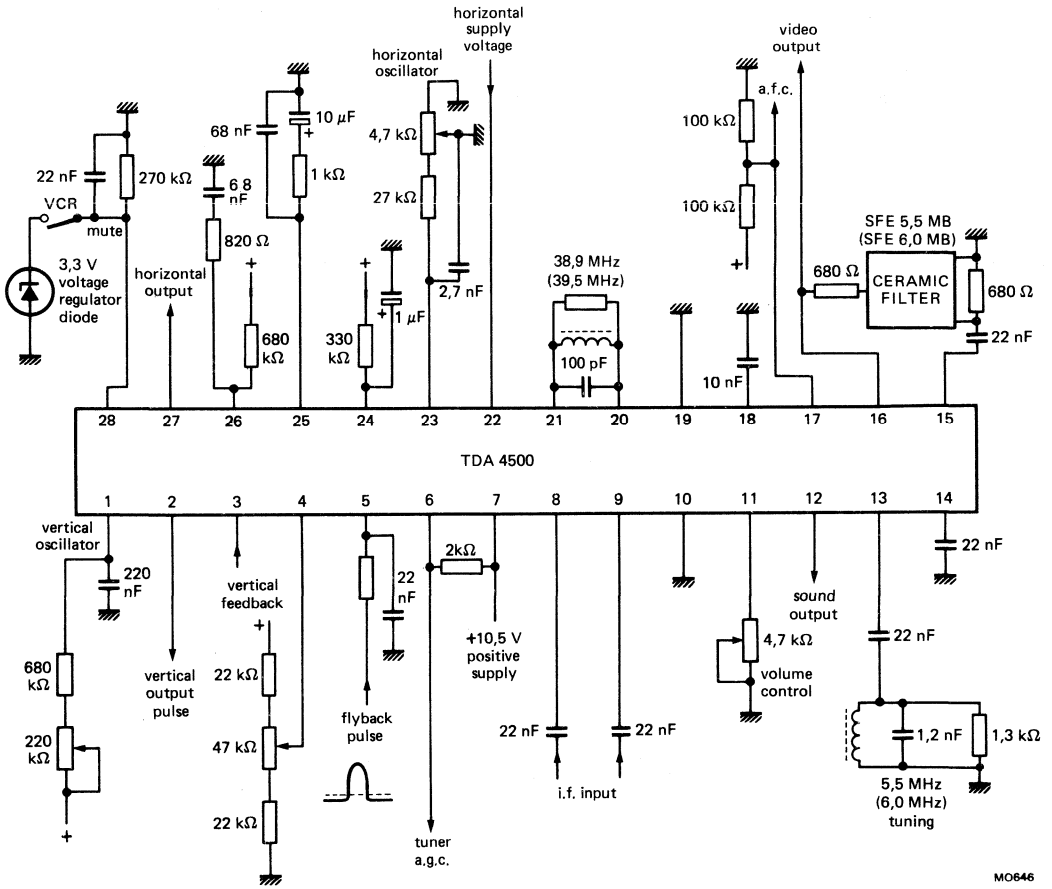


Fig. 4 Typical application circuit.

SMALL SIGNAL COMBINATION IC FOR COLOUR TV

GENERAL DESCRIPTION

The integration into a single package of all small-signal functions required for colour tv reception is achieved in the TDA4501. The only additional circuits needed to complete the receiver are a tuner, the deflection output stages and a colour decoder.
The IC includes a vision IF amplifier with synchronous demodulator and AFC circuit; an AGC detector with tuner output; an integral three-level sandcastle pulse generator; and fully synchronized vertical and horizontal drive outputs. A triggered vertical divider automatically adapts to 50 or 60 Hz working and eliminates the need for an external vertical frequency control.
Signal-strength dependent time-constant switches in the horizontal phase detector make external VCR switching unnecessary.
Sound signals are demodulated and amplified within the IC in a circuit which includes volume control and muting.

Features

- Vision IF amplifier with synchronous demodulator
- AGC detector for negative modulation
- AGC output to tuner
- AFC circuit
- Video and audio preamplifiers
- Sound IF amplifier and demodulator
- Choice of sound volume control or horizontal oscillator starting function
- Horizontal synchronization circuit with two control loops
- Triggered divider system for vertical synchronization and sawtooth generation giving automatic amplitude adjustment for 50 or 60 Hz working
- Transmitter identification circuit with mute output
- Sandcastle pulse generator

QUICK REFERENCE DATA

Supply voltage	V_{7-6}	typ.	10,5 V
Supply voltage	V_{11-6}	typ.	10,5 V
Operating ambient temperature range	T_{amb}	−25 to	+ 65 °C
Storage temperature	T_{stg}	−25 to	+ 150 °C
Power dissipation	P_{tot}	max.	1,7 W

PACKAGE OUTLINE

28-lead DIL; plastic (with internal heat spreader) (SOT117).

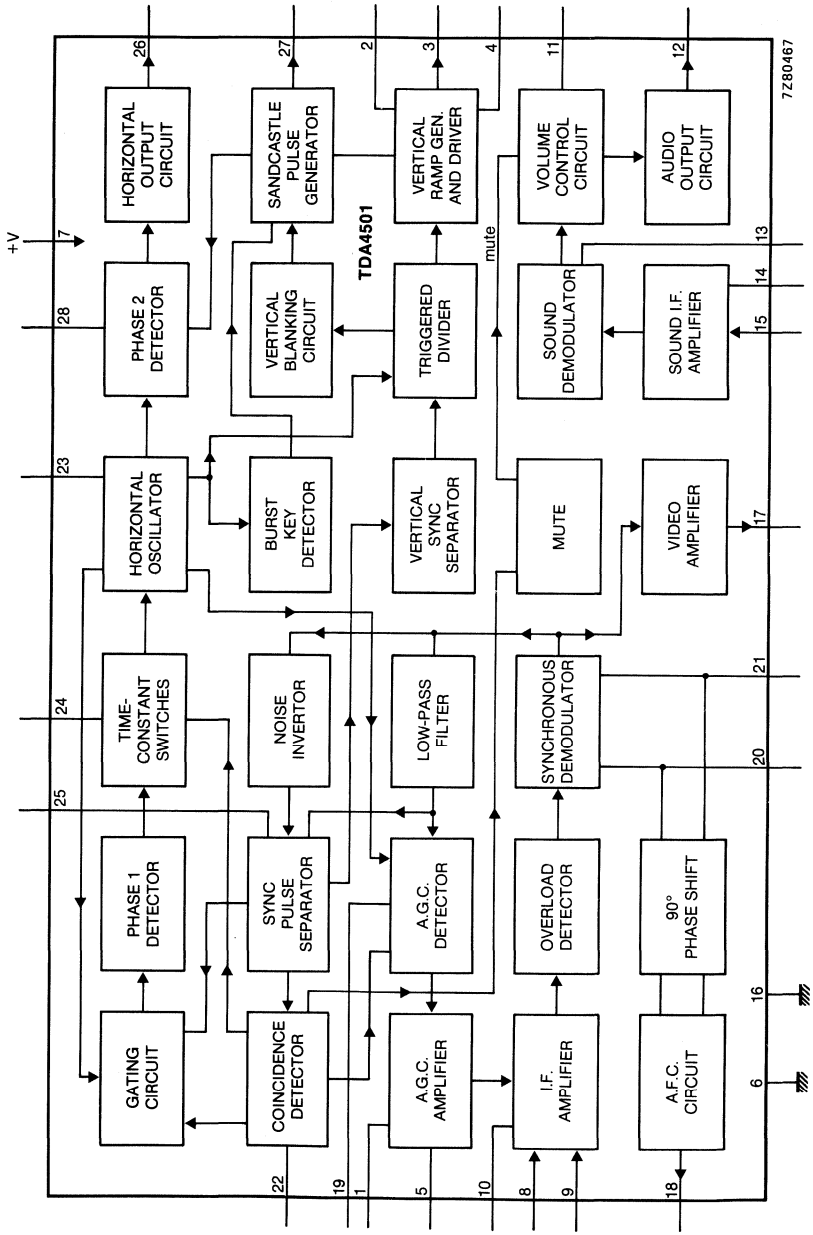


Fig. 1 Block diagram.

PINNING

1. AGC take over
2. Ramp generator
3. Vertical drive
4. Vertical feedback
5. Tuner AGC
6. Ground
7. Supply
8. IF input
9. IF input
10. Decoupling capacitor
11. Volume control/start Hor. osc.
12. Audio output
13. Sound demodulator
14. Sound IF decoupling
15. Sound IF input
16. Ground
17. Video output
18. AFC
19. AGC detection
20. Sync demodulator
21. Sync demodulator
22. Coincidence detector decoupling
23. Horizontal oscillator
24. Frequency control
25. Sync separator
26. Horizontal drive
27. Sandcastle out/flyback in
28. Phase detection

FUNCTIONAL DESCRIPTION

IF amplifier, demodulator and AFC

The IF amplifier has a symmetrical input (pins 8 and 9), the input impedance of which is suitable for SAW-filtering to be used. The synchronous demodulator and the AFC circuit share an external reference tuned circuit (pins 20 and 21). An internal RC-network provides the necessary phase-shifting for AFC operation. The AFC circuit provides a control voltage output with a swing greater than 9 V from pin 18.

DEVELOPMENT DATA

AGC circuit

Gating of the AGC detector is performed to reduce sensitivity of the IF amplifier to external electrical noise. The AGC time constant is provided by an RC-circuit connected to pin 19. Tuner AGC voltage is supplied from pin 5 and is suitable for tuners with p-n-p or n-p-n RF stages. The sense of the AGC (to increase in a positive or negative direction) and the point of tuner take-over are preset by the voltage level at pin 1.

Video amplifier

The signal through the video amplifier comprises video and sound information, therefore no gating of the video amplifier is performed during flyback periods.

Sound circuit and horizontal oscillator starting function

The input to the sound IF amplifier is obtained by a bandpass filter coupling from the video output (pin 17). The sound is demodulated and passed via a dual-function volume control stage to the audio output amplifier. The volume control function is obtained by connecting a variable resistor (10 kΩ) between pin 11 and ground, or by supplying pin 11 with a variable voltage. Sound output is suppressed by an internal mute signal when no input signal is present.

The horizontal oscillator starting function is obtained by supplying pin 11 with a current of 6 mA during the switching-on period. The IC then uses this current to generate drive pulses for the horizontal deflection. For this application, the main supply voltage for the IC can be obtained from the horizontal deflection circuit.

FUNCTIONAL DESCRIPTION (continued)

Vertical divider system

A triggered divider system is used to synchronize the vertical drive waveforms, adjusting automatically to 50 or 60 Hz working. A large window (search window) is opened between counts of 488 and 722; when a separated vertical sync pulse occurs before count 576, the system works in the 60 Hz mode, otherwise 50 Hz working is chosen.
A narrow window is opened when 15 approved sync pulses have been detected. Divider ratio between 522 and 528 switches to 60 Hz mode; between 622 and 628 switches to 50 Hz mode.
The vertical blanking pulse is also generated via the divider system by adding the anti-topflutter pulse and the blanking pulse.

Line phase detector

The circuit has three operating conditions:
a. Strong input signal and synchronized.
b. Weak signal and synchronized.
c. Non synchronized (weak and strong) signal.
The input signal condition is obtained from the AGC circuit.

D.C. volume control/horizontal oscillator start

The operation depends on the application. When during switch-on no current is supplied pin 11 will act as volume control. When a current of 6 mA is applied the volume control is set to maximum and the circuit will generate drive pulses for the horizontal deflection.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 7)	$V_P = V_{7-6}$	max.	13,2	V
Total power dissipation	P_{tot}	max.	1,7	W
Operating ambient temperature range	T_{amb}		−25 to + 65	°C
Storage temperature range	T_{stg}		−25 to + 150	°C

DEVELOPMENT DATA

CHARACTERISTICS

$V_P = V_{7-6} = 10{,}5$ V; $T_{amb} = 25$ °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage (pin 7)	V_{7-6}	9,5	10,5	13,2	V
Supply current (pin 7)	I_7	–	120	–	mA
Supply voltage (pin 11)	V_{11-6}	–	10,5	–	V
Supply current (pin 11) for horizontal oscillator start	I_{11}	–	6	–	mA
Vision IF amplifier (pins 8 and 9)					
Input sensitivity at 38,9 MHz (note 1)	V_{8-9}	40	70	120	μV
Input sensitivity at 45,75 MHz (note 1)	V_{8-9}	–	90	–	μV
Differential input resistance (pin 8 to 9)	R_{8-9}	–	1,3	–	kΩ
Differential input capacitance (pin 8 to 9)	C_{8-9}	–	5	–	pF
AGC range		–	60	–	dB
Maximum input signal	V_{8-9}	50	70	–	mV
Expansion of output signal for 50 dB variation of input signal with V_{8-9} at 150 μV (0 dB)	ΔV_{17-6}	–	1	–	dB
Video amplifier					
Output level for zero signal input (zero point of switched demodulator)	V_{17-6}	–	4,5	–	V
Output signal top sync level (note 2)	V_{17-6}	–	1,4	–	V
Amplitude of video output signal (peak-to-peak value)	$V_{17-6(p-p)}$	–	2,8	–	V
Internal bias current of output transistor (n-p-n emitter follower)	$I_{17(int)}$	1,4	2,0	–	mA
Bandwidth of demodulated output signal	B	–	6	–	MHz
Differential gain (Fig. 4)	G_{17}	–	6	–	%
Differential phase (Fig. 4)		–	4	–	%
Video non-linearity complete video signal amplitude		–	–	10	%
Intermodulation (Fig. 5) at gain control = 45 dB					
f = 1,1 MHz; blue;		55	60	–	dB
f = 1,1 MHz; yellow;		50	54	–	dB
f = 3,3 MHz; blue;		60	66	–	dB
f = 3,3 MHz; yellow		55	59	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Video amplifier (continued)					
Signal to noise ratio (note 3)					
Z_S = 75 Ω					
V_i = 10 mV	S/N	50	54	–	dB
end of gain control range	S/N	50	56	–	dB
Residual carrier signal		–	7	30	mV
Residual 2nd harmonic of carrier signal		–	3	30	mV
Tuner AGC *					
Take-over voltage (pin 1 for positive-going tuner AGC (NPN tuner)	$V_{1\text{-}6}$	–	3,5	–	V
Starting point take over; V = 5 V	$V_{1\text{-}6(rms)}$	–	0,4	2	mV
Starting point take over; V = 1,2 V	$V_{1\text{-}6(rms)}$	50	70	–	mV
Take-over voltage (pin 1) for negative-going tuner AGC (PNP tuner)	$V_{1\text{-}6}$	–	8	–	V
Starting point take over; V = 9,5 V	$V_{1\text{-}6(rms)}$	–	0,3	2	mV
Starting point take over; V = 5,6 V	$V_{1\text{-}6(rms)}$	50	70	–	mV
Maximum output swing	$I_{5\ max}$	2	3	–	mA
Output saturation voltage					
I = 2 mA	$V_{5\text{-}6(sat)}$	–	–	300	mV
Leakage current	I_5	–	–	1	μA
Input signal variation complete tuner control	ΔV_i	0,5	2	4	dB
AFC circuit (pin 18; note 4)					
AFC output voltage swing	$V_{18\text{-}6(p\text{-}p)}$	9	–	10	V
Available output current	$\pm I_{18}$	–	1	–	mA
Control steepness					
–100% picture carrier		20	40	80	mV/kHz
–10% picture carrier		–	15	–	mV/kHz
Output voltage at nom. tuning of the reference tuned circuit	$V_{18\text{-}6}$	–	5,25	–	V
Output voltage without input signal	$V_{18\text{-}6}$	2,7	5,25	8,5	V

* Starting point tuner take-over NPN current 1,8 mA; PNP tuner I = 0,2 mA.

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Sound circuit					
Input limiting voltage $V_o = V_o$ max. −3 dB; $Q_L = 16$ $f_{AF} = 1$ kHz; $f_c = 5{,}5$ MHz	V_{15lim}	–	400	–	μV
Input resistance $V_{i(rms)} = 1$ mV	$R_{15\text{-}6}$	–	2,6	–	kΩ
Input capacitance $V_{i(rms)} = 1$ mV	$C_{15\text{-}6}$	–	6	–	pF
AM rejection (Figs 8 and 9) $V_i = 10$ mV $V_i = 50$ mV	AMR AMR	– –	35 43	– –	dB dB
AF output signal $\Delta f = 7{,}5$ kHz; min. distortion	$V_{12\text{-}6(rms)}$	220	320	–	mV
AF output impedance	$Z_{12\text{-}6}$	–	150	–	Ω
Total harmonic distortion $\Delta f = 27{,}5$ kHz	THD	–	1	–	%
Ripple rejection $f_k = 100$ Hz, volume control 20 dB when muted	RR RR	– –	22 26	– –	dB dB
Output voltage mute condition	$V_{12\text{-}6}$	–	2,6	–	V
Signal to noise ratio weighted noise (CCIR 468)	S/N	–	47	–	dB
Volume control					
Voltage (pin 11 disconnected)	$V_{11\text{-}6}$	–	4,8	–	V
Current (pin 11 short circuited)	I_{11}	–	1	–	mA
External control resistor	$R_{11\text{-}6}$	–	10	–	kΩ
Suppression output signal during mute condition		–	66	–	dB
Horizontal synchronization					
Slicing level sync separator		–	30	–	%
Holding range PLL		800	1100	1500	Hz
Catching range PLL		600	1000	–	Hz
Control sensitivity video to oscillator; at weak signal at strong signal during scan during vert. retrace and during catching		– – –	2 3 6	– – –	kHz/μs kHz/μs kHz/μs

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Second control loop (positive edge)					
Control sensitivity	$\Delta t_d/\Delta t_o$	–	300	–	μs
Control range	t_d	–	25	–	μs
Phase adjustment via second control loop; control sensitivity		–	25	–	μA/μs
Maximum allowed phase shift		–	± 2	–	μs
Horizontal oscillator (pin 23)					
Free running frequency R = 35 kΩ; C = 2,7 nF	f_{fr}	–	15625	–	Hz
Spread with fixed external components		–	–	4	%
Frequency variation due to change of supply voltage from 8 to 12 V	Δf_{fr}	–	0	0,5	%
Frequency variation with temperature	Δf_{fr}	–	–	1×10^{-4}	K^{-1}
Maximum frequency shift	Δf_{fr}	–	–	10	%
Maximum frequency deviation (V_{7-6} = 8 V)	Δf_{fr}	–	–	10	%
Horizontal output (pin 26)					
Output voltage high	V_{26-6}	–	–	13,2	V
Output voltage at which protection commences	V_{26-6}	–	–	15,8	V
Output voltage low at I_{26} = 10 mA	V_{26-6}	–	0,3	0,5	V
Duty cycle of horizontal output signal	δ_0	–	45	–	%
Rise and fall times of output pulse	t_r, t_f	–	150	–	ns
Flyback input and sandcastle output					
Input current required during flyback pulse	I_{27}	0,1	–	2	mA
Output voltage during burst key pulse	V_{27-6}	7,5	–	–	V
Output voltage during horizontal blanking	V_{27-6}	3,5	4,0	4,5	V
Output voltage during vertical blanking	V_{27-6}	1,8	2,2	2,6	V
Width of burst key pulse		3,1	3,5	3,9	μs
Width of horizontal blanking pulse		flyback pulse width			
Width of vertical blanking pulse 50 Hz working		–	21	–	lines
60 Hz working		–	17	–	lines
Delay between start of sync pulse at video output and rising edge of burst key pulse		–	5,2	–	μs

parameter	symbol	min.	typ.	max.	unit
Coincidence detector mute output (pin 22)					
Voltage for in-sync condition	V_{22-6}	–	9,5	–	V
Voltage for no-sync condition no signal	V_{22-6}	–	1,0	1,5	V
Switching level to switch phase detector from slow to fast	V_{22-6}	4,9	5,3	5,8	V
Fast-to-slow hysteresis		–	1	–	V
Switching level to activate mute function (transmitter identification)	V_{22-6}	2,25	2,5	2,75	V
Output current for in-sync condition (peak-to-peak value)	$I_{22(p-p)}$	0,7	1,0	–	mA
Vertical ramp generator (pin 2)					
Input current during scan	I_2	–	12	–	μA
Discharge current during retrace	I_2	–	0,5	–	mA
Minimum voltage	V_{2-6}	–	1,5	–	V
Vertical output (pin 3)					
Output current	I_3	–	–	10	mA
Output impedance	R_{3-6}	–	400	–	Ω
Feedback input (pin 4)					
Input voltage					
d.c. component	V_{4-6}	–	3	–	V
a.c. component (peak-to-peak value)	$V_{4-6(p-p)}$	–	1,2	–	V
Input current	I_4	–	–	12	μA
Internal precorrection to sawtooth		–	6	–	%
Deviation amplitude 50/60 Hz		–	–	5	%

DEVELOPMENT DATA

Notes

1. Typical value taken at starting level of AGC.
2. Signal with negative going sync, maximum white level 10% of the maximum sync amplitude (see Fig. 3).
3. Signal-to-noise ratio equals $20 \log \frac{V_{o(\text{black to white})}}{V_{n(rms)} \text{ at } B = 5 \text{ MHz}}$.
4. $V_{i(rms)} = 10$ mV; see Fig. 2; Q-factor = 36.

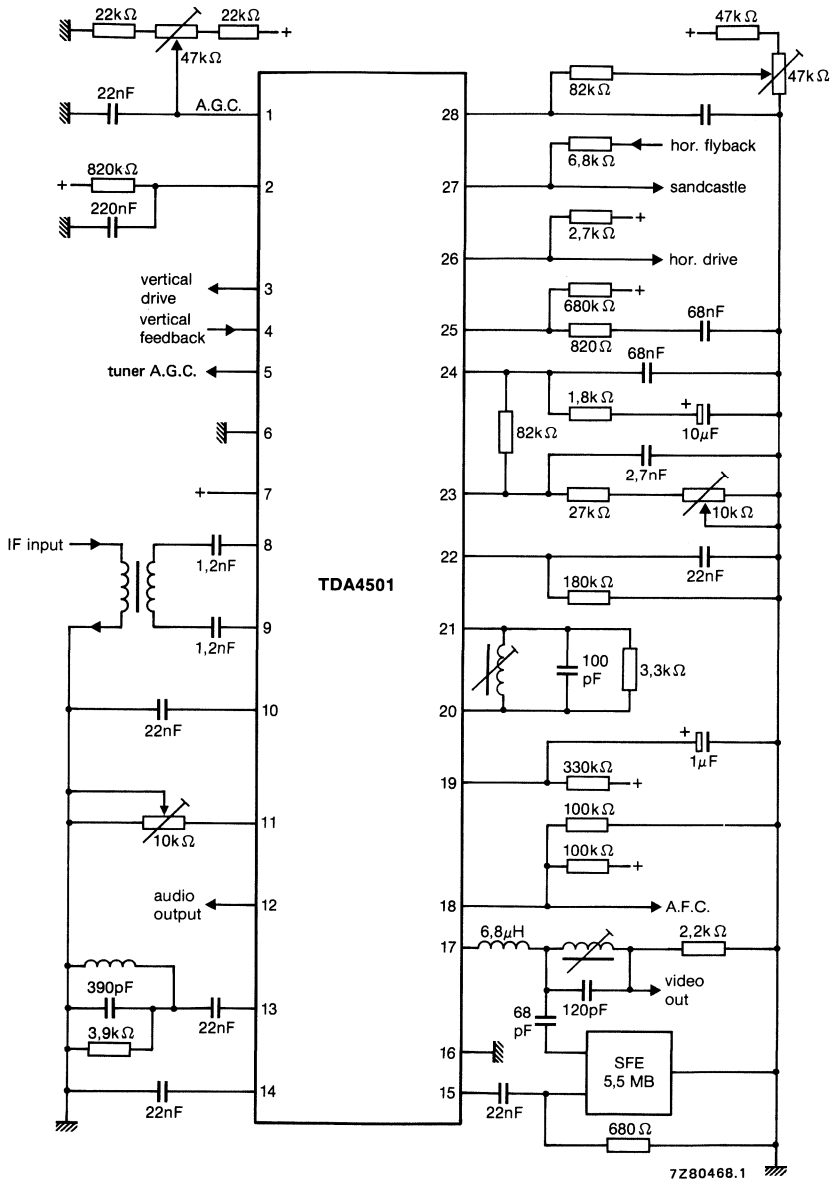


Fig. 2 Application diagram.

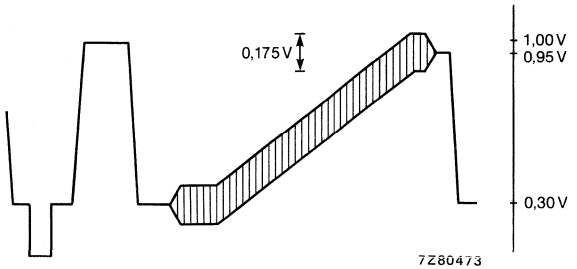


Fig. 3 Video output signal.

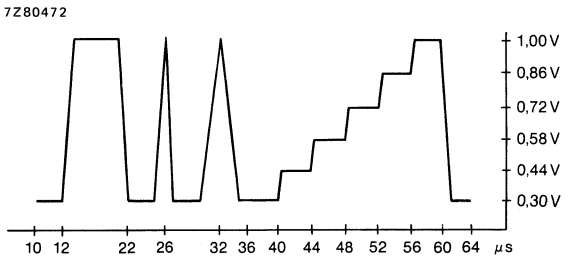


Fig. 4 E.B.U. test signal waveform (line 330).

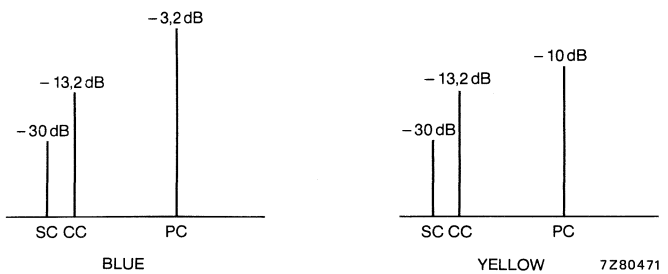


Fig. 5 Input signal conditions.
SC = sound carrier
CC = chrominance carrier
PC = picture carrier
all with respect to top sync level.

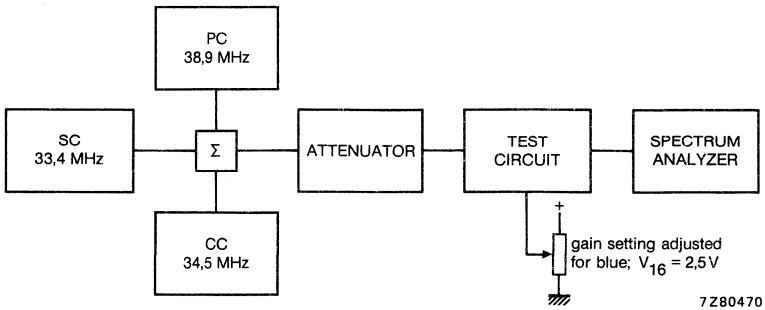


Fig. 6 Test set-up intermodulation.

Value at 1,1 MHz: $20 \log \frac{V_o \text{ at } 4{,}4 \text{ MHz}}{V_o \text{ at } 1{,}1 \text{ MHz}} + 3{,}6 \text{ dB}$

Value at 3,3 MHz: $20 \log \frac{V_o \text{ at } 4{,}4 \text{ MHz}}{V_o \text{ at } 3{,}3 \text{ MHz}}$.

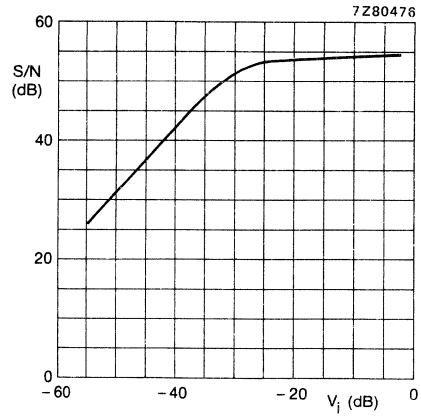


Fig. 7 S/N ratio as a function of the input voltage.

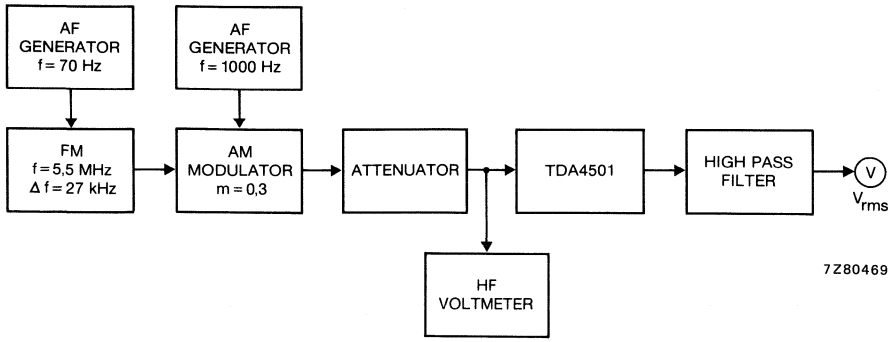


Fig. 8 Test set-up AM suppression.

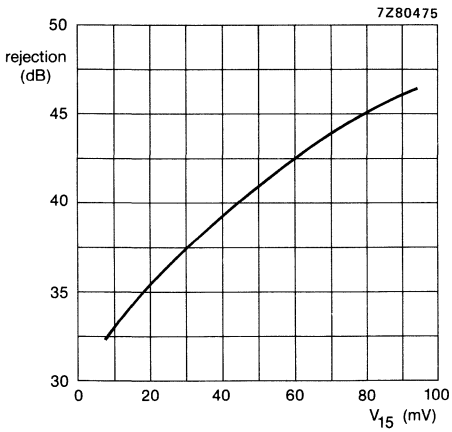


Fig. 9 AM rejection.

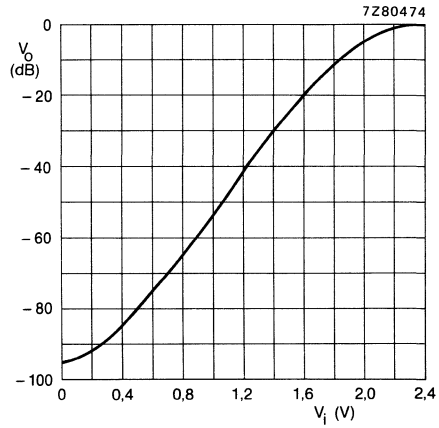


Fig. 10 Volume control characteristics.

SMALL SIGNAL COMBINATION FOR COLOUR TV

GENERAL DESCRIPTION

The integration into a single package of all small signal functions required for colour TV reception is achieved in the TDA4502A. The only additional circuits required for colour TV reception are the deflection output stages, a sound detector and amplifier, and a colour decoder.

The IC includes a vision IF amplifier and video switching circuit, AFC circuit, AGC detector with tuner output, an integral three-level sandcastle pulse generator, fully synchronized vertical and horizontal drive outputs and a mute circuit with external availability. A triggered vertical divider automatically adapts to 50 or 60 Hz operating mode thereby eliminating the need for external vertical frequency control. The sound signal must be demodulated and amplified externally.

Features

- Vision IF amplifier with synchronous demodulator
- AGC detector, suitable for negative modulation
- AGC output to tuner
- AFC circuit with ON/OFF switch
- Video preamplifier
- Video switch to select the internal, or an external, video signal
- Horizontal synchronization circuit with two control loops
- Vertical synchronization (divider system) and sawtooth generation with automatic amplitude adjustment for 50 and 60 Hz
- Transmitter identification (mute)
- Sandcastle pulse generator

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 7)	V_7	9.5	12	13.2	V
Supply current (pin 7)	I_7	–	125	–	mA
Supply current (pin 11)	V_{11}	–	6.0	8.5	mA
Operating ambient temperature range	T_{amb}	–25	–	+ 65	°C
Storage temperature range	T_{stg}	–25	–	+ 150	°C
Total power dissipation	P_{tot}	–	–	2.3	W

PACKAGE OUTLINE

28-lead DIL; plastic with internal heat spreader (SOT117).

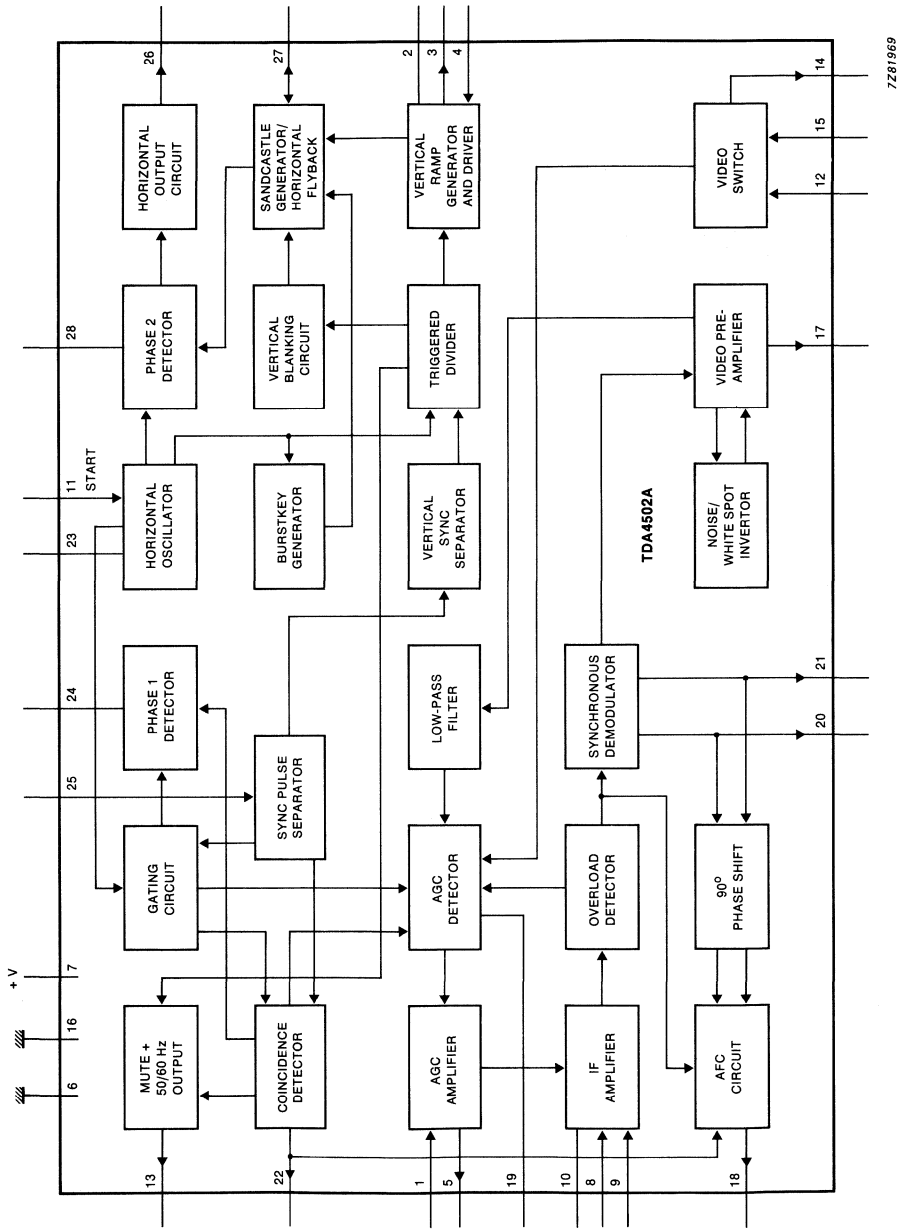


Fig. 1 Block diagram.

PINNING

1. AGC take over input
2. Ramp generator
3. Vertical drive output
4. Vertical feedback input
5. Tuner AGC output
6. Ground
7. Supply
8. IF input
9. IF input
10. Decoupling capacitor
11. Start horizontal oscillator input
12. External video input
13. Mute output
14. Video switch output
15. Internal video and switch input
16. Ground
17. Video output
18. AFC output
19. AGC detection
20. Synchronous demodulator output
21. Synchronous demodulator output
22. Coincidence detector output
23. Horizontal oscillator
24. Phase 1 detector
25. Sync separator
26. Horizontal drive output
27. Sandcastle output/flyback input
28. Phase 2 detector

FUNCTIONAL DESCRIPTION

IF amplifier, synchronous demodulator and AFC

The IF amplifier (pins 8 and 9) has a symmetrical input, the impedance of which enables SAW-filtering to be used. The synchronous demodulator and the AFC circuit share an external reference tuned circuit (pins 20 and 21). An internal RC-network provides the necessary phase-shift for AFC operation. The AFC circuit provides a control voltage output with a voltage swing greater than 9 V at pin 18. In the internal and external mode the AFC can be switched OFF when pin 22 is connected to positive supply.

AGC circuit

AGC gating is performed to reduce sensitivity of the IF amplifier to external noise. The AGC time constant is provided by an RC-circuit connected to pin 19. The tuner AGC voltage is supplied from pin 5. The point of tuner take-over is preset by the voltage level at pin 1.

Video switch circuit

The IC has a video switch with two video inputs and one video output. One input is connected to the demodulated IF signal which is also fed to the video output pin of the peritelevision connector. The other input can be switched to an external signal which is applied to the video input of the peritelevision connector. The video output signal of the switch is fed to pin 25 of the IC, which is the synchronization part and, to the colour decoder. When the video switch is in the external mode, the synchronization circuit is switched to the external signal. The vision IF, AGC and AFC circuits will not be affected by the switching action and will, therefore, operate in the normal mode. Gating for the AGC detector is switched OFF when the switch is in the external mode. The first control loop is not switched to a low time constant when weak signals are received.

Horizontal oscillator start function

The horizontal oscillator start function is achieved by applying a current of 8.5 mA to pin 11 during the switch-on period. This current can be taken from the mains rectifier. The main supply, pin 7, can then be obtained from the horizontal output stage. The load current of the driver has to be added to the start current.

Horizontal synchronization

The positive video input signal is applied to pin 25. The horizontal synchronization has two control loops which have been introduced to generate a sandcastle pulse. By using the oscillator sawtooth, an accurate timing of the burst-key pulse can be made. Therefore, the phase of this sawtooth pulse must have a fixed relationship to the sync pulse.

Horizontal phase detector

The circuit has two operating conditions:

(a) Synchronized
The first loop has a fixed time constant and a gated phase detector, this enables optimum performance for co-channel interference. The VCR mode is obtained by an additional load on pin 22.

(b) Non-synchronized
In this condition the time constant is the same as during the VCR mode.

Vertical sync pulse

The vertical sync pulse integrator will not be disturbed when the vertical sync pulses have a width of 10 μs and a separation of 22 μs. This type of vertical sync pulse is generated by video tapes with anti-copy guard.

Vertical divider system

A synchronized divider system generates the vertical sawtooth waveforms at pin 2. The system uses an internal frequency doubler circuit to enable the horizontal oscillator to operate at its normal line frequency. One line period equals 2 clock pulses.
Using the divider system avoids the requirement for vertical frequency adjustment. The divider has a discriminator window for automatic switching from 50 Hz to 60 Hz mode. When the trigger pulse arrives before line 576 the 60 Hz mode is selected, if not, the 50 Hz mode is selected.
The divider system operates with two different reset windows to give maximum interference/disturbance protection. The windows are activated via an up/down counter.
The counter is increased by 1 each time the separated vertical sync pulse is within the narrow window. When the sync pulse is not within the narrow window the counter is decreased by 1.
The operation modes of the divider system are as follows:

Mode A

Large (search) window (divider ratio between 488 and 722)

This mode is valid for the following conditions:

- Divider is looking for a new transmitter
- Divider ratio found — not within the narrow window limits
- A non-standard composite video signal is detected — when a double or enlarged vertical sync pulse is detected after the internally generated anti-top-flutter pulse has ended. This means a vertical sync pulse width $>$ 10 clock pulses (50 Hz); $>$ 12 clock pulses (60 Hz). This mode is normally activated for video tape recorders operating in the feature trick mode
- Up/down counter value of the divider system, operating in the narrow window mode, drops below count 6

Mode B

Narrow window (divider ratio between 522 to 528 (60 Hz) or 622 to 628 (50 Hz))

The divider system switches over to this mode when the up/down counter has reached its maximum value of 15 approved vertical sync pulses. When the divider operates in this mode and, a vertical sync pulse is missing within the window, the divider is reset at the end of the window and the counter value is decreased by 1. At a counter value below 6 the divider system switches over to the large window mode.
The divider system also generates an anti-top-flutter pulse which inhibits the Phase 1 detector during the vertical sync pulse. The pulse width is dependent on the divider mode. In 'Mode A' the start is generated by resetting the divider. In 'Mode B' the anti-top-flutter pulse starts at the beginning of the first equalizing pulse. The anti-top-flutter pulse ends at count 10 for the 50 Hz mode and count 12 for the 60 Hz mode.
The vertical blanking pulse is also generated via the divider system. The start is initiated by resetting the divider while the blanking pulse width is at count 34, (17 lines), for the 60 Hz mode and at count 42, (21 lines), for the 50 Hz mode. The vertical blanking pulse, at the sandcastle output (pin 27), is generated by adding the anti-top-flutter pulse to the blanking pulse. When the divider operates in 'Mode B', the vertical blanking pulse starts at the beginning of the first equalizing pulse. The length of the vertical blanking in this condition is 21 lines in the 60 Hz mode and 25 lines in the 50 Hz mode.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	$V_P = V_{7-6}$	–	13.2	V
Total power dissipation	P_{tot}	–	2.3	W
Operating ambient temperature range	T_{amb}	–25	+ 65	°C
Storage temperature range	T_{stg}	–25	+ 150	°C

CHARACTERISTICS

$V_P = V_7 = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified; all voltages are referenced to ground (pin 6) unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage (pin 7)		V_7	9.5	12.0	13.2	V
Supply current (pin 7)		I_7	–	125	–	mA
Supply current (pin 11)	note 1	I_{11}	–	6	8.5	mA
Vision IF amplifier (pins 8 and 9)						
Input sensitivity at 38.9 MHz	note 2	V_8	40	80	120	μV
Input sensitivity at 45.75 MHz	note 2	V_8	–	100	–	μV
Differential input resistance (pin 8 to pin 9)	note 3	R_{8-9}	0.8	1.3	1.8	kΩ
Differential input capacitance (pin 8 to pin 9)	note 3	C_{8-9}	–	5	–	pF
Gain control range		G_{8-9}	–	62	–	dB
Maximum input signal		V_{8-9}	50	100	–	mV
Expansion of output signal for 50 dB variation of input signal	note 4	ΔV_{17}	–	1	–	dB
Video amplifier	note 5					
Output level for zero signal input	note 6	V_{17}	3.3	3.7	4.1	V
Output signal top sync level		V_{17}	1.5	1.7	1.9	V
Amplitude of video output signal (peak-to-peak value)	note 7	$V_{17(p-p)}$	1.4	1.8	2.2	V
Internal bias current of output transistor (npn emitter follower)		$I_{17(int)}$	1.4	2.0	–	mA
Bandwidth of demodulated output signal		B	4.0	5.0	–	MHz
Differential gain	note 8	G_{17}	–	5	10	%
Differential phase	note 8	φ	–	5	10	%

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Video non-linearity	note 9	NL	–	5	12	%
Intermodulation	note 10					
f = 1.1 MHz; blue			47	50	–	dB
f = 1.1 MHz; yellow			45	47	–	dB
f = 3.3 MHz; blue			50	55	–	dB
f = 3.3 MHz; yellow			48	52	–	dB
Signal-to-noise ratio	note 11					
input signal = 10 mV		S/N	45	50	–	dB
end of gain control range as a function of input voltage	see Fig. 5	S/N	50	55	–	dB
Residual carrier signal			–	7	30	mV
Residual 2nd harmonic of carrier signal			–	15	30	mV
Video switching circuit	note 12					
External video input (positive video; pin 12)						
Input signal (peak-to-peak value)	V_o = 2.4 $V_{(p\text{-}p)}$	$V_{12\ (p\text{-}p)}$	–	0.9	–	V
Input current		I_{12}	–	3.5	–	μA
Top sync clamping level		V_{12}	–	3.4	–	V
Video output (positive video; pin 14)						
Output signal		V_{14}	2.2	2.4	2.6	V
Top sync level		V_{14}	2.4	3.0	3.6	V
Internal bias current npn output transistor		I_{14}	0.8	–	–	mA
Crosstalk of video signal	measured at 4.4 MHz					
external to internal		α	50	55	–	dB
internal to external		α	42	46	–	dB
Internal video and switch input (pin 15)						
Amplitude of input signal (peak-to-peak value)	V_o = 2.4 $V_{(p\text{-}p)}$	$V_{15\ (p\text{-}p)}$	–	1.8	–	V
Input current		I_{15}	–	7	–	μA
Top sync clamping level (via 100 kΩ to ground)		V_{15}	–	4.2	–	V
Condition for internal signal	note 12					
Condition for external signal (via 100 kΩ to positive supply)		V_{15}	–	10	12	V

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Tuner AGC						
Minimum starting point take over* (RMS value)	I = 0.2 mA	$V_{1(rms)}$	–	–	0.5	mV
Maximum starting point take over* (RMS value)	I = 0.2 mA	$V_{1(rms)}$	50	100	–	mV
Maximum output swing		I_{5max}	6	8	–	mA
Output saturation voltage	I = 2 mA	$V_{5(sat)}$	–	100	300	mV
Leakage current		I_5	–	0.7	1.0	μA
Input signal variation complete tuner control	ΔI_5 = 2 mA	ΔV_i	0.1	2.0	5.0	dB
Minimum voltage take over (pin 1)		V_1	–	–	1	V
AFC circuit (pin 18)	note 13					
AFC output voltage swing (peak-to-peak value)		$V_{18(p-p)}$	9.5	10.2	11.5	V
Available output current		I_{18}	–	± 2.2	–	mA
Control steepness			70	100	150	mV/kHz
Output voltage at nominal tuning of the reference tuned circuit		V_{18}	–	6	–	V
Offset current AFC output (pins 20 and 21 short-circuited)		I_{18}	–	0	± 220	μA
Horizontal synchronization	Fig. 7					
Sync separator and first control loop (pin 25)						
Sync pulse amplitude	note 14	V_{25}	200	–	–	mV
Input current	V_{25} = > 5 V	I_{25}	–	10	–	μA
Input current	V_{25} = 0 V	I_{25}	–	−10	–	mA
Holding range PLL		Δf	–	± 1.1	± 1.5	kHz
Catching range PLL		Δf	+ 0.6	± 1.0	–	kHz
Control sensitivity	note 15					
in sync condition		Δ_{td}	–	2.5	–	kHz/μs
in non-sync condition		Δ_{td}	–	7.5	–	kHz/μs
Second control loop (positive edge)						
Control sensitivity	note 16	$\Delta t_d/\Delta to$	–	50	–	
Control range		t_d	–	25	–	μs

* Take over to be adjusted by a potentiometer with a value of 47 kΩ.

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Phase adjustment (via second control loop)						
Control sensitivity			–	25	–	$\mu A/\mu s$
Maximum allowed phase shift		α	–	± 2	–	μs
Horizontal oscillator (pin 23)						
Free running frequency	R = *; C = 2.7 nF	f_{fr}	–	15625	–	Hz
Spread with fixed external components		Δ_f	–	–	4	%
Frequency variation due to change of supply voltage from 9.5 to 13.2 V		Δf_{fr}	–	0	0.5	%
Frequency variation with temperature		TC	–	–	1.6	Hz/°C
Maximum frequency shift		Δf_{fr}	–	4	10	%
Maximum frequency deviation at start horizontal out		Δf_{fr}	0	+ 8	+ 10	%
Horizontal output (pin 26)						
Output voltage high		V_{26}	–	–	13.2	V
Output voltage at which protection commences		V_{26}	–	–	15.8	V
Output voltage low	I_{26} = 10 mA	V_{26}	–	0.3	0.5	V
Duty factor of horizontal output signal	t_p = 10 μs	d	–	45	–	%
Duty factor during start-up		d	–	52	–	%
Rise time of output pulse		t_r	–	260	–	ns
Fall time of output pulse		t_f	–	100	–	ns
Horizontal flyback input and sandcastle output	note 17					
Input current required during flyback pulse		I_{27}	0.1	–	2.0	mA
Output voltage						
during burst-key pulse		V_{27}	8.4	9.0	–	V
during horizontal blanking		V_{27}	4.1	4.35	5.0	V
during vertical blanking		V_{27}	2.1	2.4	2.7	V

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Horizontal flyback input and sandcastle output (continued)						
Pulse width						
burst-key pulse	60 Hz	t_W	3.1	3.45	3.9	μs
burst-key pulse	50 Hz	t_W	3.5	3.8	4.4	μs
horizontal blanking pulse			flyback pulse width			
vertical blanking pulse						
50 Hz divider in search window			–	21	–	lines
60 Hz divider in search window			–	17	–	lines
50 Hz divider in narrow window			–	25	–	lines
60 Hz divider in narrow window			–	21	–	lines
Delay between start of sync pulse at video output and trailing edge of burst-key pulse			–	–	9.2	μs
Coincidence detector mute output (pin 22)	Fig 6; note 18					
Voltage for in-sync condition		V_{22}	8.5	10.0	10.5	V
Voltage for no-sync condition	no signal	V_{22}	0	0.3	0.6	V
Switching level to switch phase detector from slow to fast		V_{22}	4.9	5.3	5.8	V
Hysteresis		V_{22}	–	0.6	–	V
Voltage for AFC switch-off		V_{22}	–	10.5	11.0	V
Switching level to activate mute function		V_{22}	2.25	2.5	2.75	V
Hysteresis mute function		V_{22}	–	0.6	–	V
Output current (peak-to-peak value)	in-sync	$I_{22(p-p)}$	0.7	1.0	–	mA
Discharge current (peak-to-peak value)		$I_{22(p-p)}$	–	0.5	–	mA
Video transmitter identification output (pin 13)						
Output voltage active	no-sync; $I = 5$ mA	V_{13}	–	0.3	0.5	V
Output current active		I_{13}	–	–	5	mA
Output current inactive	sync	I_{13}	–	–	1	μA

parameter	conditions	symbol	min.	typ.	max.	unit
50/60 Hz identification (pin 13)						
Output voltage						
50 Hz		V_{13}	9	12	–	V
60 Hz		V_{13}	4.7	6.0	6.4	V
Vertical ramp generator (pin 2)	note 19					
Input current during scan		I_2	–	1	2	μA
Discharge current during retrace		I_2	0.3	0.35	–	mA
Sawtooth amplitude (peak-to-peak value)		$V_{2(p-p)}$	–	0.8	1.1	V
Vertical drive output (pin 3)						
Maximum available output current		I_3	1.5	3.5	–	mA
Maximum output voltage		V_3	–	4	–	V
Vertical feedback input (pin 4)						
Input voltage DC component		V_4	2.4	3.0	4.1	V
AC component (peak-to-peak value)		$V_{4(p-p)}$	–	1.2	–	V
Input current		I_4	–	–	12	μA
Internal precorrection to sawtooth		Δt_p	–	6	–	%
Deviation amplitude	50/60 Hz		–	–	2	%
Vertical guard	note 20					
Active at a deviation with respect to the DC feedback level	V_{27} = 2.5 V					
switching voltage level LOW		ΔV_4	0.6	0.9	–	V
switching voltage level HIGH		ΔV_4	–	2	–	V

DEVELOPMENT DATA

Notes to the characteristics

1. The horizontal oscillator can be started when a current of 8.5 mA is applied to pin 11; this current can be taken from the mains rectifier. The main supply (pin 7) can then be derived from the horizontal output stage. The load current of the driver must be added to the start current (8.5 mA).
2. On set AGC.
3. Input impedance selected so that a SAW-filter can be applied.
4. Measured with 0 dB = 150 μV.
5. Measured at 10 mV(rms) top sync input signal.
6. Projected zero point with switched demodulator.
7. Signal with negative going sync top white level 10% of the top sync amplitude.
8. Measured in accordance with the test line given in Fig. 2.
   The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier amplitude at blanking level.
   The differential phase is defined as the difference in degrees between the largest and smallest phase angle.

Notes to the characteristics (continued)

9. This figure is valid for the complete video signal amplitude (peak white to black) and measured with a 6.6 kΩ damping resistor connected between pins 20 and 21 (see Fig. 3).
10. The test set-up and input conditions are given in Fig. 4. The figures are measured at an input signal of 10 mV(rms).
11. Measured with a source impedance of 75 Ω, where:
$$S/N = 20 \log \frac{V_o \text{ black-to-white}}{V_{n(rms)} \text{ at } B = 5 \text{ MHz}}.$$
12. The internal video and video switch inputs are applied to pin 15. By externally connecting the internal video signal to the video switch enables the sound trap to be connected between pins 15 and 17. When the video signal is applied internally to the switch then sound traps are required at two outputs. The switch is activated via a 100 kΩ resistor. When the resistor is connected to ground or left open-circuit the internal video signal is available at pin 14. When the resistor is connected to + V_S the external video signal is available at pin 14. When the video switch is in the external mode the AFC can still be switched off when pin 22 is connected to the supply voltage.
13. The measured figures are obtained at an input signal of 10 mV(rms) and the AFC output loaded with 2 x 100 kΩ between the supply voltage and ground. The unloaded Q-factor of the reference tune circuit is 70. The AFC is switched off when pin 22 is connected to the supply voltage.
14. The minimum value is obtained by connecting a 1.8 kΩ series resistor between pins 14 and 25. The slicing level can be varied by changing the value of this resistor (a higher resistor value will result in a higher value of the minimum sync pulse amplitude). The slicing level is independent of the video information.
15. Frequency control is obtained by supplying a correction current to the oscillator RC network via a resistor between pins 23 and 24. The oscillator can be adjusted to the correct frequency using either of the following methods:

    (a) Interrupt the resistor between pins 23 and 24.
    (b) Short-circuit the sync separator bias network (pin 25 to supply voltage).

    The device uses a long time constant for the first phase detector. The phase detector is gated to obtain optimal performance for co-channel interference. The VCR mode must be switched on via pin 22.
16. This figure is valid for an external load impedance of 82 kΩ connected between pin 28 and the shift-adjustment potentiometer.
17. The flyback input and sandcastle output are combined at pin 27. The flyback pulse is clamped to a level of 4.35 V. The minimum current required to drive the second control loop is 0.1 mA.
18. The functions in-sync/out-of-sync and transmitter identification are combined at pin 22. The 22 nF capacitor is charged during the sync pulse and discharged during the time difference between gating and sync pulse.
19. Because the vertical scan is synchronized via a divider system, no adjustment is required for the ramp generator. The divider system detects whether the incoming signal has a vertical frequency of 50 or 60 Hz and subsequently corrects the vertical amplitude.
20. To avoid screenburn, due to a collapse of the vertical deflection, a continuous blanking level is inserted in the sandcastle pulse when the feedback voltage from the vertical deflection is not within the specified limits.

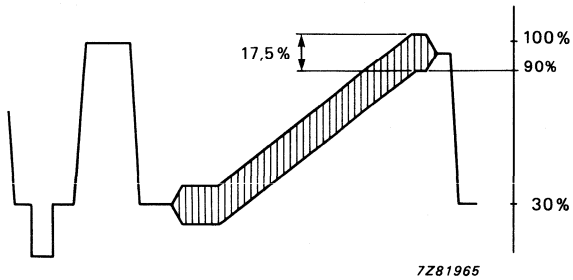


Fig. 2 Video output signal.

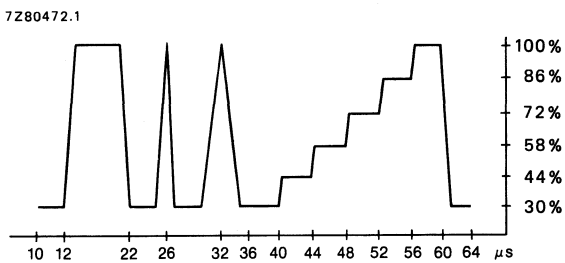
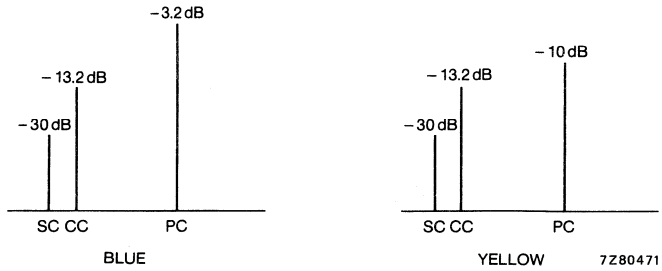


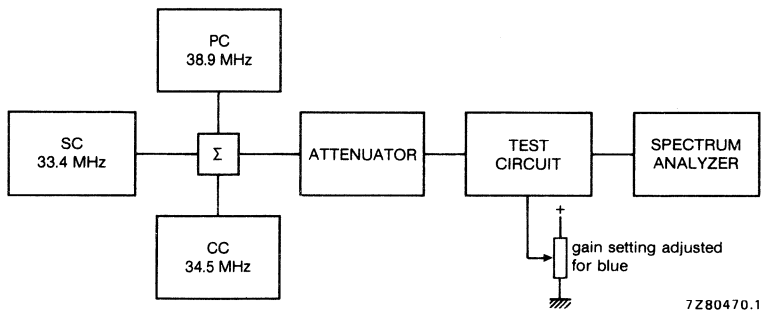
Fig. 3 EBU test signal waveform (line 330).



Input signal conditions:

SC = sound carrier
CC = chrominance carrier
PC = picture carrier

all with respect to top sync level.



Where:

$$\text{Value at 1.1 MHz: } 20 \log \frac{V_o \text{ at } 4.4 \text{ MHz}}{V_o \text{ at } 1.1 \text{ MHz}} + 3.6 \text{ dB}$$

$$\text{Value at 3.3 MHz: } 20 \log \frac{V_o \text{ at } 4.4 \text{ MHz}}{V_o \text{ at } 3.3 \text{ MHz}}$$

Fig. 4 Test set-up intermodulation.

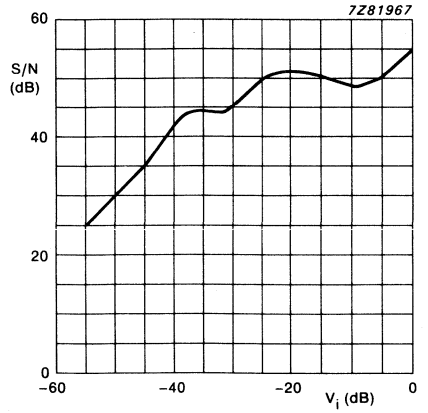
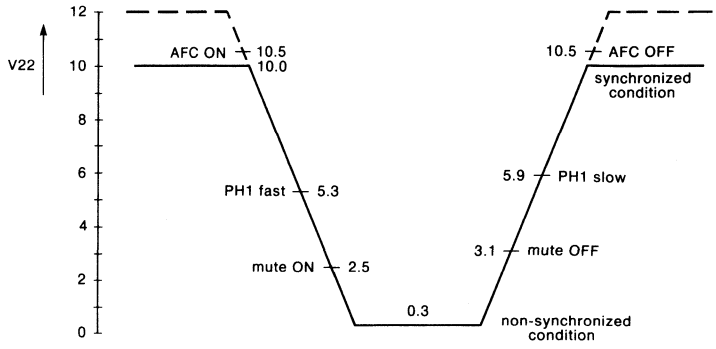


Fig. 5 S/N ratio as a function of the input voltage (0 dB = 100 mV).

DEVELOPMENT DATA



condition	control sensitivity horizontal oscillator kHz/μs		vertical sync separator pulse after
	T2 – T1	T3 = scan	
V22 > 5.9 and			
strong signal	2.5	2.5	16 μs
weak signal	2.5	2.5	9 μs
V22 < 5.3 and			
strong signal	7.5	7.5	16 μs
weak signal	7.5	7.5	9 μs

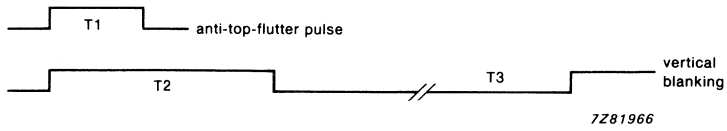
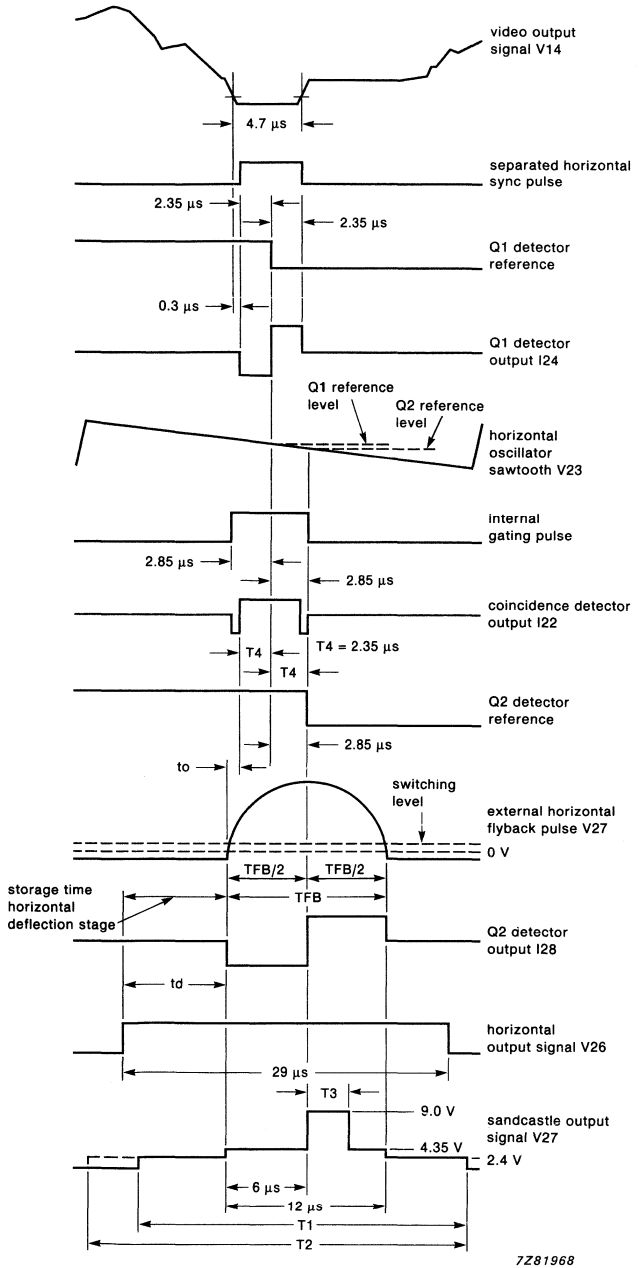


Fig. 6 Switching levels coincidence detector.

DEVELOPMENT DATA



	50 Hz	60 Hz
T1 – Search window	42P	34P
T2 – Narrow window	50P	42P
T3	3.8 µs	3.45 µs

Where: $P = \frac{1}{2 F_H}$

Fig. 7 Timing diagram.

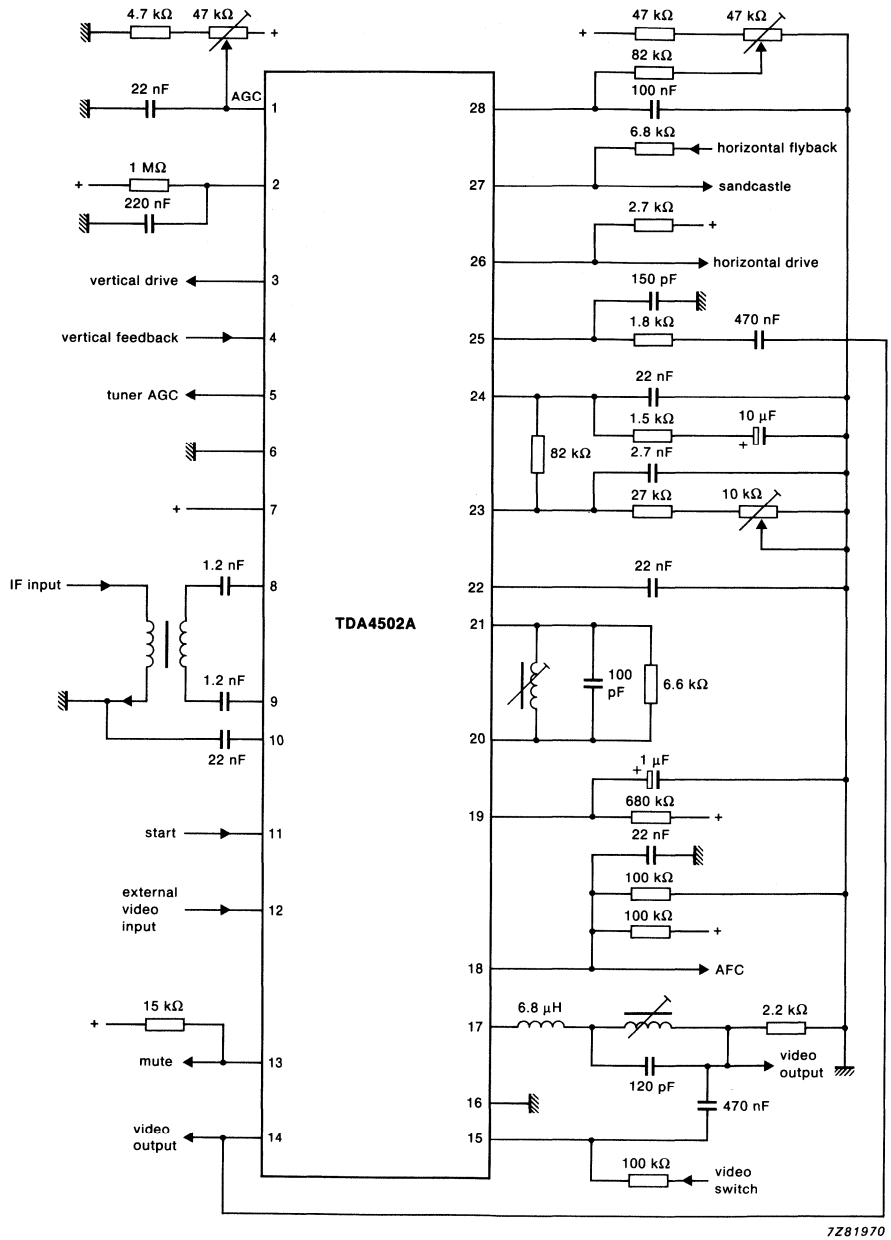


Fig. 8 Application diagram.

SMALL-SIGNAL COMBINATION IC FOR BLACK-AND-WHITE TV

GENERAL DESCRIPTION

This IC contains all small-signal functions required for black-and-white tv reception. The only additional circuits needed to complete the receiver are a tuner and the deflection output stages.

The IC includes a vision i.f. amplifier with synchronous demodulator and a.f.c. circuit, an a.g.c. detector with tuner output and fully synchronized vertical and horizontal drive outputs.

Sound signals are demodulated and amplified within the IC in a circuit which includes volume control and internal muting.

The TDA4503 may also be adapted for simple colour tv reception by the use of an external, three-level sandcastle pulse generator.

Features

- Vision i.f. amplifier with synchronous demodulator
- A.G.C. detector and amplifier with a.g.c. output to tuner
- A.F.C. circuit
- Video preamplifier
- Audio preamplifier
- Sound i.f. amplifier and demodulator
- D.C. volume control
- Horizontal synchronization circuit
- Transmitter identification and mute circuit
- Vertical synchronization circuit and sawtooth generator

QUICK REFERENCE DATA

Supply voltage (pin 7)	$V_{7\text{-}10}$	typ.	10,5 V
Supply current (pin 7)	I_7	typ.	82 mA
Supply voltage (pin 22)	$V_{22\text{-}10}$	typ.	10,5 V
Supply current (pin 22)	I_{22}	typ.	5 mA
Operating ambient temperature range	T_{amb}		−25 to + 65 °C
Storage temperature range	T_{stg}		−25 to +150 °C
Power dissipation	P_{tot}	typ.	920 mW

PACKAGE OUTLINE

28-lead DIL; plastic (with internal heat spreader) (SOT117).

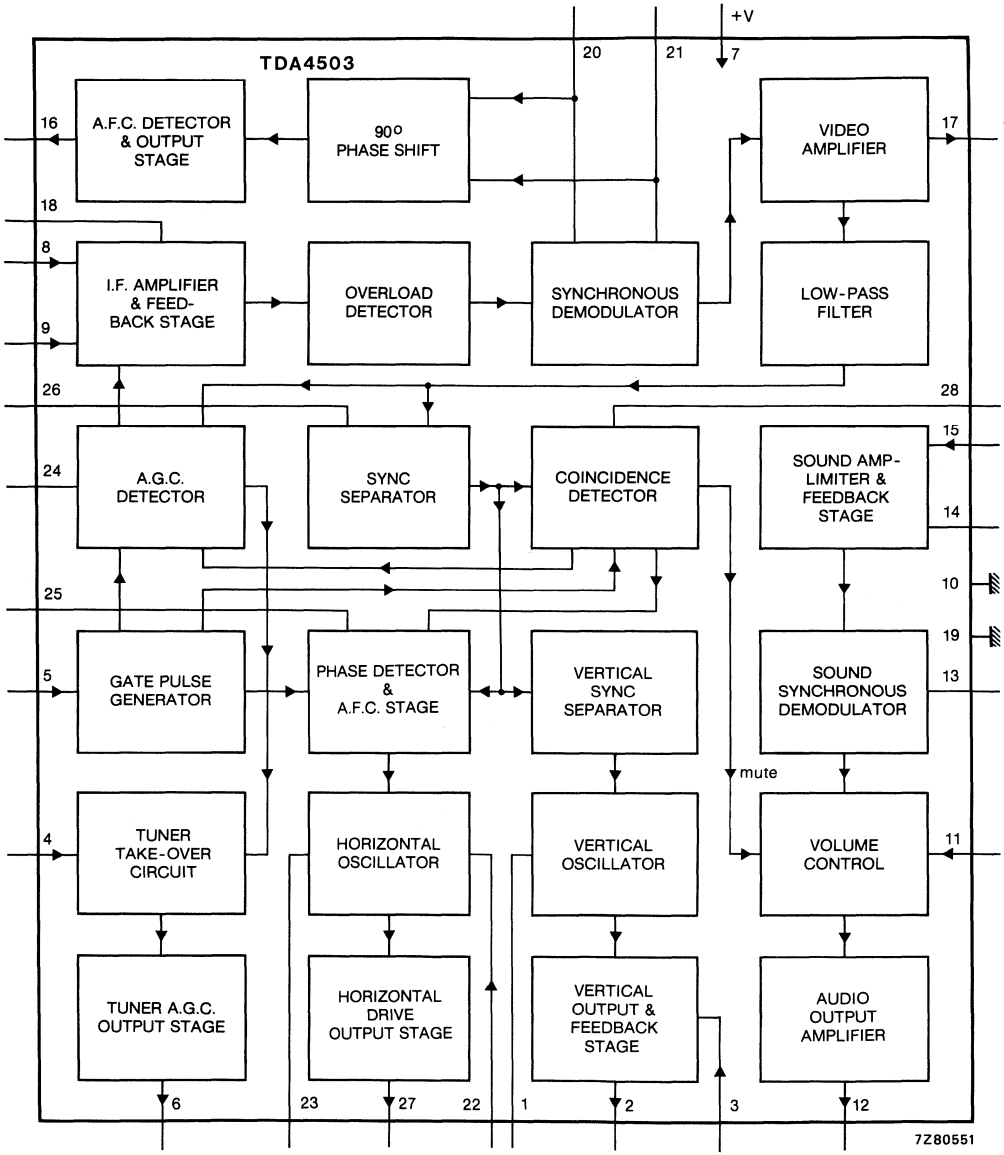


Fig. 1 Block diagram.

PINNING

1. Vertical oscillator input
2. Vertical drive output
3. Vertical drive feedback
4. Tuner take-over input
5. Flyback pulse input
6. A.G.C. output to tuner
7. Power supply input
8. I.F. input
9. I.F. input
10. Power supply return (ground)
11. Volume control
12. Audio output
13. Sound demodulator reference input
14. Sound i.f. decoupling
15. Sound i.f. input
16. A.F.C. output
17. Video output
18. I.F. amplifier decoupling
19. Ground (for critical circuits)
20. Synchronous demodulator
21. Synchronous demodulator
22. Horizontal oscillator start input
23. Horizontal oscillator
24. A.G.C. time constant
25. Horizontal phase detector filter
26. Sync separator slicing level
27. Horizontal drive output
28. Coincidence detector time constant

FUNCTIONAL DESCRIPTION

I.F. amplifier, demodulator and A.F.C.

The i.f. amplifier operates with symmetrical inputs at pins 8 and 9 and has an input impedance suitable for SAW filter application. The amplifier sensitivity gives a peak-to-peak output voltage of 3 V for an r.m.s. input of 70 μV. The demodulator and the a.f.c. circuit share an external reference tuned circuit (pins 20 and 21) and an internal RC-network provides the phase-shifting necessary for a.f.c. operation. The a.f.c. circuit provides a control voltage output with a (typical) swing of 9 V from pin 16 (V_P = 10,5 V).

A.G.C. circuit

Gating of the a.g.c. detector is performed to reduce sensitivity of the i.f. amplifier to external electrical noise. The a.g.c. time constant is provided by an RC-network connected to pin 24. The typical gain control range of the i.f. amplifier is 60 dB. Tuner a.g.c. voltage is supplied from pin 6 and is suitable for tuners with pnp or npn RF stages. The sense of the AGC (to incease in a positive or negative direction) and the point of tuner take-over are preset by the voltage level at pin 4 (V_4 = 3,5 V (typ) for positive a.g.c.; V_4 = 8 V (typ) for negative a.g.c.).

Video amplifier

The video signal output from pin 17 has a peak-to-peak value of 3 V (top sync level = 1,5 V) and carries negative-going sync. In order to retain sound information at pin 17, the video signal is not blanked during flyback periods.

Sound circuit

The sound i.f. signal present at the video output (pin 17) is coupled to the sound circuit by a band-pass filter to pin 15. The sound circuit has an amplifier-limiter stage, a synchronous demodulator with reference tuned circuit at pin 13, a volume control stage and an output amplifier. The volume control has a range of approximately 80 dB and the audio output signal at maximum volume and with Δf = 7,5 kHz is 320 mV (r.m.s. value). The sound output signal is suppressed when no input signal is detected.

Synchronization circuits

The sync separator slicing level is determined by an external resistor network at pin 26. The slicing level is referred to the top sync level and the recommended value for slicing is 30%. Internal protection from electrical noise is included.

A gated phase detector compares the phase of the separated sync pulses with a sawtooth waveform obtained from the flyback pulse at pin 5. In-sync and out-of-sync conditions are detected by the coincidence detector at pin 28 (this circuit also gives transmitter identification). During the out-of-sync condition, gating of the phase detector is switched off and the output current from the phase detector increases to give the detector a short time-constant and thus a fast response. This condition can be imposed by clamping the voltage at pin 28 to 3,5 V for the reception of VCR signals.

The horizontal oscillator frequency is controlled by the output voltage of the phase detector circuit. The horizontal drive output from pin 27 has a duty factor of 40%.

Vertical sync pulses are separated by an internal integrating network and are used to trigger the vertical oscillator. A comparator circuit compares the vertical sawtooth waveform, generated by the vertical oscillator, with feedback from the deflection coils and supplies the drive voltage for the output stage at pin 2.

Power supplies

The main supply is to pin 7 (positive supply) and pin 10 (ground). The horizontal oscillator is supplied from pin 22 to facilitate starting of the oscillator from a high-voltage rail. A special ground connection at pin 19 is used by critical voltage dividers in the feedback loops of the vision and sound i.f. circuits.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 7)	$V_P = V_{7-10}$	max.	13,2 V
Total power dissipation	P_{tot}	max.	1,7 W
Operating ambient temperature range	T_{amb}		−25 to + 65 °C
Storage temperature range	T_{stg}		−25 to +150 °C

CHARACTERISTICS

V_{7-10} = 10,5 V; V_{22-10} = 10,5 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage (pin 7)	V_{7-10}	9,5	10,5	13,2	V
Supply current (pin 7)	I_7	–	82	100	mA
Supply voltage (pin 22)	V_{22-10}	9,5	10,5	13,2	V
Supply current (pin 22) (note 1)	I_{22}	–	5	6,5	mA
Total power dissipation	P_{tot}	–	920	1150	mW
Vision i.f. amplifier (pins 8 and 9)					
Input sensitivity at 38,9 MHz (note 2)	V_{8-9}	40	80	120	μV
Input sensitivity at 45,75 MHz (note 2)	V_{8-9}	–	90	–	μV
Differential input resistance (pin 8 to 9)	R_{8-9}	–	1,3	–	kΩ
Differential input capacitance (pin 8 to 9)	C_{8-9}	–	5	–	pF
A.G.C. range		–	59	–	dB
Maximum input signal	V_{8-9}	50	70	–	mV
Expansion of output signal (pin 17) for 50 dB variation of input signal (pins 8 and 9) (note 3)	ΔV_{17-10}	–	0,5	1,0	dB
Video amplifier (note 4)					
Output level for zero signal input (zero point of switched demodulator)	V_{17-10}	4,2	4,5	4,8	V
Output signal top sync level (note 5)	V_{17-10}	1,25	1,45	1,65	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Amplitude of video output signal (peak-to-peak value)	$V_{17\text{-}10(p\text{-}p)}$	2,4	2,7	3,0	V
Internal bias current of output transistor (npn emitter follower)	$I_{17(int)}$	1,4	2,0	–	mA
Bandwidth of demodulated output signal	B	–	5	–	MHz
Differential gain (Fig. 4 and note 6)	G_{17}	–	6	–	%
Differential phase (Fig. 4 and note 6)		–	4	–	%
Video non-linearity over total video amplitude (peak white to black)		–	–	10	%
Intermodulation (Figs 5 and 6) at gain control = 45 dB					
f = 1,1 MHz; blue;		55	60	–	dB
f = 1,1 MHz; yellow;		50	54	–	dB
f = 3,3 MHz; blue;		60	66	–	dB
f = 3,3 MHz; yellow;		55	59	–	dB
Signal-to-noise ratio (note 7)					
at V_i = 10 mV	S/N	50	54	–	dB
at end of a.g.c. range	S/N	50	56	–	dB
as a function of input signal		see Fig. 7			
Residual A.M. of intercarrier output signal (note 8)		–	5	10	%
Residual carrier signal		–	7	30	mV
Residual 2nd harmonic of carrier signal		–	3	30	mV
Tuner a.g.c. (note 9)					
Take-over voltage (pin 4) for positive-going tuner a.g.c. (NPN tuner)	$V_{4\text{-}10}$	–	3,5	–	V
Starting point take-over at $V_{4\text{-}10}$ = 5 V (r.m.s. value)	$V_{8\text{-}9(rms)}$	–	0,4	2,0	mV
Starting point take-over at $V_{4\text{-}10}$ = 1,2 V (r.m.s. value)	$V_{8\text{-}9(rms)}$	50	70	–	mV
Take-over voltage (pin 1) for negative-going tuner a.g.c. (PNP tuner)	$V_{4\text{-}10}$	–	8	–	V
Starting point take over at $V_{4\text{-}10}$ = 9,5 V (r.m.s. value)	$V_{8\text{-}9(rms)}$	–	0,3	2,0	mV
Starting point take over at $V_{4\text{-}10}$ = 5,6 V (r.m.s. value)	$V_{8\text{-}9(rms)}$	50	70	–	mV
Maximum tuner a.g.c. output swing	I_{6max}	2	3	–	mA
Output saturation voltage at I_6 = 2 mA	$V_{6\text{-}10(sat)}$	–	–	300	mV
Leakage current at pin 6	I_6	–	–	1	μA
Input signal variation required for complete tuner control	$\Delta V_{8\text{-}9}$	0,5	2	4	dB

parameter	symbol	min.	typ.	max.	unit
A.F.C. circuit (pin 16; note 10)					
A.F.C. output voltage swing (peak-to-peak value)	$V_{16\text{-}10(p\text{-}p)}$	9	–	10	V
Available output current	$\pm I_{16}$	–	1	–	mA
Control steepness at					
100% picture carrier		20	40	80	mV/kHz
10% picture carrier		–	15	–	mV/kHz
Output voltage at nominal tuning of the reference tuned circuit	$V_{16\text{-}10}$	–	5,25	–	V
Output voltage without input signal	$V_{16\text{-}10}$	2,7	6,0	8,5	V
Sound circuit					
Input limiting voltage (note 11) (r.m.s. value) at $V_o = V_{o\ max}$ - 3 dB	$V_{15\ lim}$	–	2	–	mV
Input resistance at $V_{i(rms)}$ = 1 mV	$R_{15\text{-}10}$	–	2,6	–	kΩ
input capacitance at $V_{i(rms)}$ = 1 mV	$C_{15\text{-}10}$	–	6	–	pF
A.M. rejection (Figs 8 and 9) at					
V_i = 10 mV	AMR	–	35	–	dB
V_i = 50 mV	AMR	–	43	–	dB
A.F. output signal (note 12) (r.m.s. value)	$V_{12\text{-}6(rms)}$	220	320	–	mV
A.F. output impedance	$Z_{12\text{-}10}$	–	150	–	Ω
Total harmonic distortion (note 12)	THD	–	1	–	%
Ripple rejection at					
f_k = 100 Hz, volume control 20 dB	RR	–	22	–	dB
when muted	RR	–	26	–	dB
Output voltage in mute condition	$V_{12\text{-}10}$	–	2,6	–	V
Signal-to-noise ratio; weighted noise (CCIR 468)	S/N	–	47	–	dB
Volume control					
Voltage (pin 11 disconnected)	$V_{11\text{-}10}$	–	6,9	–	V
Current (pin 11 connected to ground)	I_{11}	–	1	–	mA
External control resistor (note 13)	$R_{11\text{-}10}$	–	5	–	kΩ
Suppression of output signal during mute condition		–	66	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Horizontal synchronization					
Slicing level sync separator (note 14)		–	30	–	%
Phase-lock loop holding range		±800	±1100	±1500	Hz
Phase-lock loop catching range		±600	1000	–	Hz
Control sensitivity video to flyback (note 15)		–	2,3	–	kHz/μs
Delay between leading edge of sync pulse and zero cross-over of sawtooth (pin 5)		–	3	–	μs
Horizontal oscillator (pin 23)					
Free-running frequency R = 35 kΩ; C = 2,7 nF	f_{fr}	–	15625	–	Hz
Spread with fixed external components		–	–	4	%
Frequency variation due to change of supply voltage from 8 to 12 V	Δf_{fr}	–	0	0,5	%
Temperature coefficient	TC	–	–	1×10^{-4}	K^{-1}
Maximum frequency shift	Δf_{fr}	–	–	10	%
Maximum frequency deviation(V_{7-10} = 8 V)	Δf_{fr}	–	–	10	%
Horizontal output (pin 27)					
Output current	I_{27}	5	–	–	mA
Output impedance	R_{27}	–	200	–	Ω
Output voltage at I_{27} = 5 mA	V_{27-10}	–	1,4	–	V
	V_{27-22}	–	2,5	–	V
Duty factor of horizontal output signal (note 16)	α	0,35	0,40	0,45	%
Rise and fall times of output pulse	t_r, t_f	–	400	–	ns
Flyback input (pin 5)					
Amplitude of input pulse	V_5	2	4	6	V
Voltage at which gate pulse generator changes state (note 17)	V_5	–	0	–	V

parameter	symbol	min.	typ.	max.	unit
Coincidence detector mute output (pin 28) (note 18)					
Voltage for in-sync condition	V_{28-10}	–	9,5	–	V
Voltage for no-sync condition (no input signal)	V_{28-10}	–	1,0	1,5	V
Voltage level for phase detector to switch from slow to fast	V_{28-10}	3,7	4,1	4,5	V
Fast-to-slow hysteresis		–	1	–	V
Voltage level to activate mute function (transmitter identification)	V_{28-10}	2,25	2,5	2,75	V
Output current for in-sync condition (peak-to-peak value)	$I_{22(p-p)}$	0,7	1,0	–	mA
Vertical oscillator (pin 1)					
Free-running frequency at C = 220 nF; R = 560 kΩ	f_{fr}	–	47,5	–	Hz
Spread with fixed external components		–	–	4	%
Holding range at nominal frequency		52,5	–	–	Hz
Temperature coefficient	TC	–	–	$2x10^{-4}$	K^{-1}
Frequency variation due to change of supply voltage from 9,5 to 12 V	Δf_{fr}	–	3	5	%
Leakage current at pin 1	I_1	–	–	1,6	μA
Vertical output (pin 2)					
Output current	I_2	1	1,3	–	mA
Output resistance	R_2	–	2	–	kΩ
Feedback input (pin 3)					
Input voltage					
d.c. component	V_{3-10}	4,0	5,0	5,5	V
a.c. component (peak-to-peak value)	$V_{3-10(p-p)}$	–	1,2	–	V
Input current	I_3	–	–	12	μA
Non-linearity of deflection current at V_{7-10} = 10,5 V	ΔI_3	–	–	2,5	%
Delay between leading edge of vertical sync and start of vertical oscillator flyback		6	–	10	μs

Notes to the characteristics

1. The horizontal oscillator can be started by supplying a current of 6 mA to pin 22. Taking this current from the mains rectifier allows the positive supply voltage to pin 7 to be derived from the horizontal output stage (the load current of pin 27 is additional to the 6 mA quoted).
2. At start of a.g.c.
3. Measured with 0 dB = 200 μV.
4. Measured at 10 mV (rms) top sync output signal.
5. Signal with negative-going sync; top white = 10% of the top sync amplitude.
6. Measured with test line as shown in Fig. 4. The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest values relative to the subcarrier amplitude at blanking level. The differential phase is defined as the difference in degrees between the largest and smallest phase angles.
7. Measured with a source impedance of 75 Ω.

$$\text{Signal-to-noise ratio} = 20\log \frac{V_o \text{ black-to-white}}{V_{i(rms)} \text{ at } B = 5 \text{ MHz}}.$$

8. Measured with a sawtooth-modulated input signal: m = 90%; $V_{i(rms)}$ = 10 mV;

$$\text{Amplitude modulation} = \frac{V_o \text{ SC at top sync} - V_o \text{ SC at white}}{V_o \text{ SC at top sync} + V_o \text{ SC at white}} \times 100\%.$$

(SC = sound carrier)

9. Starting point of tuner take-over for an npn tuner is when I_6 = 1,8 mA, and for a pnp tuner is when I_6 = 0,2 mA.
10. Measured at $V_{8\text{-}9(rms)}$ = 10 mV and pin 16 loaded with 2 x 100 kΩ between V_7 and ground. Reference tuned circuit Q-factor = 36.
11. Reference tuned circuit Q-factor = 16; audio frequency = 1 kHz; carrier frequency = 5,5 MHz.
12. The demodulator tuned circuit must be tuned for minimum distortion; output signal is measured at Δf = 7,5 kHz; other measurements are at Δf = 27,5 kHz.
13. Volume control can be realized by a variable resistor (5 kΩ) connected between pin 11 and ground, or by a variable voltage direct to pin 11 (the low value of input impedance to pin 11 must be taken into account).
14. The sync separator is noise-gated; the slicing level is referred to the top sync level and is independent of the video signal. The value stated is a percentage of the sync pulse amplitude, the level being dependent on external resistors connected to pin 26.
15. The phase detector current is increased by a factor of 7 during catching and when the phase detector is switched to 'fast' via pin 28, thus ensuring a wide catching range and a high dynamic loop gain.
16. The negative-going edge initiates switching-off of the line output transistor (simultaneous driver).
17. The circuit requires an integrated flyback pulse. Gate pulses for a.g.c. and coincidence detectors are obtained from the sawtooth waveform.
18. The functions of in-sync, out-of-sync and transmitter identification are combined on pin 28. For the reception of VCR signals, V_{28} must be fixed between 3 V and 4,5 V so that the time constant is fast and sound information is preserved.

APPLICATION INFORMATION

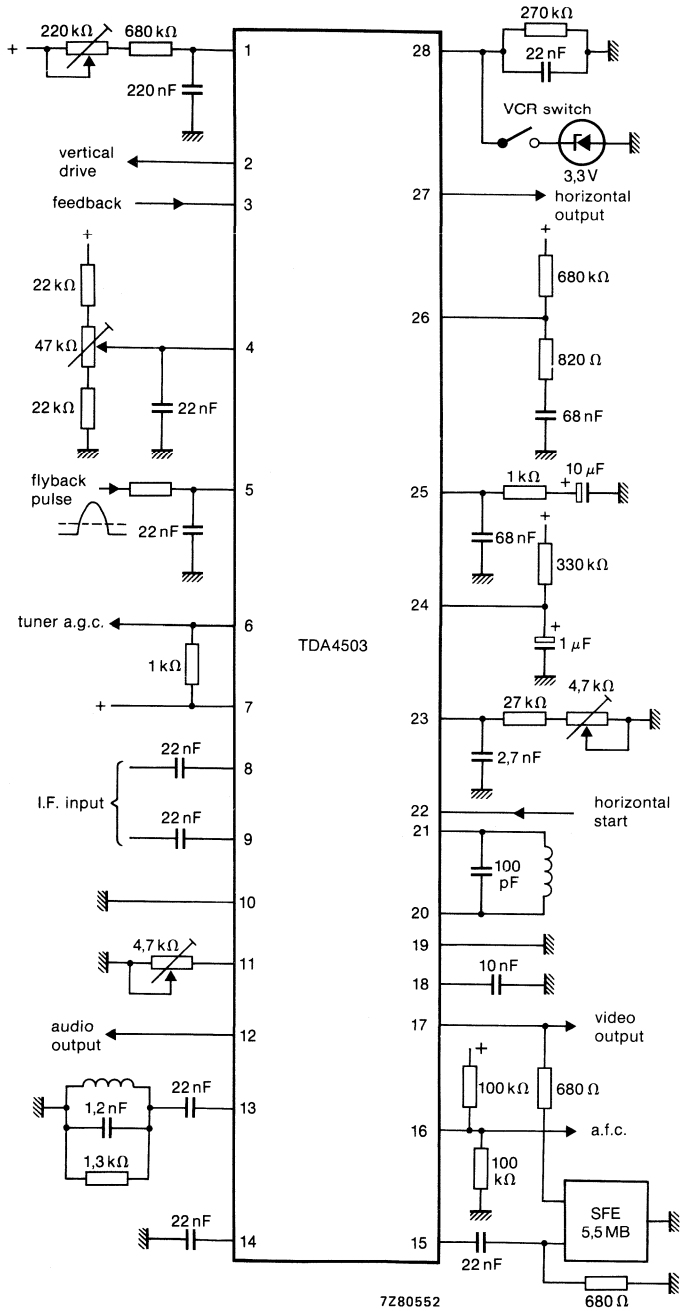


Fig. 2 Application circuit diagram.

APPLICATION INFORMATION (continued)

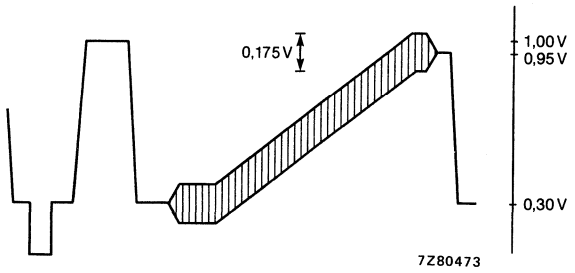


Fig. 3 Video output signal.

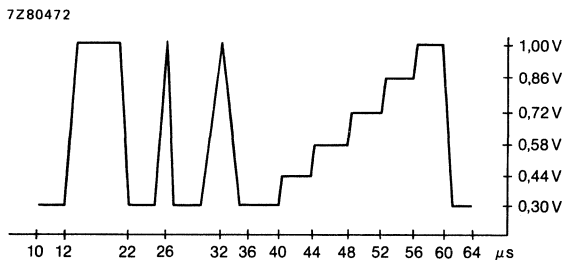


Fig. 4 E.B.U. test signal - line 330.

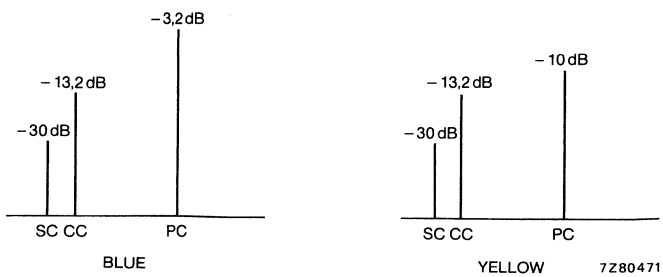


Fig. 5 Input signal conditions for intermodulation test: SC = sound carrier; CC = chrominance carrier; PC = picture carrier; all values are with respect to the top sync level.

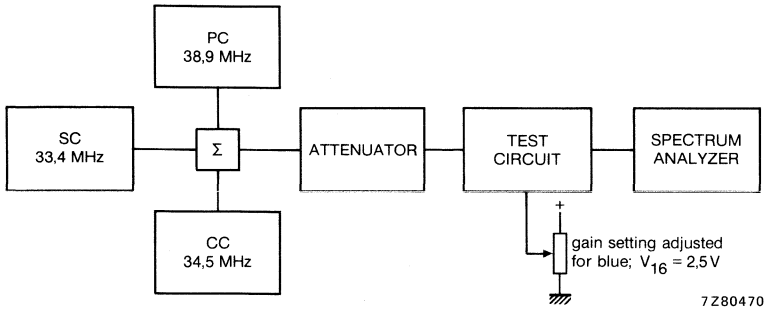


Fig. 6 Circuit for intermodulation test:

value at 1,1 MHz = 20log $\frac{V_o \text{ at } 4,4 \text{ MHz}}{V_o \text{ at } 1,1 \text{ MHz}}$ + 3,6 dB;

value at 3,3 MHz = 20log $\frac{V_o \text{ at } 4,4 \text{ MHz}}{V_o \text{ at } 3,3 \text{ MHz}}$

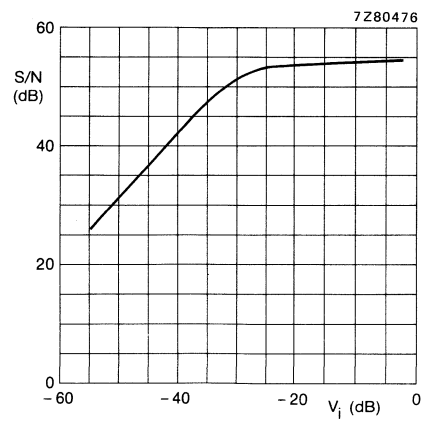


Fig. 7 Signal-to-noise ratio as a function of input voltage.

APPLICATION INFORMATION (continued)

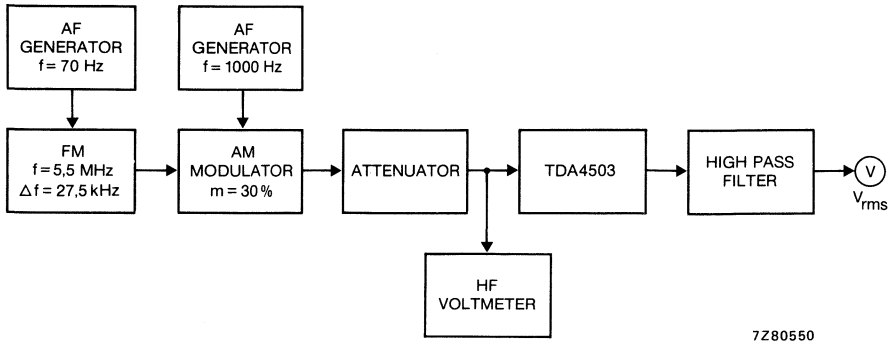


Fig. 8 Circuit for amplitude modulation rejection test.

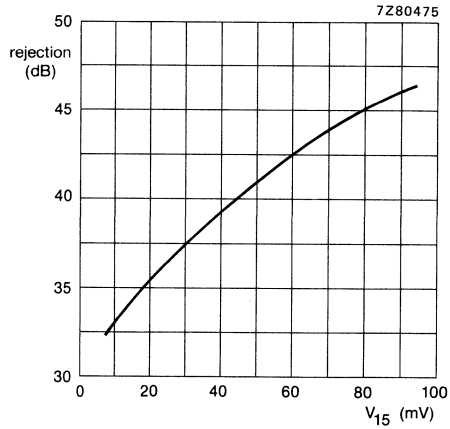


Fig. 9 Typical amplitude modulation rejection curve.

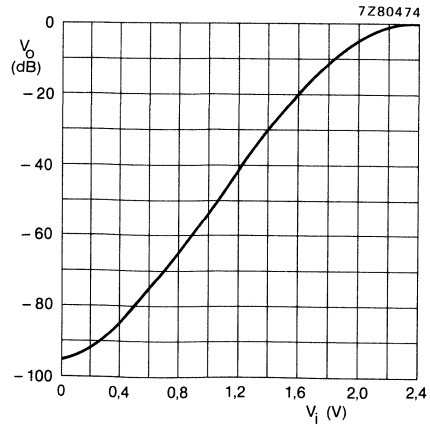


Fig. 10 Volume control characteristic.

SMALL SIGNAL COMBINATION IC FOR COLOUR TV

GENERAL DESCRIPTION

The TDA4505 is a TV sub-system circuit, for colour television receivers. For a complete colour television receiver only a tuner, a colour decoder and output stages are required.

Features

- Vision IF amplifier with synchronous demodulator
- Tuner AGC (negative going control voltage with increasing signal)
- AGC detector suited for negative modulation
- AFC circuit
- Video preamplifier
- Sound IF amplifier, demodulator and preamplifier
- DC volume control **or** separate supply for starting the oscillator
- Horizontal synchronization circuit with two control loops
- Vertical synchronization (divider system) and sawtooth generation with automatic amplitude adjustment for 50 or 60 Hz mode
- Transmitter identification (mute)
- Three level sandcastle pulse generation

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 7)	V_{7-6}	9,5	12	13,2	V
Supply current (pin 7)	I_7	–	135	–	mA
Supply current (pin 11)	I_{11}	–	6	8,5	mA
Operating ambient temperature range	T_{amb}	–25	–	+ 65	°C
Storage temperature range	T_{stg}	–25	–	+ 150	°C
Total power dissipation	P_{tot}	–	–	2,3	W

PACKAGE OUTLINE

28-lead DIL; plastic (with internal heat spreader) (SOT117).

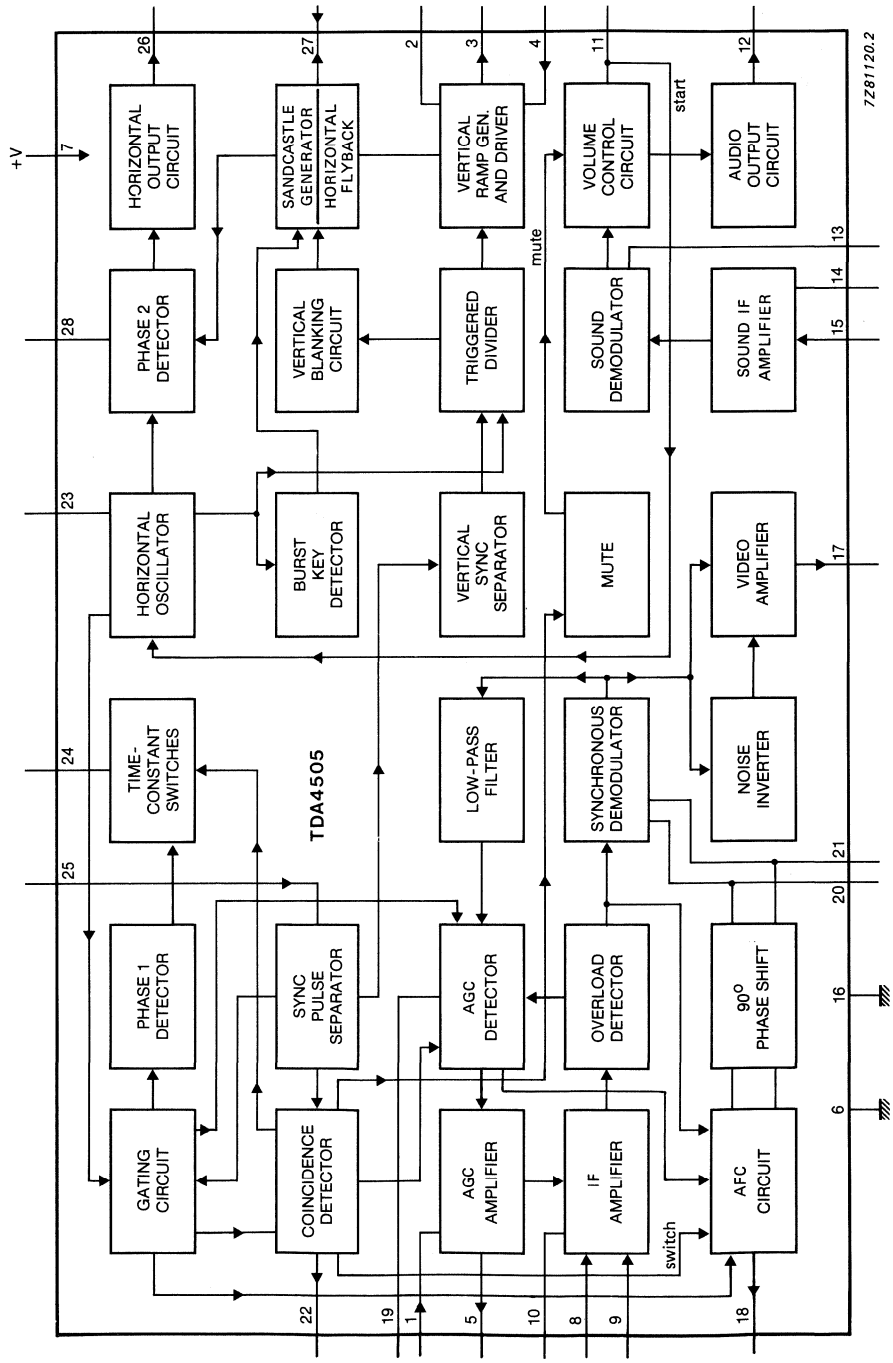


Fig. 1 Block diagram.

PINNING

1. AGC take over
2. Vertical ramp generator
3. Vertical drive
4. Vertical feedback
5. Tuner AGC
6. Ground
7. Supply
8. Vision IF input
9. Vision IF input
10. Decoupling capacitor
11. Volume control/start horizontal oscillator
12. Audio output
13. Sound demodulator
14. Sound IF decoupling
15. Sound IF input
16. Ground
17. Video output
18. AFC output
19. AGC detection
20. Synchronous demodulator
21. Synchronous demodulator
22. Coincidence detector decoupling
23. Horizontal oscillator
24. Phase 1 detector
25. Sync separator
26. Horizontal drive
27. Sandcastle output/flyback input
28. Phase 2 detector

FUNCTIONAL DESCRIPTION

IF amplifier, demodulator and AFC

The IF amplifier has a symmetrical input (pins 8 and 9). The synchronous demodulator and the AFC circuit share an external reference tuned circuit (pins 20 and 21). An internal RC-network provides the necessary phase-shift for AFC operation. The AFC circuit is gated by an internally generated gating pulse. As a result the AFC output voltage contains no video information. The AFC circuit provides a control voltage output with a swing greater than 10 V at pin 18.

AGC circuit

Gating of the AGC detector is performed to reduce sensitivity of the IF amplifier to external electrical noise. The AGC time constant is provided by an RC-circuit connected to pin 19. The point of tuner take-over is preset by the voltage level at pin 1.

Video amplifier

The signal through the video amplifier comprises video and sound information.

Sound circuit and horizontal oscillator starting function

The input to the sound IF amplifier is obtained by a bandpass filter coupling from the video output (pin 17). The sound is demodulated and passed via a dual-function volume control stage to the audio output amplifier. The volume control function is obtained by connecting a variable resistor (4,7 kΩ) between pin 11 and ground, or by supplying pin 11 with a variable voltage. Sound output is suppressed by an internal mute signal when no TV signal is identified.

DC volume control/Horizontal oscillator start

The circuit can be used with a DC volume control or with a starting possibility of the horizontal oscillator. The operation depends on the application. When during switch-on no current is supplied to pin 11 this pin will act as volume control. When a current of 6 mA is supplied to pin 11 the volume control is set to a fixed output signal and the IC will generate drive pulses for the horizontal deflection. The main supply of the IC can then be derived from the horizontal deflection.

FUNCTIONAL DESCRIPTION (continued)

Horizontal synchronization

The video input signal (positive video) is connected to pin 25.
The horizontal synchronization has two control loops. This has been introduced to generate a sand-castle pulse. Using the oscillator sawtooth facilitates accurate timing of the burst key pulse. Therefore, the phase of this sawtooth must have a fixed relationship to the sync pulse, which is achieved by use of a second loop.

Horizontal phase detector

The circuit has the following operating conditions.

(a) Strong input signal, synchronized or not synchronized.
(The input signal condition is obtained from the AGC-circuit, the in-sync./out-of-sync from the coincidence detector). In this condition the time constant is optimal for VCR-playback i.e.; fast time constant during the vertical retrace (to be able to correct head-errors of the VCR) and such a time constant during scan that fluctuations of the sync. are corrected. The phase detector is not gated.

(b) Weak signal.
In this condition the time constant is doubled compared to condition (a). Also the phase detector is gated when the oscillator is synchronized. This ensures a stable display which is not disturbed by the noise in the video signal.

(c) Not synchronized (weak signal).
In this condition the time constant during scan and vertical retrace are the same as during scan in condition (a).

Vertical sync pulse

The vertical sync pulse integrator will not be disturbed when the vertical sync pulses have a width of only 10 μs with a separation of 22 μs. This type of vertical sync pulses are generated by video tapes with anti-copy guard.

Vertical divider system

The TDA4505 embodies a synchronized divider system for generating the vertical sawtooth at pin 2.
The divider system has an internal frequency doubling circuit, which allows the horizontal oscillator to operate at its normal line frequency. One line period equals 2 clock pulses.
Use of the divider system avoids the requirement for vertical frequency adjustment. The divider has a discriminator window for automatic switching from 60 Hz to 50 Hz mode. When the trigger pulse comes before line 576 the 60 Hz mode is selected, otherwise the 50 Hz mode is selected.
The divider system operates with 2 different divider reset windows for maximum interference/disturbance protection.
The windows are activated via an up/down counter.
The counter increases its counter value by 1 each time the separated vertical sync pulse is within the search window. When not within the search window this value is decreased by 1.
The operating modes of the divider system are as follows.

Mode A

Large (search) window (divider ratio between 488 and 722)

This mode is valid for the following conditions:

- Divider is looking for a new transmitter
- Divider ratio found – not within the narrow window limits
- Non-standard TV-signal condition detected while a double or enlarged vertical sync pulse is found after the internally generated anti-topflutter pulse has ended. This means a vertical sync pulse width > 8 clock pulses (50 Hz); > 10 clock pulses (60 Hz)
  Usually this mode is activated for video tape recorders operating in the feature trick mode
- Up/down counter value of the divider system operating in the narrow window mode drops below count 10

Mode B

Narrow window (divider ratio between 522 to 528; 60 Hz or 622 to 628; 50 Hz)

The divider system switches over to this mode when the up/down counter has reached its maximum value of 15 approved vertical sync pulses. When the divider operates in this mode and a vertical sync pulse is missing within the window, the divider is reset at the end of the window and the counter value is decreased by 1. At a counter value below 10 the divider system switches over the large window mode. The divider system also generates an anti-topflutter pulse which inhibits the Phase 1 detector during the vertical sync pulse. The pulse width is dependent on the divider mode. In Mode A the start is generated by reset of the divider. In Mode B the anti-topflutter pulse starts at the beginning of the first equalizing pulse.
The anti-topflutter pulse ends at count 10 for the 50 Hz mode and count 12 for the 60 Hz mode.
The vertical blanking pulse is also generated via the divider system. The start is by reset of the divider while the blanking pulse width is 34 (17 lines) for the 60 Hz mode and at count 42 (21 lines) for the 50 Hz mode. The vertical blanking pulse at the sandcastle output (pin 27) is generated by adding the anti-topflutter pulse to the blanking pulse. Thus the vertical blanking pulse starts at the beginning of the first equalizing pulse when the divider operates in Mode B. The length of the vertical blanking in this condition is 21 lines in the 60 Hz mode and 25 lines in the 50 Hz mode.

DEVELOPMENT DATA

Application when external video signals require synchronization

The input to the sync separator is externally available via pin 25. For normal application the video output signal at pin 17 is AC coupled to this input as shown in Fig. 10. It is possible to interrupt this connection and drive the sync separator from other sources such as:

- a teletext decoder in serial mode
- an external audio signal via a peritelevision connector

When a teletext decoder is applied the IF amplifier and synchronization circuit are operating in the same phase which allows various connections between the two parts (i.e. AGC gating) can remain active. When external signals are applied to the sync separator the connections between the two parts must be interrupted. This can be achieved by connecting pin 22 to ground, which results in the following conditions:

- AGC detector is not gated
- AFC circuit is active
- Mute circuit not active – sound channel remains switched on
- Phase detector 1 has an optimal time constant for external video sources

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 7)	$V_P = V_{7-6}$	–	13,2	V
Total power dissipation	P_{tot}	–	2,3	W
Operating ambient temperature range	T_{amb}	−25	+ 65	°C
Storage temperature range	T_{stg}	−25	+ 150	°C

CHARACTERISTICS

$V_P = V_{7-6} = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage (pin 7)		V_{7-6}	9,5	12	13,2	V
Supply current (pin 7)		I_7	–	135	–	mA
Supply current (pin 11) for horizontal oscillator start	note 1	I_{11}	–	6	8,5	mA
Vision IF amplifier (pins 8 and 9)						
Input sensitivity at 38,9 MHz	on-set AGC	V_{8-9}	60	130	180	μA
Input sensitivity at 45,75 MHz	on-set AGC	V_{8-9}	–	140	–	μA
Differential input resistance (pin 8 to 9)		R_{8-9}	800	1300	1800	Ω
Differential input capacitance (pin 8 to 9)		C_{8-9}	–	5	–	pF
Gain control range		G_{8-9}	–	63	–	dB
Maximum input signal		V_{8-9}	50	180	–	mV
Expansion of output signal for 40 dB variation of input signal with V_{8-9} at 300 μV, 0 dB)		ΔV_{17-6}	–	1	–	dB
Video amplifier						
Measured at top sync input signal voltage (rms value) of 10 mV						
Output level for zero signal input (zero point of switched demodulator)		V_{17-6}	5,4	5,8	6,2	V
Output signal top sync level	note 2	V_{17-6}	2,7	2,9	3,1	V
Amplitude of video output signal (peak-to-peak value)		$V_{17-6(p-p)}$	2,3	2,6	2,9	V

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Internal bias current of output transistor (npn emitter follower)		$I_{17(int)}$	1,4	2,0	–	mA
Bandwidth of demodulated output signal		B	4	4,5	–	MHz
Differential gain	note 3	G_{17}	–	4	10	%
Differential phase	note 3	φ	–	3	10	deg
Video non-linearity	note 4	NL	–	4	10	%
Intermodulation with input signal of 10 mV(rms)	see Fig. 2 and Fig. 5					
f = 1,1 MHz (blue)			50	55	–	dB
f = 1,1 MHz (yellow)			48	52	–	dB
f = 3,3 MHz (blue)			50	55	–	dB
f = 3,3 MHz (yellow)			50	55	–	dB
Signal-to-noise ratio	Z_S = 75 Ω; note 5					
V_i = 10 mV		S/N	45	50	–	dB
end of gain control range		S/N	50	55	–	dB
as a function of the input signal		S/N	see Fig. 6			
Residual carrier signal			–	7	30	mV
Residual 2nd harmonic of carrier signal			–	24	40	mV
Tuner AGC	note 6					
Minimum starting point take-over (rms value)		$V_{1-6(rms)}$	–	–	0,5	mV
Maximum starting point take-over (rms value)		$V_{1-6(rms)}$	50	180	–	mV
Maximum output swing		$I_{5(max)}$	6	10	–	mA
Output saturation voltage	I_5 = 2 mA	$V_{5-6(sat)}$	–	100	300	mV
Leakage current		I_5	–	0,7	1	μA
Input signal variation complete tuner control		ΔV_i	0,2	2,0	5,0	dB
AFC circuit (pin 18)	note 7					
AFC output voltage swing (peak-to-peak value)		$V_{18-6(p-p)}$	9,2	10	11,5	V
Available output current		$\pm I_{18}$	–	2,8	–	mA
Control steepness			35	50	70	mV/kHz
Output voltage at nominal tuning of the reference tuned circuit		V_{18-6}	–	6	–	V
Offset current AFC output (pins 20 and 21 short-circuited)		I_{18}	–	0	± 100	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Sound circuit						
Input limiting voltage	$V_o = V_{o(max)} = 3$ dB; $Q_L = 16$; $f_{AF} = 1$ kHz; $f_c = 5{,}5$ MHz	$V_{15\text{-}6}$	–	400	800	μA
Input resistance	$V_{i(rms)} = 1$ mV	R_{15}	–	2,6	–	kΩ
Input capacitance	$V_{i(rms)} = 1$ mV	C_{15}	–	6	–	pF
AM suppression (Figs 7 and 8)	$V_i = 10$ mV	AMS	–	46	–	dB
	$V_i = 50$ mV	AMS	–	50	–	dB
AF output signal (rms value)	Δf = 7,5 kHz; minimum distortion; maximum volume control	$V_{12\text{-}6(rms)}$	400	600	800	mV
AF output signal pin 11 as starting pin (rms value)	Δf = 50 kHz; $V_{11\text{-}6} > 10{,}5$ V	$V_{12\text{-}6(rms)}$	300	700	1400	mV
AF output impedance		Z_{12}	–	25	100	Ω
Total harmonic distortion	volume control 20 dB; Δf = 7,5 kHz	THD	–	1	3	%
Ripple rejection	volume control 20 dB; $f_k = 100$ Hz	RR	–	27	–	dB
	when muted	RR	–	30	–	dB
Output voltage in mute condition		$V_{12\text{-}6}$	–	3,0	–	V
Signal-to-noise ratio	Δf = 27,5 kHz; weighted noise in accordance with CCIR 468	S/N	–	56	–	dB
Volume control	see Fig. 9					
Output voltage	pin 11 open-circuit	$V_{11\text{-}6}$	–	5,5	7,0	V
Output current	pin 11 short-circuit	I_{11}	–	0,9	1,5	mA
External control resistor		R_{11}	–	4,7	–	kΩ
Suppression output signal during mute condition		OSS	60	66	–	dB

parameter	conditions	symbol	min.	typ.	max.	unit
Sync separator and first control loop						
Required sync pulse amplitude (peak-to-peak value)	R_{17-25} = 1,8 kΩ; note 8	$V_{25-6(p-p)}$	200	800	–	mV
Input current	$V_{25-6} > 5$ V	I_{25}	–	8,5	–	μA
	V_{25-6} = 0 V	I_{25}	–	10	–	mA
Holding range PLL		± Δf	–	1100	1500	Hz
Catching range PLL		± Δf	600	1000	–	Hz
Second control loop (positive edge)						
Control sensitivity		Δ_{td}/Δ_{to}	–	50	–	
Control range		t_d	–	25	–	μs
Phase adjustment (via second control loop)						
Control sensitivity			–	25	–	μA/μs
Maximum allowed phase shift		α	–	± 2	–	μs
Horizontal oscillator (pin 23)	note 9					
Free running frequency	R = *; C = 2,7 nF	f_{fr}	–	15625	–	Hz
Spread with fixed external components		Δf	–	0,4	4	%
Frequency variation due to change of supply voltage from 9,5 to 13,2 V		Δf_{fr}	–	0,2	0,5	%
Frequency variation with temperature		TC	–	–	1,6	Hz/K
Maximum frequency shift		Δf_{fr}	–	4	10	%
Maximum frequency deviation at start horizontal output		Δf_{fr}	–	8	10	%
Horizontal output (pin 26)						
Output voltage high level		V_{26-6}	–	–	13,2	V
Output voltage at which protection commences		V_{26-6}	–	13,2	15,8	V
Output voltage LOW	I_{26} = 10 mA	V_{26-6}	–	0,15	0,5	V
Duty cycle of horizontal output signal	t_p = 10 μs	d	–	0,45	–	
Rise time of output pulse		t_r	–	300	370	ns
Fall time of output pulse		t_f	–	120	240	ns

* Value to be fixed.

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Horizontal flyback input and sandcastle output	note 10					
Input current required during flyback pulse		I_{27}	0,1	–	2,0	mA
Output voltage						
during burst key pulse		V_{27-6}	8,4	9,0	–	V
during horizontal blanking		V_{27-6}	4,1	4,4	5,0	V
during vertical blanking		V_{27-6}	2,1	2,4	2,7	V
Pulse width						
burst key pulse	60 Hz	t_W	3,1	3,5	3,9	μs
burst key pulse	50 Hz	t_W	3,5	3,8	4,4	μs
horizontal blanking pulse			flyback pulse width			
vertical blanking pulse						
50 Hz divider in search window			–	21	–	lines
60 Hz divider in search window			–	17	–	lines
50 Hz divider in narrow window			–	25	–	lines
60 Hz divider in narrow window			–	21	–	lines
Delay between start of sync pulse at video output and falling edge of burst key pulse for NTSC signals			–	–	9,2	μs
Coincidence detector mute output	note 11					
Voltage for in-sync condition		V_{22-6}	9,5	10,3	11	V
Voltage for no-sync condition	no signal	V_{22-6}	1,2	1,45	2,2	V
Switching level to switch off AFC		V_{22-6}	–	6,4	–	V
Hysteresis AFC switch		V_{22-6}	–	0,4	–	V
Switching level to activate mute function (transmitter identification)		V_{22-6}	2,25	2,4	2,75	V
Hysteresis MUTE function		V_{22-6}	–	0,5	–	V
Charge current (peak-to-peak value)	in-sync 4,7 μs	$I_{22(p-p)}$	0,7	1,0	–	mA
Discharge current (peak-to-peak value)	in-sync 1,0 μs	$I_{22(p-p)}$	–	0,5	–	mA
Required voltage to allow synchronization of circuit with signals which have no relation to the video output signal		V_{22-6}	–	1,0	1,2	mA

parameter	conditions	symbol	min.	typ.	max.	unit
Vertical ramp generator	note 12					
Input current during scan		I_2	–	0,5	2,0	μA
Discharge current during retrace		I_2	0,3	0,35	0,4	mA
Sawtooth amplitude (peak-to-peak value)		$I_{2\text{-}6(p\text{-}p)}$	–	0,8	1,1	V
Vertical drive output (pin 3)						
Maximum available output current		I_3	1,5	3,0	–	mA
Maximum output voltage	I_3 = 1,5 mA	$V_{3\text{-}6}$	–	4,0	–	V
Vertical feedback input (pin 4)						
Input voltage DC component		$V_{4\text{-}6}$	2,9	3,3	3,7	V
AC component (peak-to-peak value)		$V_{4\text{-}6(p\text{-}p)}$	–	1,3	–	V
Input current		I_4	–	–	12	μA
Internal precorrection to sawtooth		Δt_p	–	6	–	%
Deviation amplitude	50/60 Hz		–	–	2	%
Vertical guard	note 13					
Active at a deviation with respect to the DC feedback level	$V_{27\text{-}6}$ = 2,5 V					
switching level LOW		$\Delta_{4\text{-}6}$	–	−1,3	–	V
switching level HIGH		$\Delta_{4\text{-}6}$	–	+1,9	–	V

DEVELOPMENT DATA

Notes to the characteristics

1. Pin 11 has a double function. When during switch-on a current of 6 mA is supplied to this pin, which is used to start the horizontal oscillator. The main supply can then be obtained from the horizontal deflection stage. When no current is supplied to this pin it can be used as volume control. The indicated maximum value is the current at which all ICs will start. Higher currents are allowed, the excess current is bypassed to ground.
2. Signal with negative going sync, top white 10% of the top sync amplitude.
3. Measured according the test line shown in Fig. 3:
   - The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier at blanking level.
   - The differential phase is defined as the difference in degrees between the largest and smallest phase angle.
4. This figure is valid for the complete video signal amplitude (peak white-to-black); see Fig. 4.
5. Signal-to-noise ratio = $20 \log \frac{V_{\text{out black-to-white}}}{V_{n(\text{rms}) \text{ at } B = 5\,\text{MHz}}}$.
6. Tuner AGC; starting point tuner take-over at I = 0,2 mA. Take-over to be adjusted with a potentiometer of 47 kΩ. The voltage at pin 1 must not be reduced below 1 V.

Notes to the characteristics (continued)

7. The AFC control voltage is obtained by multiplying the IF output signal (which is also used to drive the synchronous demodulator) with a reference carrier. This reference carrier is obtained from the demodulator tuned circuit via a 90° phase shift network. The IF output signal has an asymmetrical frequency spectrum with respect to the carrier frequency. To avoid problems due to this asymmetrical signal the AFC circuit is gated by an internally generated gating pulse. As a result the detector is operative only during sync/black level at a constant carrier amplitude which contains no additional side bands. Thus the AFC output voltage contains no video information.

   At very weak input signals the drive signal for the AFC circuit will have a high noise content. The noise input has an asymmetrical frequency spectrum which will cause an offset of the AFC output voltage. To avoid problems due to this effect the AFC is switched off when the AGC is controlled to maximum gain.

   Values are measured with an input signal of 10 mV (rms) and the AFC output loaded with 2 x 470 kΩ between supply voltage and ground. The unloaded Q-factor of the reference tuned circuit is 70. The AFC is switched off when no signal is detected by the coincidence detector or when the voltage at pin 22 is between 1,2 V and 6,4 V. This can be realized by a resistor of 68 kΩ connected between pin 22 and ground.
8. The slicing level can be varied by changing the value of the resistance between pin 17 and pin 25. A higher resistance results in a larger value of the minimum sync pulse amplitude. The slicing level is independent of the video information.
9. Frequency control is obtained by supplying a correction current to the oscillator RC-network via a resistor, connected between the Phase 1 detector output and the oscillator network. The oscillator can be adjusted to the correct frequency by one of the two following methods:
   (a) Interrupt R_{23-24}.
   (b) Short-circuit the sync separator bias network (pin 25 to power supply).
   To avoid the necessity of a VCR switch, the time-constant of phase detector at strong input signal is sufficiently short to obtain a stable picture during VCR playback. During the vertical retrace period the time-constant is even shorter so that the head errors of the VCR are compensated at the beginning of the scan. During weak signal conditions (information derived from the AGC circuit) the time constant is increased to obtain a good noise immunity.
10. The horizontal flyback input and the sandcastle output have been combined on pin 27. The flyback pulse is clamped to a level of 4,9 V. The minimum current to drive the second control loop is 0,1 mA.
11. The functions in-sync/out-of-sync and transmitter identification have been combined on pin 22. The capacitor is charged during the sync pulse and discharged during the time difference between gating and sync pulse.
12. The vertical scan is synchronized by means of a divider system. Therefore no adjustment is required for the ramp generator. The divider detects whether the incoming signal has a vertical frequency of 50 or 60 Hz and corrects the vertical amplitude.
13. To avoid screenburn due to a collapse of the vertical deflection a continuous blanking level is inserted into the sandcastle pulse when the feedback voltage of the vertical deflection is not within the specified limits.

Where

SC = sound carrier
CC = chrominance carrier
PC = picture carrier

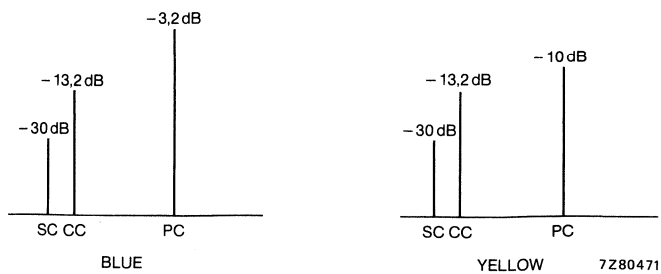


Fig. 2 Input signal conditions for intermodulation test; all values are with respect to the top sync level.

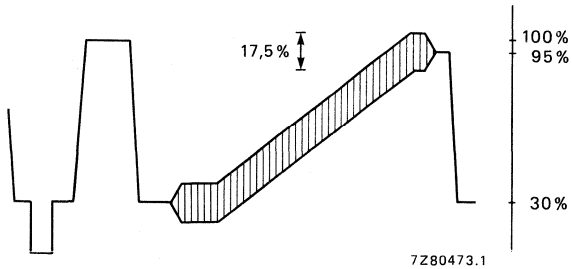


Fig. 3 Video output signal.

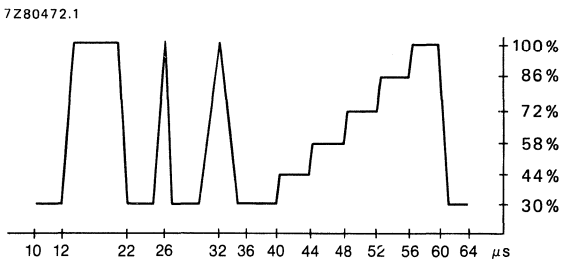
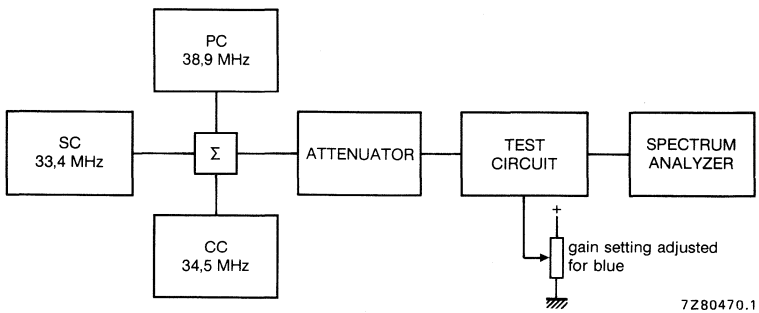


Fig. 4 European Broadcasting Union (EBU) test signal waveform (line 330).

DEVELOPMENT DATA



Where:

Value at 1,1 MHz: $20 \log \frac{V_o \text{ at } 4,4 \text{ MHz}}{V_o \text{ at } 1,1 \text{ MHz}} + 3,6 \text{ dB}$

Value at 3,3 MHz: $20 \log \frac{V_o \text{ at } 4,4 \text{ MHz}}{V_o \text{ at } 3,3 \text{ MHz}}$

Fig. 5 Test set-up intermodulation.

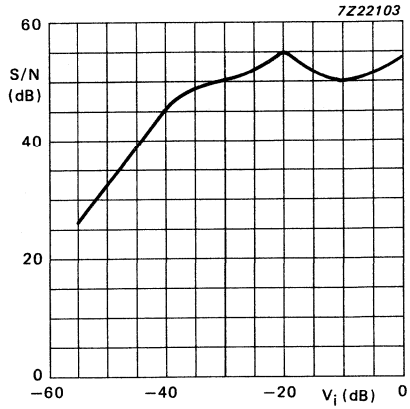


Fig. 6 Signal-to-noise ratio as a function of input voltage; 0 dB = 100 mV.

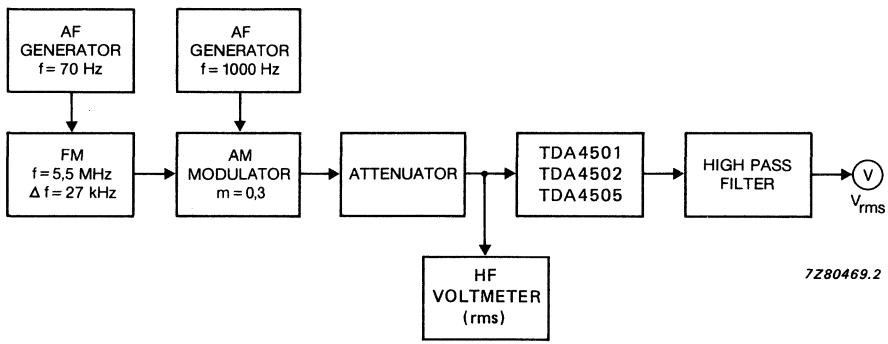


Fig. 7 Test set-up AM suppression.

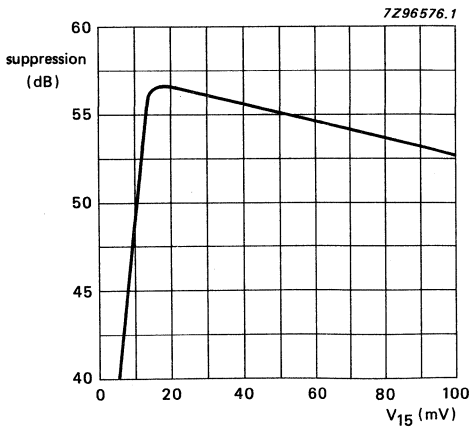


Fig. 8 AM suppression.

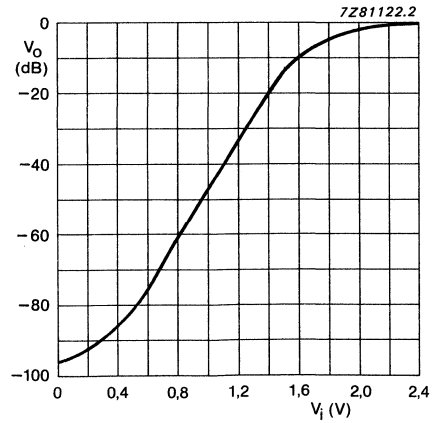


Fig. 9 Volume control characteristics.

DEVELOPMENT DATA

APPLICATION INFORMATION

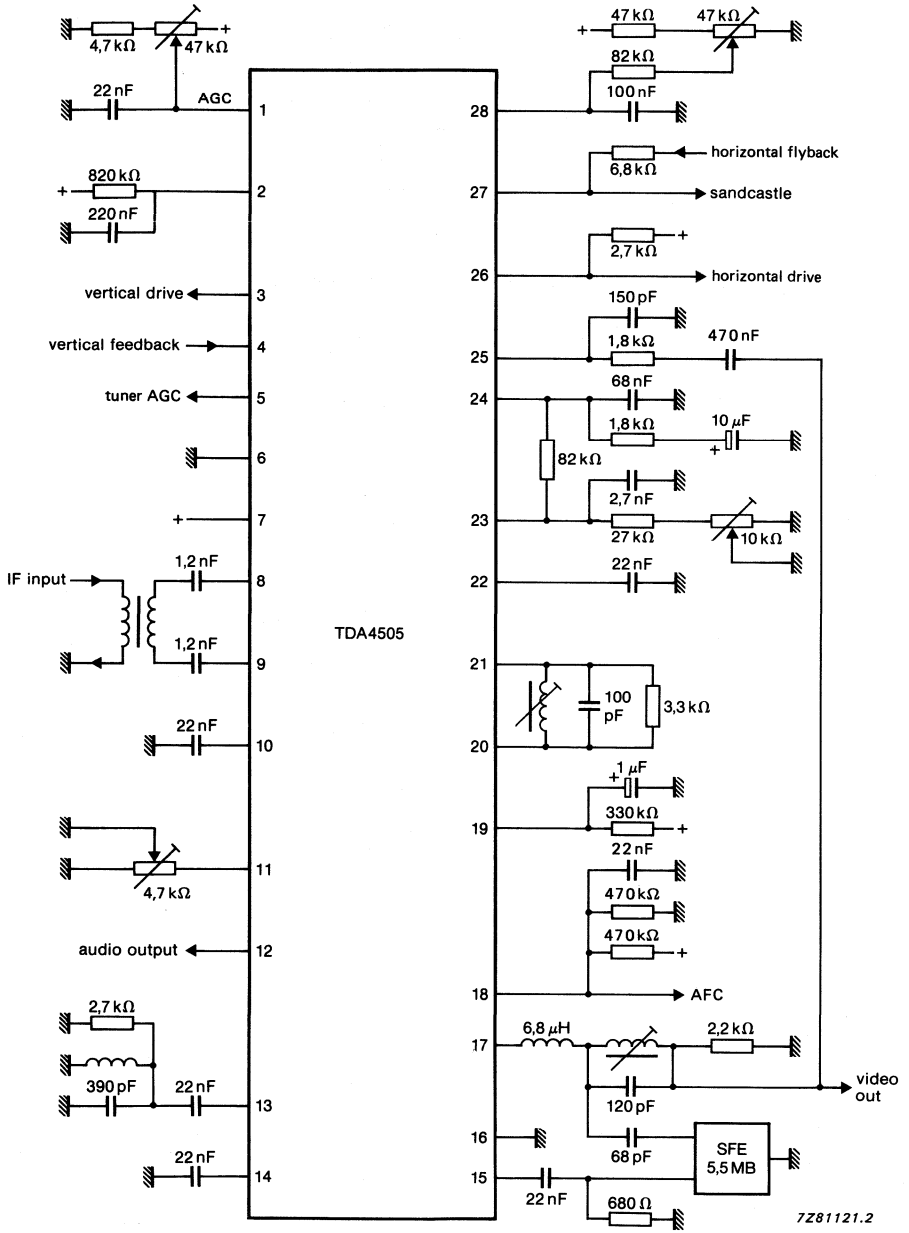


Fig. 10 Application diagram.

PAL DECODER

The TDA4510 is a colour decoder for the PAL standard, which is pin sequent compatible with multi-standard decoder TDA4555 and also pin compatible with NTSC decoder TDA4570. It incorporates the following functions:

Chrominance part

- Gain controlled chrominance amplifier with operating point control stage
- Chrominance output stage for driving the 64 μs delay line
- Blanking circuit for the colour burst signal
- Automatic chrominance control (ACC) with sampled rectifier during burst-key

Oscillator and control voltage part

- Reference oscillator for double subcarrier frequency
- Gated phase comparison
- Identification demodulator and automatic colour killer
- Sandcastle pulse detector
- Service switch

Demodulator part

- Two synchronous demodulators for the (B-Y) and (R-Y) signals
- PAL flip-flop and PAL switch
- Colour switching stages
- Separate colour switching output
- (B-Y) and (R-Y) signal output stages
- Internal filtering of residual carrier

QUICK REFERENCE DATA

Supply voltage	$V_P = V_{7-3}$	typ.	12 V
Supply current	$I_P = I_7$	typ.	50 mA
Chrominance input signal (peak-to-peak)	$V_{9-3(p-p)}$		10 to 400 mV
Chrominance output signal (peak-to-peak)	$V_{6-3(p-p)}$	typ.	1,6 V
Colour difference output signals (peak-to-peak values)			
—(R-Y) signal	$V_{1-3(p-p)}$	typ.	1,05 V ± 2 dB
—(B-Y) signal	$V_{2-3(p-p)}$	typ.	1,33 V ± 2 dB
Sandcastle pulse, required amplitude for			
burst gating level	V_{15-3}	typ.	7,7 V
horizontal pulse separation	V_{15-3}	typ.	4,5 V
vertical and horizontal pulse separation	V_{15-3}	typ.	2,5 V

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

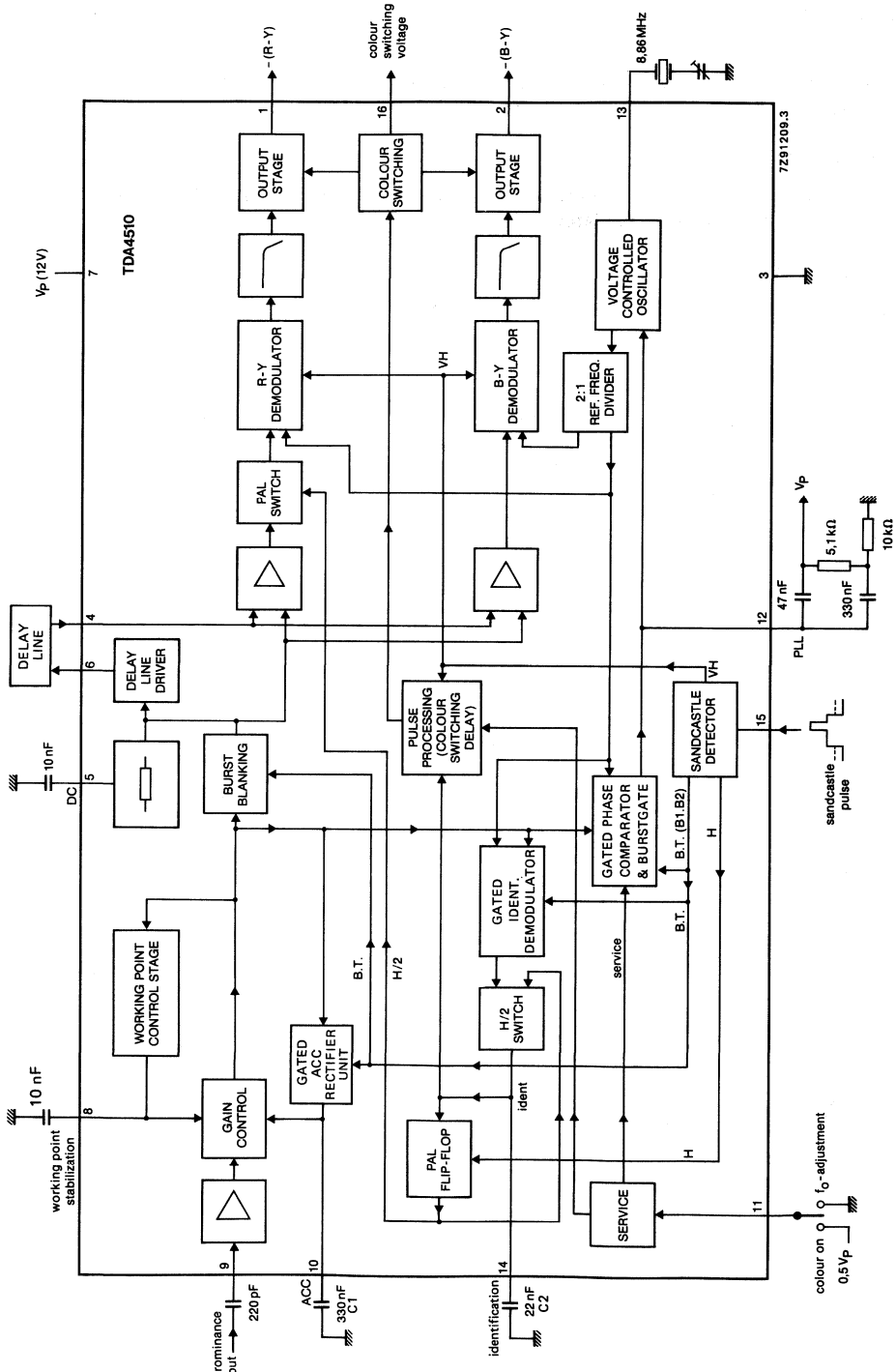


Fig. 1 Block diagram.

External capacitors in Fig. 1

C1 filter capacitor for control voltage (pin 10)

C2 filter capacitor for identification signal (pin 14)

FUNCTIONAL DESCRIPTION

DIVIDER STAGES

The divider stages provide −(R-Y) and −(B-Y) reference signals with the correct 90 degrees relation for the demodulators.

PHASE COMPARATOR

The phase comparator compares the −(R-Y) reference signal with the burst pulse and controls the frequency and phase of the reference oscillator.

IDENTIFICATION DEMODULATOR

The identification demodulator delivers a positive going identification signal for PAL-signals at pin 14, also used for the automatic colour-killer.

SERVICE SWITCH

The service switch has two functions. The first position ($V_{14-3} < 1$ V) allows the adjustment of the reference oscillator. Therefore the colour is switched on and the burst for the oscillator PLL is switched off. The second position ($V_{14-3} > 5$ V) switches the colour on and the output signals can be observed.

DEVELOPMENT DATA

SANDCASTLE PULSE DETECTOR

Sandcastle pulse detector for burst-gate, line and blanking (horizontal and vertical) pulse detection. The vertical part of the sandcastle pulse is needed for the internal colour-on and colour-off delay.

PULSE PROCESSING PART

Pulse processing part which shall prevent a premature switching on of the colour. The colour-on delay, two or three field periods after identification of the PAL signal, is achieved by a counter. The colour is switched off immediately or at the latest one field period after disappearance of the identification voltage.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	$V_P = V_{7-3}$	10,8 to 13,2		V
Currents				
at pins 1 and 2	$-I_{1,2}$	max.	5	mA
at pin 6	$-I_6$	max.	15	mA
at pin 16	$-I_{16}$	max.	5	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature	T_{stg}	−25 to + 150		°C
Operating ambient temperature	T_{amb}	0 to + 70		°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; measured in Fig. 2 unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply current	I_7	–	50	–	mA
Chrominance part					
Input voltage range (peak-to-peak value)	$V_{9\text{-}3(p\text{-}p)}$	10	–	400	mV
Nominal input voltage (peak-to-peak value)					
with 75% colour bar signal	$V_{9\text{-}3(p\text{-}p)}$	–	100	–	mV
Input impedance	$Z_{9\text{-}3}$	–	3,3	–	kΩ
Input capacitance	$C_{9\text{-}3}$	–	4	–	pF
Colour ON					
Chrominance output voltage (peak-to-peak)					
with 75% colour bar signal	$V_{6\text{-}3(p\text{-}p)}$	–	1,6	–	V
d.c. voltage at chrominance output	$V_{6\text{-}3}$	–	8,2	–	V
Oscillator and control voltage part					
Oscillator frequency	f_o	–	8,8	–	MHz
Input resistance	$R_{13\text{-}3}$	–	350	–	Ω
Catching range					
(depending on RC-network at pin 12)	f	± 400	–	–	Hz
Control voltage					
without burst signal	$V_{14\text{-}3}$	–	6,0	–	V
colour on switching threshold	$V_{14\text{-}3}$	–	6,6	–	V
hysteresis of colour switching	$V_{14\text{-}3}$	–	150	–	mV
flip-flop correction (FFC) voltage	$V_{14\text{-}3}$	–	5,5	–	V
hysteresis of FFC	$V_{14\text{-}3}$	–	170	–	mV
Colour-on delay		2	–	3	f.p.*
Colour-off delay		0	–	1	f.p.*
First service position (PLL is inactive					
for oscillator adjustment, colour on)	$V_{11\text{-}3}$	0	–	1	V
second service position (colour on)	$V_{11\text{-}3}$	5	–	–	V
Colour switching output (open npn emitter)					
output current	$-I_{16}$	–	–	5	mA
colour-on voltage	$V_{16\text{-}3}$	–	6	–	V
colour-off voltage	$V_{16\text{-}3}$	–	0	–	V
Demodulator part					
Delayed chrominance input signal (peak-to-peak value)					
with 75% colour bar signal	$V_{4\text{-}3(p\text{-}p)}$	–	200	–	mV
Colour difference output signals (peak-to-peak value)					
–(R-Y) signal	$V_{1\text{-}3(p\text{-}p)}$	0,84	1,05	1,32	V
–(B-Y) signal	$V_{2\text{-}3(p\text{-}p)}$	1,06	1,33	1,67	V

parameter	symbol	min.	typ.	max.	unit
Ratio of colour difference output signals (R-Y)/(B-Y)	$V_{1\text{-}3}/V_{2\text{-}3}$	0,71	0,79	0,87	V
D.C. voltage at colour difference outputs	$V_{1;\,2\text{-}3}$	–	7,7	–	V
Residual carrier voltage at colour difference outputs					
1 x subcarrier frequency (4,4 MHz)	$V_{1,2\text{-}3(p\text{-}p)}$	–	–	20	mV
2 x subcarrier frequency (8,8 MHz)	$V_{1,2\text{-}3(p\text{-}p)}$	–	–	20	mV
Sandcastle pulse detector					
Thresholds:					
Field- and line-pulse separation pulse ON	$V_{15\text{-}3}$	1,3	1,6	1,9	V
Required pulse amplitude	$V_{15\text{-}3}$	2,0	2,5	3,0	V
Line pulse separation; pulse ON	$V_{15\text{-}3}$	3,3	3,6	3,9	V
Required pulse amplitude	$V_{15\text{-}3}$	4,1	4,5	4,9	V
Burst pulse separation; pulse ON	$V_{15\text{-}3}$	6,6	7,1	7,6	V
Required pulse amplitude	$V_{15\text{-}3}$	7,7	–	–	V
Input voltage during horizontal scanning	$V_{15\text{-}3}$	–	–	1,1	V
Input current	$-I_{15}$	–	–	100	μA

DEVELOPMENT DATA

* f.p. is shortening for field periods in this case.

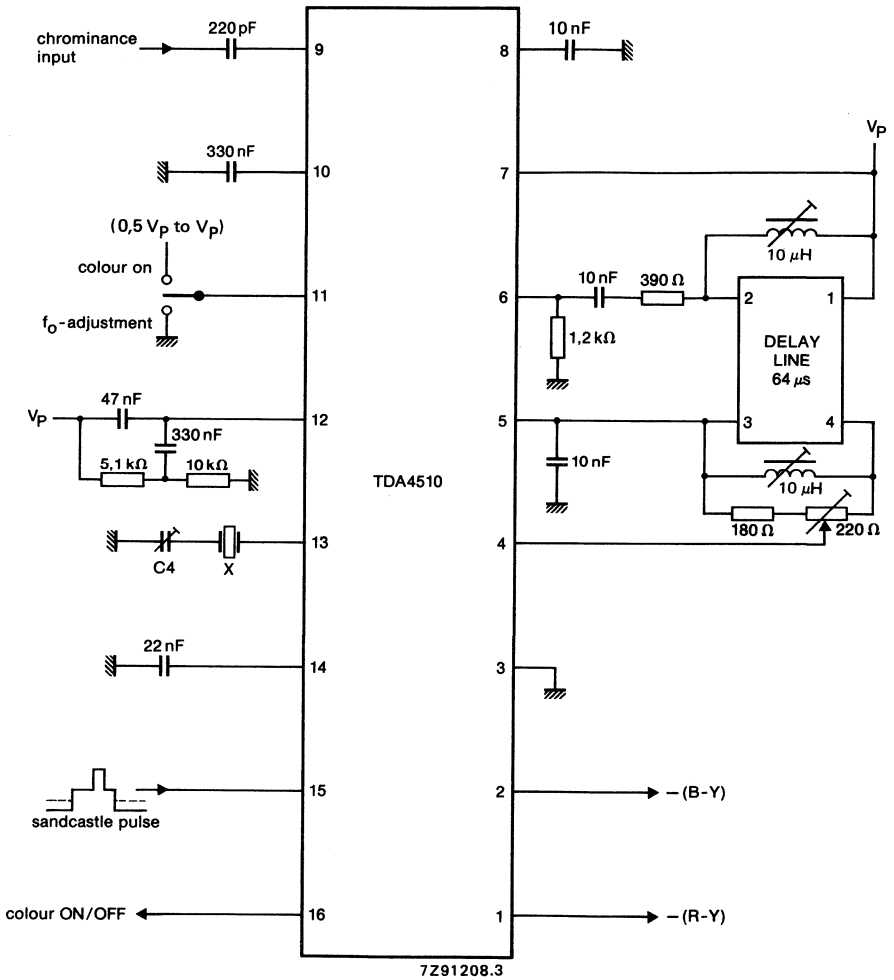


Fig. 2 Application information and test circuit.

C4 = 5 to 27 pF, X = 8,8 MHz; nominal frequency 8,867 238 MHz; resonance resistance 60 Ω, load capacitance 20 pF, dynamic capacitance 22 fF and static capacitance 5,5 pF.

SECAM DECODER

GENERAL DESCRIPTION

The TDA4532 is a monolithic integrated colour decoder for SECAM television receivers. It is pin compatible with the multi-standard decoder TDA4555.

Features

Chrominance part

- Gain controlled amplifier with operating point control stage
- ACC (automatic chrominance control) with rectifier which is disabled during horizontal and vertical flyback
- Chrominance output stage for driving the 64 μs glass delay line
- Limiter stages for direct and delayed chrominance signal
- SECAM permutator

Identification part

- Identification demodulator which is active during the horizontal identification signal and/or during part of the vertical flyback
- Identification mode switch (horizontal, vertical or combined horizontal and vertical)
- Service switch for forced colour on
- Sandcastle pulse for detection of burst gating pulse, horizontal blanking pulse, combined horizontal and vertical blanking pulse. The vertical part of the sandcastle pulse is required for the internal colour ON and colour OFF delay
- Pulse processor part which prevents premature switch-on of the colour. A counter provides colour ON delay of 2 or 3 vertical periods after identification of the SECAM signal. Colour is switched off immediately the identification voltage disappears, or 1 vertical period later

Demodulator part

- Two quadrature demodulators with external reference tuned circuits
- Internal filtering of residual carrier in the demodulated colour difference signals
- De-emphasis circuit and colour switching stages in front of the output stages. The colour switching stages are controlled by the pulse processing part
- (B-Y) and (R-Y) colour difference output stages are low resistance n-p-n emitter followers

QUICK REFERENCE DATA

Supply voltage (pin 13)	$V_P = V_{13-9}$	typ.	12 V
Supply current (pin 13)	$I_P = I_{13}$	typ.	60 mA
Chrominance input signal (peak-to-peak)	$V_{15-9(p-p)}$	20 to 400	mV
Chrominance output signal (peak-to-peak)	$V_{12-9(p-p)}$	typ.	1,6 V
Colour difference output signals (peak-to-peak values)			
−(R-Y)	$V_{1-9(p-p)}$	typ.	1,05 V
−(B-Y)	$V_{3-9(p-p)}$	typ.	1,33 V
Sandcastle pulse; required amplitude for			
vertical and horizontal pulse separation	V_{24-9}	typ.	2,5 V
horizontal pulse separation	V_{24-9}	typ.	4,5 V
burst gating	V_{24-9}	min.	7,7 V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

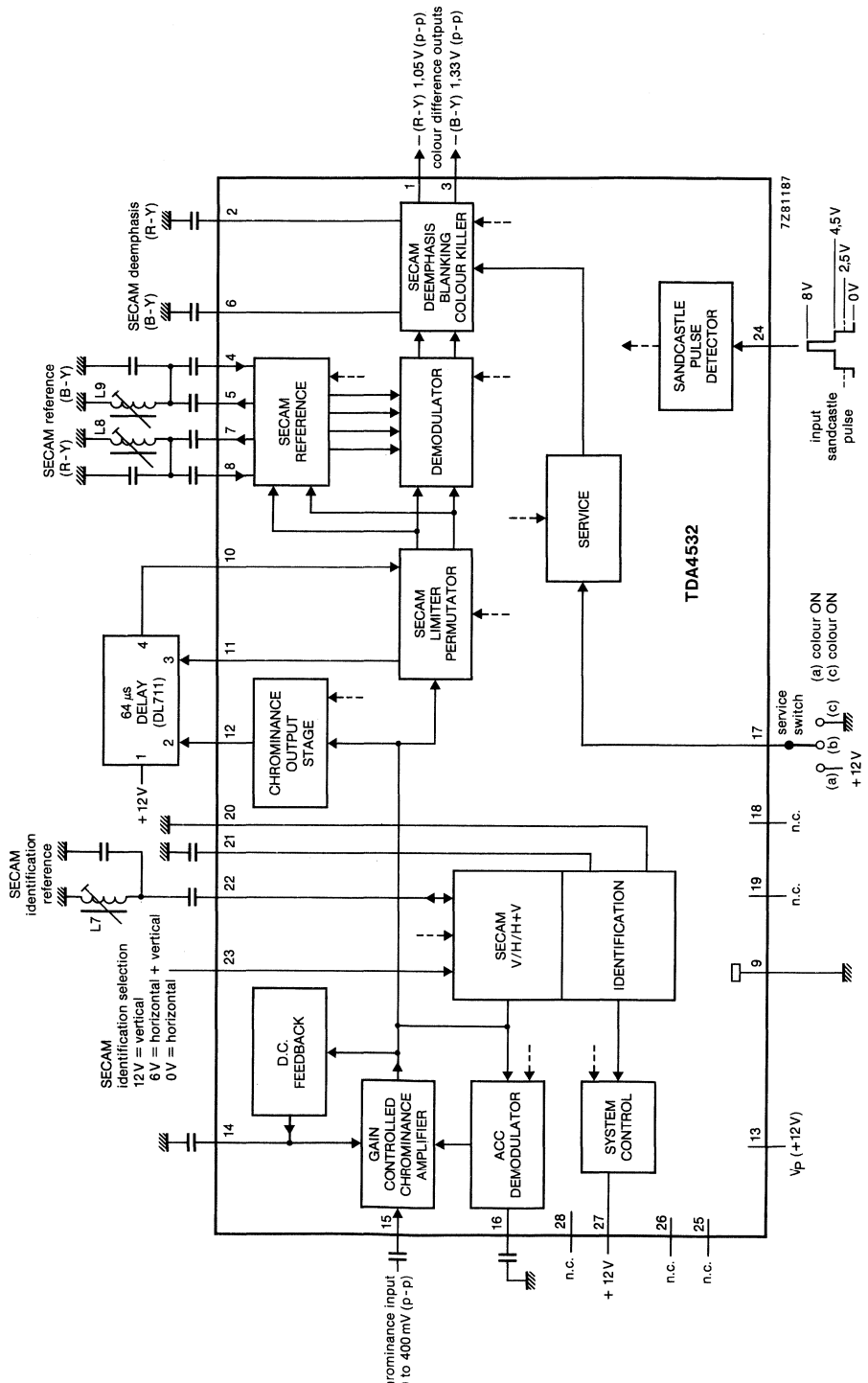


Fig. 1 Block diagram.

n.c. = not connected.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 13)	$V_P = V_{13-9}$	max.	13,2	V
Voltage range at pins 10, 11, 17, 23, 24, 27 to pin 9 (ground)	V_{n-9}		0 to V_P	V
Current at pin 12	I_{12}	max.	10	mA
Total power dissipation	P_{tot}	max.	1,4	W
Storage temperature range	T_{stg}		−25 to + 150	°C
Operating ambient temperature range	T_{amb}		0 to + 70	°C

DEVELOPMENT DATA

CHARACTERISTICS

$V_P = V_{13-9} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply (pin 13)					
Supply voltage range	$V_P = V_{13-9}$	10,8	–	13,2	V
Supply current	$I_P = I_{13}$	–	60	–	mA
Chrominance part					
Chrominance input signal (pin 15)					
input voltage (peak-to-peak value)	$V_{15-9(p-p)}$	20	100	400	mV
input impedance	$\lvert Z_{15-9}\rvert$	2,3	3,3	–	kΩ
Chrominance output signal (pin 12)					
output voltage (peak-to-peak value)	$V_{12-9(p-p)}$	–	1,6	–	V
output impedance (n-p-n emitter follower)	$\lvert Z_{12-9}\rvert$	–	–	20	Ω
d.c. output voltage	V_{12-9}	–	8,2	–	V
Input for delayed signal (pin 10)					
d.c. input current	I_{10}	–	–	10	μA
input resistance	R_{10-9}	10	–	–	kΩ
Demodulator part					
Colour difference output signals (note 1) output voltage (proportional to V_{13-9}) (peak-to-peak value)					
–(R-Y) signal (pin 1)	$V_{1-9(p-p)}$	–	1,05*	–	V
–(B-Y) signal (pin 3)	$V_{3-9(p-p)}$	–	1,33*	–	V
Ratio of colour difference output signals –(R-Y)/–(B-Y)	$V_{1/3-9}$	0,71*	0,79*	0,87*	
Residual carrier (4 to 5 MHz) (peak-to-peak value)	$V_{1,\ 3-9(p-p)}$	–	20	30	mV
Residual carrier (8 to 10 MHz) (peak-to-peak value)	$V_{1,\ 3-9(p-p)}$	–	20	30	mV
H/2 ripple at –(R-Y) –(B-Y) outputs (peak-to-peak value) with f_o signals	$V_{1,\ 3-9(p-p)}$	–	–	30	mV
D.C. output voltage	$V_{1,\ 3-9}$	–	7,7	–	V
Shift of inserted levels relative to levels of demodulated f_o frequencies (IC only) with temperature	$\Delta V/\Delta T$	–	0,5*	0,6*	mV/K
with supply voltage	$\Delta V/\Delta V_P$	–	8,0*	15*	mV/K

* Value measured without influence of external circuitry.

parameter	symbol	min.	typ.	max.	unit
Identification mode switch (pin 23)					
Input voltage for					
horizontal identification (H)	V_{23-9}	–	–	2	V
vertical identification (V)	V_{23-9}	10	–	–	V
combined (H) and (V) identification	V_{23-9}	–	6**	–	V
Colour killer delay time					
colour ON	t_{dC1}	–	–	3	field periods
colour OFF	t_{dC2}	–	–	1	field periods
Service switch					
Switching voltage (pin 17) (for forced colour ON)					
connected to ground	V_{17-9}	–	–	0,5	V
connected to supply voltage	V_{17-9}	6	–	–	V
Sandcastle pulse detector (note 2)					
Input voltage pulse levels (pin 24)					
to separate vertical and horizontal blanking pulses	V_{24-9}	1,3	1,6	1,9	V
required pulse amplitude	V_{24-9}	2,0	2,5	3,0	V
to separate horizontal blanking pulse	V_{24-9}	3,3	3,6	3,9	V
required pulse amplitude	V_{24-9}	4,1	4,5	4,9	V
to separate burst gating pulse	V_{24-9}	6,6	7,1	7,6	V
required pulse amplitude	V_{24-9}	7,7	–	–	V
Input voltage during horizontal scanning	V_{24-9}	–	–	1,1	V
Input current	$-I_{24}$	–	–	100	μA

DEVELOPMENT DATA

Notes to the characteristics

1. The signal amplitude of the colour difference output signals –(R-Y) and –(B-Y) is dependent on the characteristics of the external tuned circuits at pins 7, 8 and 4, 5 respectively. Adjustment of the amplitude is achieved by varying the Q-factor of these tuned circuits. The resonant frequency must be adjusted such that the demodulated output frequency (f_o) provides the same output level as the internally inserted reference voltage (achromatic value).
2. The sandcastle pulse is compared with three internal threshold levels, which are proportional to the supply voltage.

** Or not connected.

APPLICATION INFORMATION

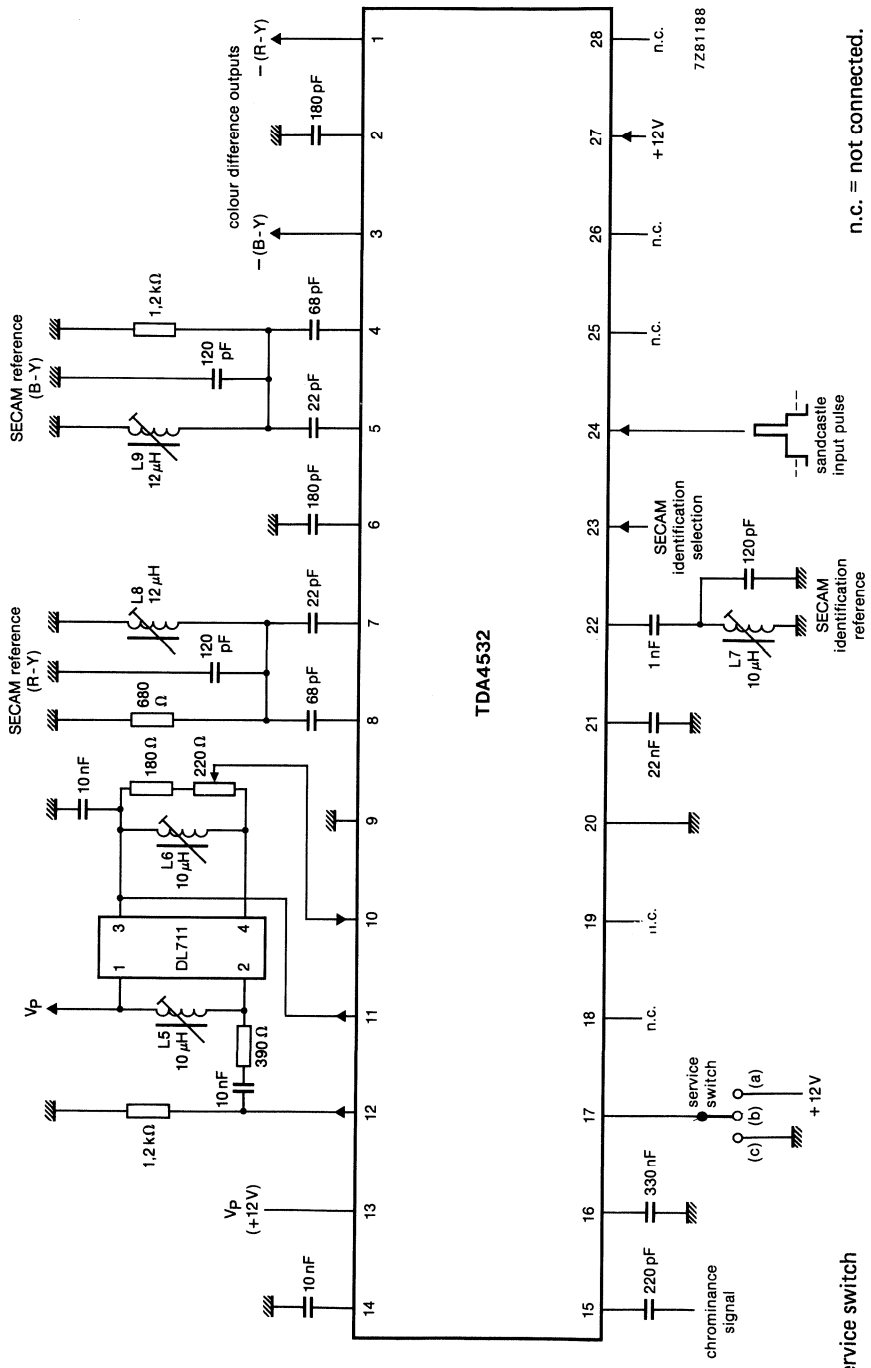


Fig. 2 Application diagram.

Service switch
(a) colour ON
(c) colour ON)

MULTISTANDARD DECODER

GENERAL DESCRIPTION

The TDA4555 and TDA4556 are monolithic integrated multistandard colour decoders for the PAL, SECAM, NTSC 3,58 MHz and NTSC 4,43 MHz standards. The difference between the TDA4555 and the TDA4556 is the polarity of the colour difference output signals (B-Y) and (R-Y).

Features

Chrominance part

- Gain controlled chrominance amplifier for PAL, SECAM and NTSC
- ACC rectifier circuits (PAL/NTSC, SECAM)
- Burst blanking (PAL) in front of 64 μs glass delay line
- Chrominance output stage for driving the 64 μs glass delay line (PAL, SECAM)
- Limiter stages for direct and delayed SECAM signal
- SECAM permutator

Demodulator part

- Flyback blanking incorporated in the two synchronous demodulators (PAL, NTSC)
- PAL switch
- Internal PAL matrix
- Two quadrature demodulators with external reference tuned circuits (SECAM)
- Internal filtering of residual carrier
- De-emphasis (SECAM)
- Insertion of reference voltages as achromatic value (SECAM) in the (B-Y) and (R-Y) colour difference output stages (blanking)

Identification part

- Automatic standard recognition by sequential inquiry
- Delay for colour-on and scanning-on
- Reliable SECAM identification by PAL priority circuit
- Forced switch-on of a standard
- Four switching voltages for chrominance filters, traps and crystals
- Two identification circuits for PAL/SECAM (H/2) and NTSC
- PAL/SECAM flip-flop
- SECAM identification mode switch (horizontal, vertical or combined horizontal and vertical)
- Crystal oscillator with divider stages and PLL circuitry (PAL, NTSC) for double colour subcarrier frequency
- HUE control (NTSC)
- Service switch

QUICK REFERENCE DATA

Supply voltage (pin 13)	$V_P = V_{13-9}$	typ.	12	V
Supply current (pin 13)	$I_P = I_{13}$	typ.	65	mA
Chrominance input signal (peak-to-peak)	$V_{15-9(p-p)}$		20 to 200	mV
Chrominance output signal (peak-to-peak)	$V_{12-9(p-p)}$	typ.	1,6	V
Colour difference output signals (peak-to-peak values)				
TDA4555: −(R-Y); **TDA4556:** + (R-Y)	$V_{1-9(p-p)}$	typ.	1,05	V ± 2 dB
TDA4555: −(B-Y); **TDA4556:** + (B-Y)	$V_{3-9(p-p)}$	typ.	1,33	V ± 2 dB
Sandcastle pulse; required amplitude for				
vertical and horizontal pulse separation	V_{24-9}	typ.	2,5	V
horizontal pulse separation	V_{24-9}	typ.	4,5	V
burst gating	V_{24-9}	typ.	7,7	V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

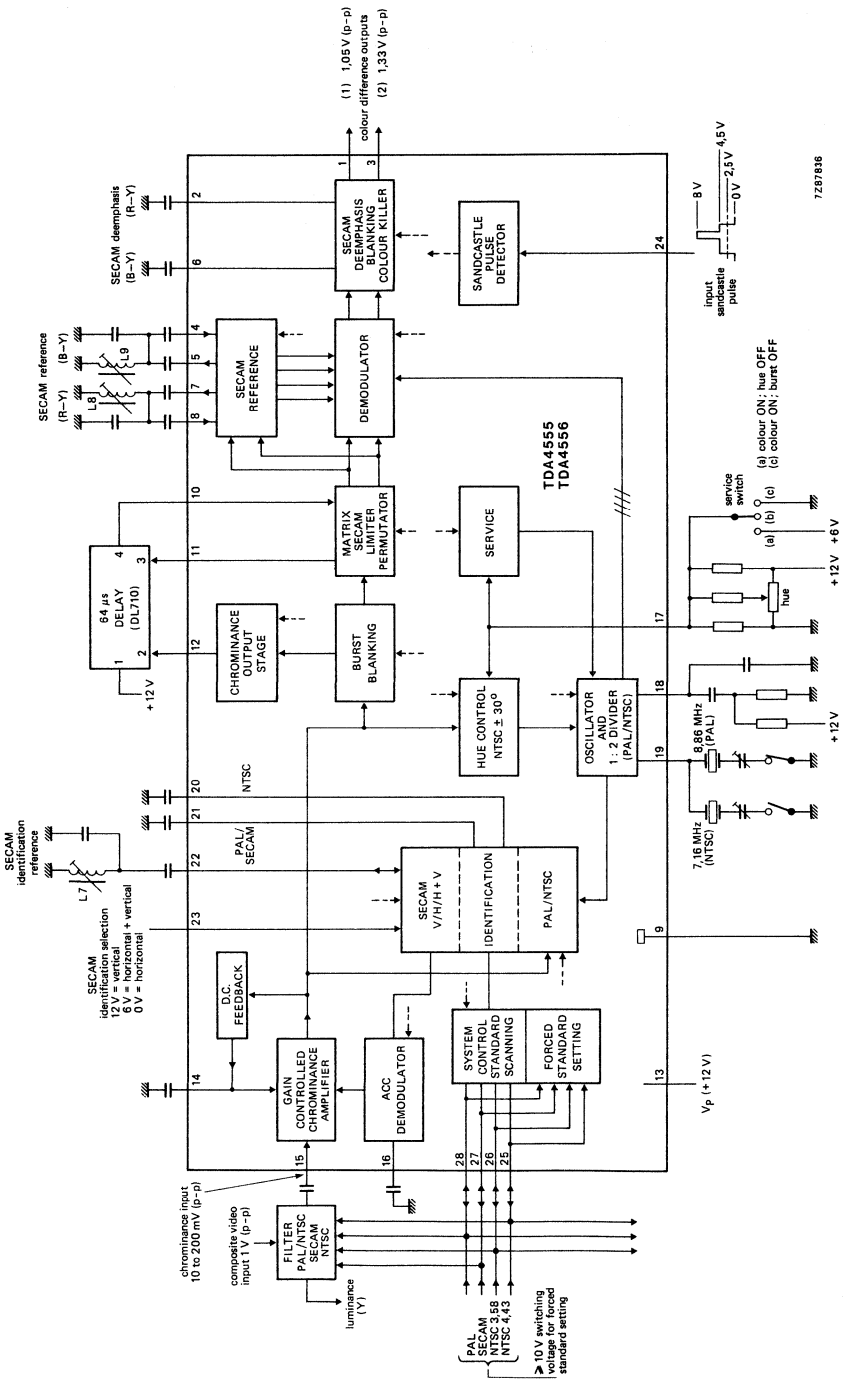


Fig. 1 Block diagram.

(1) TDA4555: —(R-Y); TDA4556: + (R-Y)
(2) TDA4555: —(B-Y); TDA4556: + (B-Y)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 13)	$V_P = V_{13-9}$	max.	13,2	V
Voltage range at pins 10, 11, 17, 23, 24, 25, 26, 27, 28 to pin 9 (ground)	V_{n-9}		0 to V_P	V
Current at pin 12	I_{12}	max.	8	mA
Peak value	I_{12M}	max.	15	mA
Total power dissipation	P_{tot}	max.	1,4	W
Storage temperature range	T_{stg}		−25 to +150	°C
Operating ambient temperature range	T_{amb}		0 to +70	°C

CHARACTERISTICS

$V_P = V_{13-9} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 13)					
Supply voltage range	$V_P = V_{13-9}$	10,8	–	13,2	V
Supply current	$I_P = I_{13}$	–	65	–	mA
Chrominance part					
Chrominance input signal (pin 15)					
input voltage with 75% colour bar signal (peak-to-peak value)	$V_{15-9(p-p)}$	20	100	200	mV
input impedance	$\|Z_{15-9}\|$	2,3	3,3	–	kΩ
Chrominance output signal (pin 12)					
output voltage (peak-to-peak value)	$V_{12-9(p-p)}$	–	1,6	–	V
output impedance (n-p-n emitter follower)	$\|Z_{12-9}\|$	–	–	20	Ω
d.c. output voltage	V_{12-9}	–	8,2	–	V
Input for delayed signal (pin 10)					
d.c. input current	I_{10}	–	–	10	μA
input resistance	R_{10-9}	10	–	–	kΩ
Demodulator part (PAL/NTSC)					
Colour difference output signals					
output voltage (proportional to V_{13-9}) (peak-to-peak value)					
TDA4555					
– (R-Y) signal (pin 1)	$V_{1-9(p-p)}$	–	1,05 V ± 2 dB	–	V
– (B-Y) signal (pin 3)	$V_{3-9(p-p)}$	–	1,33 V ± 2 dB	–	V
TDA4556					
+ (R-Y) signal (pin 1)	$V_{1-9(p-p)}$	–	1,05 V ± 2 dB	–	V
+ (B-Y) signal (pin 3)	$V_{3-9(p-p)}$	–	1,33 V ± 2 dB	–	V
Ratio of colour difference output signals (R-Y)/(B-Y)	$V_{1/3-9}$	–	0,79 ± 10%	–	
Residual carrier (subcarrier frequency) (peak-to-peak value)	$V_{1,3-9(p-p)}$	–	–	30	mV
Residual carrier (PAL only) (peak-to-peak value)	$V_{1,3-9(p-p)}$	–	10	–	mV
H/2 ripple at (R-Y) output (pin 1) (peak-to-peak value) without input signal	$V_{1-9(p-p)}$	–	–	10	mV
D.C. output voltage n-p-n emitter follower with internal current source of 0,3 mA	$V_{1,3-9}$	–	7,7	–	V
output impedance	$\|Z_{1,3-9}\|$	–	–	150	Ω

parameter	symbol	min.	typ.	max.	unit
Demodulator part (SECAM)					
Colour difference signals (see note 1) output voltage (proportional to V_{13-9}) (peak-to-peak value) TDA4555					
–(R-Y) signal (pin 1	$V_{1-9(p-p)}$	–	1,05	–	V
– (B-Y) signal (pin 3)	$V_{3-9(p-p)}$	–	1,33	–	V
TDA4556					
+ (R-Y) signal (pin 1)	$V_{1-9(p-p)}$	–	1,05	–	V
+ (B-Y) signal (pin 3)	$V_{3-9(p-p)}$	–	1,33	–	V
Ratio of colour difference output signals (R-Y)/(B-Y)	$V_{1/3-9}$	–	0,79* ± 10%	–	
Residual carrier (4 to 5 MHz) (peak-to-peak value)	$V_{1,3-9(p-p)}$	–	20	30	mV
Residual carrier (8 to 10 MHz) (peak-to-peak value)	$V_{1,3-9(p-p)}$	–	20	30	mV
H/2 ripple at (R-Y) (B-Y) outputs (pins 1 and 3) (peak-to-peak value) with f_o signals	$V_{1,3-9(p-p)}$	–	–	20	mV
D.C. output voltage	$V_{1,3-9}$	–	7,7	–	V
Shift of inserted levels relative to levels of demodulated f_o frequencies (IC only)	$\Delta V/\Delta T(R-Y)$	–	–0,55	–	mV/K
	$\Delta V/\Delta T(B-Y)$	–	+0,25	–	mV/K
HUE control (NTSC)/service switch					
Phase shift of reference carrier at V_{17-9} = 2 V	$-\phi$	–	30**	–	deg
at V_{17-9} = 3 V	ϕ	–	0	–	deg
at V_{17-9} = 4 V	$+\phi$	–	30**	–	deg
Input resistance	R_{17-9}	–	5	–	kΩ
Service position					
Switching voltage (pin 17) burst OFF; colour ON (for oscillator adjustment)	V_{17-9}	–	–	0,5	V
HUE control OFF; colour ON (for forced colour ON)	V_{17-9}	6	–	–	V
Crystal oscillator (pin 19)					
For double colour subcarrier frequency input resistance	R_{19-9}	–	350	–	Ω
lock-in-range referred to subcarrier frequency	Δf	± 400	–	–	Hz

* Value measured without influence of external circuitry.

** Relative to phase at V_{17-9} = 3 V.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Identification part					
Switching voltages for chrominance filters and crystals at pin 28 (PAL) at pin 27 (SECAM) at pin 26 (NTSC 3,58 MHz) at pin 25 (NTSC 4,43 MHz)					
Control voltage OFF state	$V_{25,26,27,28-9}$	–	–	0,5	V
Control voltage ON state during scanning; colour OFF	$V_{25,26,27,28-9}$	–	2,45	–	V
colour ON	$V_{25,26,27,28-9}$	–	5,8	–	V
Output current	$-I_{25,26,27,28-9}$	–	–	3	mA
Voltage for forced switching ON PAL	V_{28-9}	9	–	–	V
SECAM	V_{27-9}	9	–	–	V
NTSC 3,58 MHz	V_{26-9}	9	–	–	V
NTSC 4,43 MHz	V_{25-9}	9	–	–	V
Delay time for restart of scanning	t_{dS}	2 to 3 vertical periods			
colour ON	t_{dC1}	2 to 3 vertical periods			
colour OFF	t_{dC2}	0 to 1 vertical periods			
SECAM identification (pin 23)					
Input voltage for horizontal identification (H)	V_{23-9}	–	–	2	V
vertical identification (V)	V_{23-9}	10	–	–	V
combined (H) and (V) identification	V_{23-9}	–	6*	–	V
Sequence of standard inquiry PAL-SECAM-NTSC 3,58 MHz-NTSC 4,43 MHz Reliable SECAM identification by PAL priority circuit					
Scanning time for each standard	t_S	4 vertical periods			

* Or not connected.

parameter	symbol	min.	typ.	max.	unit
Sandcastle pulse detector (see note 2)					
Input voltage pulse levels (pin 24) to separate vertical and horizontal blanking pulses	$V_{24\text{-}9}$	1,2	–	2,0	V
required pulse amplitude	$V_{24\text{-}9(p\text{-}p)}$	2,0	–	3,0	V
to separate horizontal blanking pulse	$V_{24\text{-}9}$	3,2	–	4,0	V
required pulse amplitude	$V_{24\text{-}9(p\text{-}p)}$	4,0	–	5,0	V
to separate burst gating pulse	$V_{24\text{-}9}$	6,5	–	7,7	V
required pulse amplitude	$V_{24\text{-}9(p\text{-}p)}$	7,7	–	V_P	V
Input voltage during horizontal scanning	$V_{24\text{-}9}$	–	–	1,0	V
Input current	$-I_{24}$	–	–	100	μA

Notes to the characteristics

1. The signal amplitude of the colour difference signals (R-Y) and B-Y) is dependent on the characteristics of the external tuned circuits at pins 7, 8 and 4, 5 respectively. Adjustment of the amplitude is achieved by varying the Q-factor of these tuned circuits. The resonant frequency must be adjusted such that the demodulated output frequency (f_o) provides the same output level as the internally inserted reference voltage (achromatic value).
2. The sandcastle pulse is compared with three internal threshold levels, which are proportional to the supply voltage.

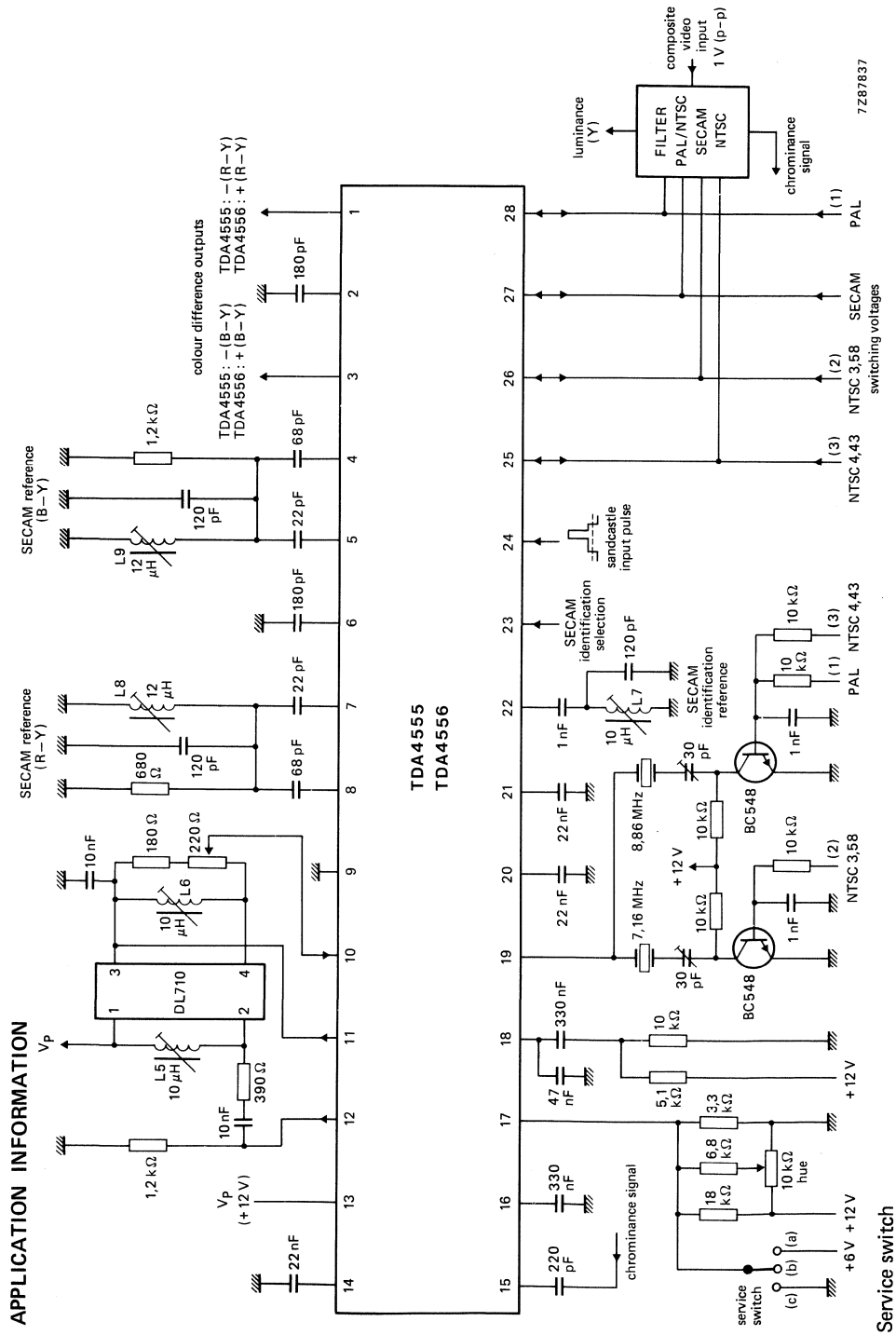


Fig. 2 Application diagram.

MULTISTANDARD DECODER

GENERAL DESCRIPTION

The TDA4557 is a monolithic integrated multistandard colour decoder for the PAL, SECAM, NTSC 3.58 MHz and NTSC 4.43 MHz standards.

Features

Chrominance part

- Gain controlled chrominance amplifier for PAL, SECAM and NTSC
- ACC rectifier circuits (PAL/NTSC, SECAM)
- Burst blanking (PAL) in front of 64 μs glass delay line
- Chrominance output stage for driving the 64 μs glass delay line (PAL, SECAM)
- Limiter stages for direct and delayed SECAM signal
- SECAM permutator

Demodulator part

- Flyback blanking incorporated in the demodulators (PAL, NTSC, SECAM)
- PAL switch
- Internal PAL matrix
- Two quadrature demodulators with external reference tuned circuits (SECAM)
- Internal filtering of residual carrier
- De-emphasis (SECAM)

Identification part

- Automatic standard recognition by sequential inquiry
- Delay for colour-on and scanning-on
- Reliable SECAM identification by PAL priority circuit and 50/60 Hz recognition
- Forced switch-on of a standard
- Four switching voltages for chrominance filters, traps and crystals
- Two identification circuits for PAL/SECAM (H/2) and NTSC
- PAL/SECAM flip-flop
- SECAM identification mode switch (horizontal, vertical or combined horizontal and vertical)
- Crystal oscillator with divider stages and PLL circuitry (PAL, NTSC) for double colour subcarrier frequency
- HUE control (NTSC)
- Service switch

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 13)	V_P	10.8	12.0	13.2	V
Supply current (pin 13)	I_P	–	65	–	mA
Chrominance input voltage (peak-to-peak value)	$V_{15(p-p)}$	20	100	400	mV
Chrominance output voltage (peak-to-peak value)	$V_{12(p-p)}$	–	1.6	–	V
Colour difference output voltages (peak-to-peak values)					
–(R-Y)	$V_{1(p-p)}$	–	1.05 V ± 2 dB	–	V
–(B-Y)	$V_{3(p-p)}$	–	1.33 V ± 2 dB	–	V
Sandcastle pulse (pin 24)					
Required amplitude to separate					
vertical and horizontal pulse	$V_{24(p-p)}$	2.0	2.5	3.0	V
horizontal pulse	$V_{24(p-p)}$	4.1	4.5	4.9	V
burst gating pulse	$V_{24(p-p)}$	7.7	–	V_P	V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

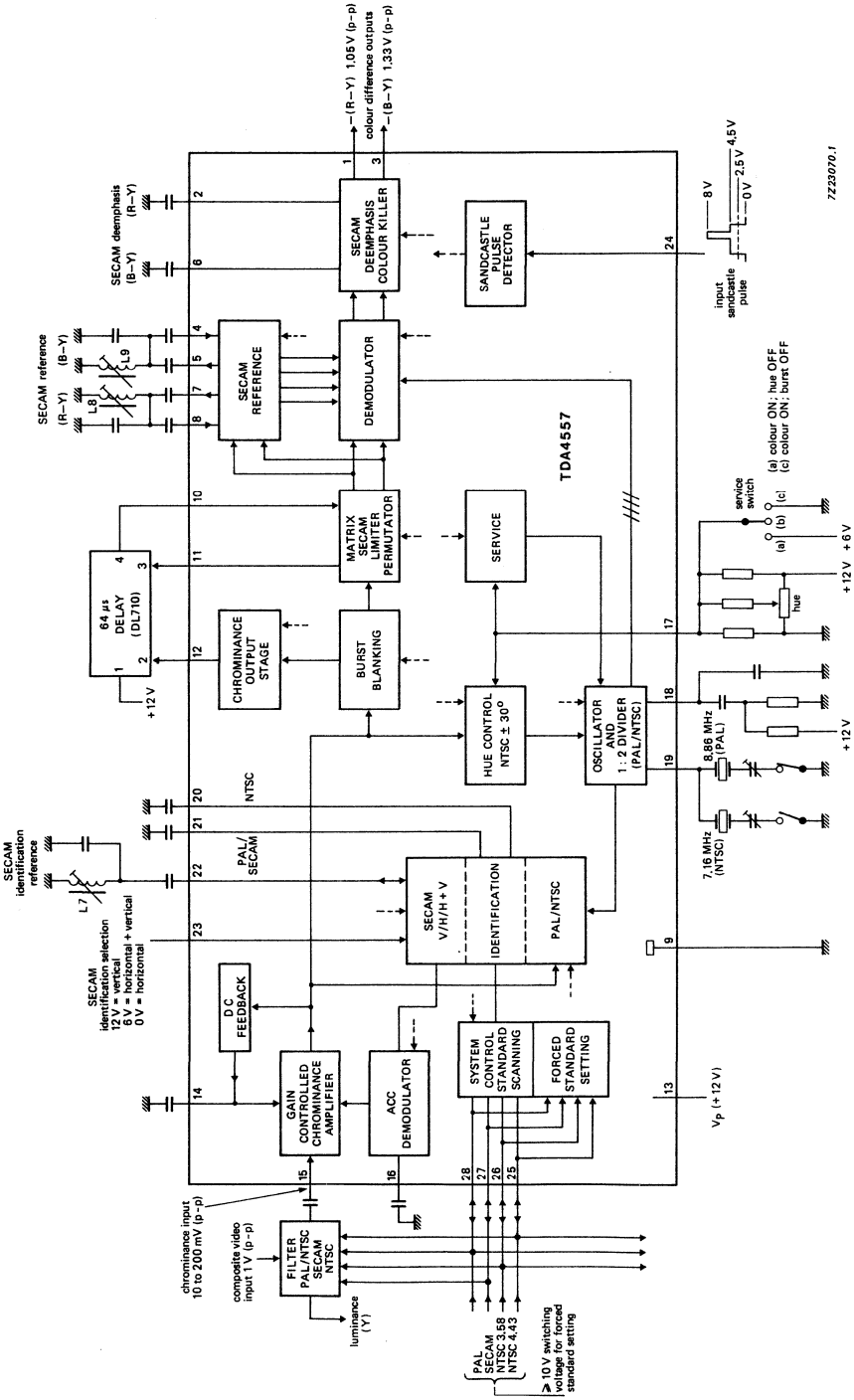


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 13)	V_P	–	13.2	V
Voltage range at pins 10, 11, 17, 23, 24, 25, 26, 27, 28 to pin 9 (ground)	$V_{n\text{-}9}$	0	V_P	V
Current at pin 12	I_{12}	–	8	mA
Peak value	I_{12M}	–	15	mA
Total power dissipation	P_{tot}	–	1.4	W
Storage temperature range	T_{stg}	–25	+ 150	°C
Operating ambient temperature range	T_{amb}	0	+ 70	°C

DEVELOPMENT DATA

CHARACTERISTICS

$V_P = V_{13-9} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 13)					
Supply voltage range	V_P	10.8	12	13.2	V
Supply current	I_P	50	65	80	mA
Chrominance part					
Chrominance input signal (pin 15)					
input voltage with 75% colour bar signal (peak-to-peak value)	$V_{15(p-p)}$	20	100	400	mV
input impedance	$\|Z_{15-9}\|$	7	10	–	kΩ
Chrominance output signal (pin 12)					
output voltage (peak-to-peak value)	$V_{12(p-p)}$	1.1	1.6	1.75	V
output impedance (npn emitter follower)	$\|Z_{12-9}\|$	–	–	20	Ω
DC output voltage	V_{12-9}	7.3	8.2	9.0	V
Input for delayed signal (pin 10)					
DC input current	I_{10}	–	–	10	μA
input resistance	R_{10-9}	10	–	–	kΩ
Demodulator part (PAL/NTSC)					
Colour difference output signals					
output voltage (proportional to V_{13-9}) (peak-to-peak value)					
– (R-Y) signal (pin 1)	$V_{1(p-p)}$	–	1.05 V ± 2 dB	–	V
– (B-Y) signal (pin 3)	$V_{3(p-p)}$	–	1.33 V ± 2 dB	–	V
Ratio of colour difference output signals (R-Y)/(B-Y)	$V_{1/3-9}$	–	0.79 ± 10%	–	
Residual carrier (subcarrier frequency) (peak-to-peak value)	$V_{1,3(p-p)}$	–	–	30	mV
Residual carrier (PAL only) (peak-to-peak value)	$V_{1,3(p-p)}$	–	10	–	mV
H/2 ripple at (R-Y) output (pin 1) (peak-to-peak value) without input signal	$V_{1(p-p)}$	–	–	10	mV
DC output voltage					
npn emitter follower with internal current source of 0.3 mA	$V_{1,3-9}$	7.0	7.7	8.4	V
output impedance	$\|Z_{1,3-9}\|$	–	–	150	Ω

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Demodulator part (SECAM)					
Colour difference signals (see note 1) output voltage (proportional to V_{13-9}) (peak-to-peak value)					
—(R-Y) signal (pin 1	$V_{1(p-p)}$	—	1.05	—	V
— (B-Y) signal (pin 3)	$V_{3(p-p)}$	—	1.33	—	V
Ratio of colour difference output signals (R-Y)/(B-Y)	$V_{1/3-9}$	—	0.79* ± 10%	—	
Residual carrier (4 to 5 MHz) (peak-to-peak value)	$V_{1,3(p-p)}$	—	20	30	mV
Residual carrier (8 to 10 MHz) (peak-to-peak value)	$V_{1,3(p-p)}$	—	20	30	mV
H/2 ripple at (R-Y) (B-Y) outputs (pins 1 and 3) (peak-to-peak value) with f_o signals	$V_{1,3(p-p)}$	—	—	30	mV
DC output voltage	$V_{1,3-9}$	7.0	7.7	8.4	V
Shift of inserted levels relative to levels of demodulated f_o frequencies (IC only)	$\Delta V/\Delta T(R-Y)$	—	0.5	0.6	mV/K
	$\Delta V/\Delta V_P$	—	8	—	mV/V
HUE control (NTSC)/service switch					
Phase shift of reference carrier at V_{17-9} = 2 V	$-\phi$	30	40	—	deg
at V_{17-9} = 3 V	ϕ	—	0	—	deg
at V_{17-9} = 4 V	$+\phi$	30	40	—	deg
Input resistance	R_{17-9}	—	5	—	kΩ
Service position					
Switching voltage (pin 17) burst OFF; colour ON (for oscillator adjustment)	V_{17-9}	0	—	0.5	V
HUE control OFF; colour ON (for forced colour ON)	V_{17-9}	6	—	V_P	V
Crystal oscillator (pin 19)					
For double colour subcarrier frequency input resistance	R_{19-9}	—	350	—	Ω
lock-in-range referred to subcarrier frequency	Δf	± 400	—	—	Hz

* Value measured without influence of external circuitry.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Identification part					
Switching voltages for chrominance filters and crystals at pin 28 (PAL) at pin 27 (SECAM) at pin 26 (NTSC 3.58 MHz) at pin 25 (NTSC 4.43 MHz)					
Control voltage OFF state	$V_{25,26,27,28-9}$	–	–	0.5	V
Control voltage ON state during scanning; colour OFF	$V_{25,26,27,28-9}$	2.1	2.45	2.7	V
colour ON	$V_{25,26,27,28-9}$	5.5	5.8	6.2	V
Output current	$-I_{25,26,27,28-9}$	–	–	3	mA
Voltage for forced switching ON PAL	V_{28-9}	9	–	V_P	V
SECAM	V_{27-9}	9	–	V_P	V
NTSC 3.58 MHz	V_{26-9}	9	–	V_P	V
NTSC 4.43 MHz	V_{25-9}	9	–	V_P	V
Delay time for restart of scanning	t_{dS}	2 to 3 vertical periods			
colour ON	t_{dC1}	2 to 3 vertical periods			
colour OFF	t_{dC2}	0 to 1 vertical periods			
SECAM identification (pin 23)					
Input voltage for horizontal identification (H)	V_{23-9}	0	–	2	V
vertical identification (V)	V_{23-9}	10	–	V_P	V
combined (H) and (V) identification	V_{23-9}	–	6*	–	V
Sequence of standard inquiry PAL-SECAM-NTSC 3.58 MHz-NTSC 4.43 MHz Reliable SECAM identification by PAL priority circuit					
Scanning time for each standard	t_S	4 vertical periods			

* Or not connected.

parameter	symbol	min.	typ.	max.	unit
Sandcastle pulse detector (see note 2)					
Input voltage pulse levels (pin 24) to separate vertical and horizontal blanking pulses	$V_{24\text{-}9}$	1.3	1.6	1.9	V
required pulse amplitude	$V_{24(p\text{-}p)}$	2.0	2.5	3.0	V
to separate horizontal blanking pulse	$V_{24\text{-}9}$	3.3	3.6	3.9	V
required pulse amplitude	$V_{24(p\text{-}p)}$	4.1	4.5	4.9	V
to separate burst gating pulse	$V_{24\text{-}9}$	6.6	7.1	7.6	V
required pulse amplitude	$V_{24(p\text{-}p)}$	7.7	–	V_P	V
Input voltage during horizontal scanning	$V_{24\text{-}9}$	–	–	1.0	V
Input current	$-I_{24}$	–	–	100	μA

Notes to the characteristics

1. The signal amplitude of the colour difference signals (R-Y) and B-Y) is dependent on the characteristics of the external tuned circuits at pins 7, 8 and 4, 5 respectively. Adjustment of the amplitude is achieved by varying the Q-factor of these tuned circuits. The resonant frequency must be adjusted such that the demodulated output frequency (f_o) provides the same output level as the internally inserted reference voltage (achromatic value).
2. The sandcastle pulse is compared with three internal threshold levels, which are proportional to the supply voltage.

DEVELOPMENT DATA

APPLICATION INFORMATION

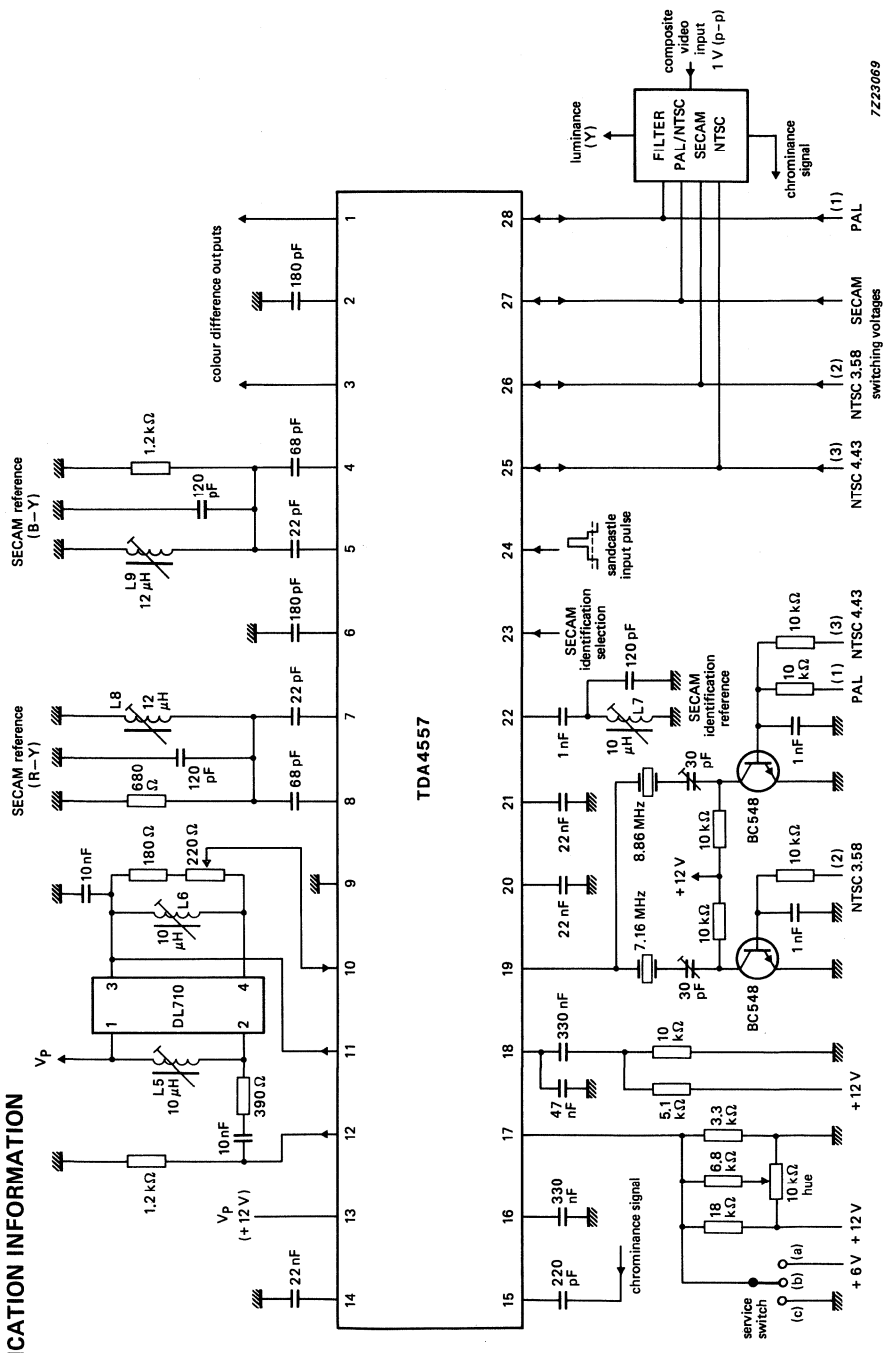


Fig. 2 Application diagram.

Service switch
(a) colour ON; hue OFF
(c) colour ON; burst OFF

COLOUR TRANSIENT IMPROVEMENT CIRCUIT

GENERAL DESCRIPTION

The TDA4560 is a monolithic integrated circuit for colour transient improvement (CTI) and luminance delay line in gyrator technique in colour television receivers.

Features

- Colour transient improvement for colour difference signals (R-Y) and (B-Y) with transient detecting-, storage- and switching stages resulting in high transients of colour difference output signals
- A luminance signal path (Y) which substitutes the conventional Y-delay coil with an integrated Y-delay line
- Switchable delay time from 720 ns to 1035 ns in steps of 45 ns
- Output for the option of velocity modulation

QUICK REFERENCE DATA

Supply voltage (pin 10)	$V_P = V_{10-18}$	typ.	12 V
Supply current (pin 10)	$I_P = I_{10}$	typ.	35 mA
(R-Y) and (B-Y) attenuation	α_{cd}	typ.	0 dB
(R-Y) and (B-Y) output transient time	t_{tr}	typ.	150 ns
Adjustable Y-delay time	t_d		720 to 1035 ns
Y-attenuation	α_y	typ.	7 dB

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

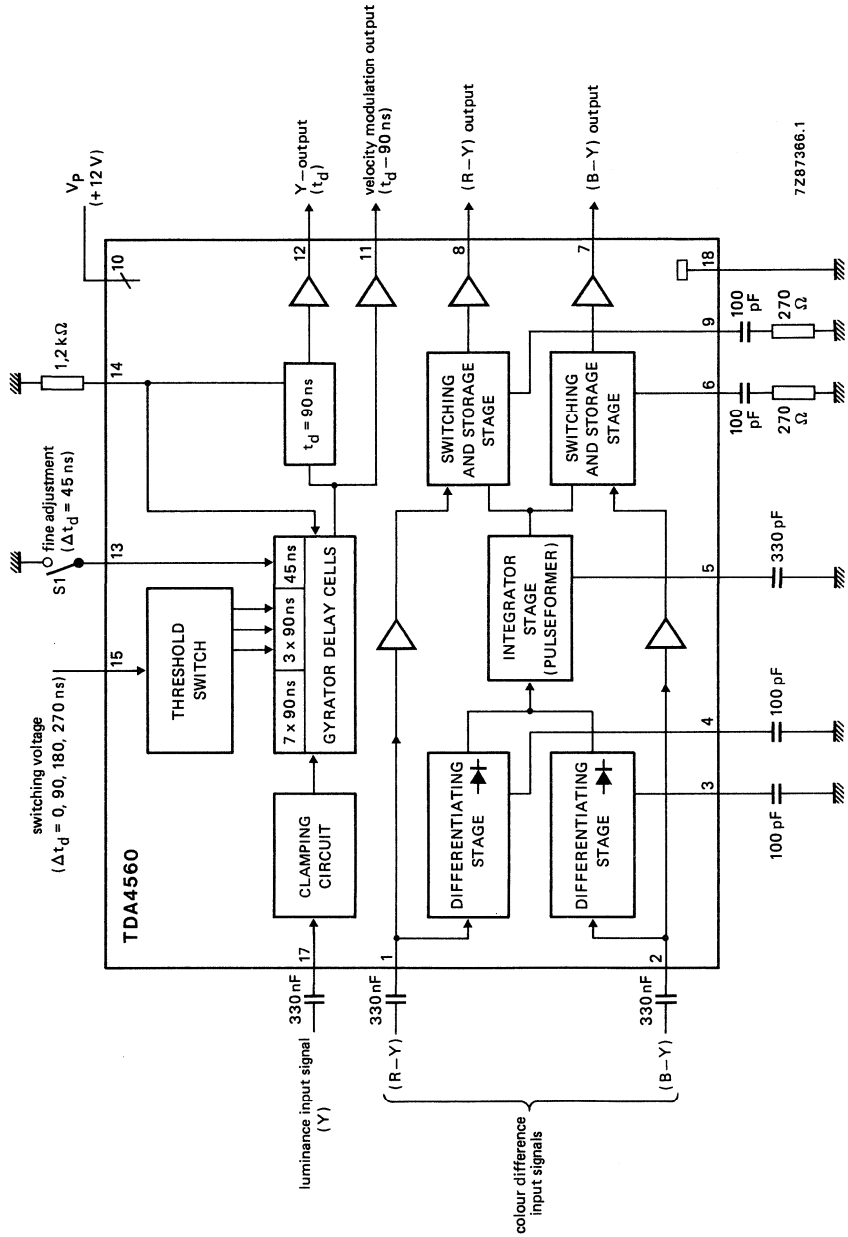


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

The IC consists of two colour difference channels (B-Y) and (R-Y) and a luminance signal path (Y) as shown in Fig. 1.

Colour difference channels

The (B-Y) and (R-Y) colour difference channels consist of a buffer amplifier at the input, a switching stage and an output amplifier. The switching stages, which are controlled by transient detecting stages (differentiators), switch to a value that has been stored at the beginning of the transients. The differentiating stages get their signal direct from the colour difference detecting signal (pins 1 and 2). Two parallel storage stages are incorporated in which the colour difference signals are stored during the transient time of the signal. After a time of about 600 ns they are switched immediately (transient time of 150 ns) to the outputs. The colour difference channels are not attenuated.

Y-signal path

The Y-signal input (pin 17) is capacitively coupled to an input clamping circuit. Gyrator delay cells provide a maximum delay of 1035 ns including an additional delay of 45 ns via the fine adjustment switch (S1) at pin 13. Three delay cells are switched with two interstage switches dependent on the voltage at pin 15. Thus three switchable delay times of 90 ns, 180 ns or 270 ns less than the maximum delay time are available. A tuning compensation circuit ensures accuracy of delay time despite process tolerances. The Y-signal path has a 7 dB attenuation as a normal Y-delay coil and can replace this completely. The output is fed to pin 12 via a buffer amplifier. An additional output stage provides a signal of 90 ns less delay at pin 11 for the option of velocity modulation.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC)

Supply voltage (pin 10)	$V_P = V_{10-18}$	max. 13,2	V
Voltage ranges to pin 18 (ground)			
at pins 1,2,12,15	V_{n-18}	0 to V_P	V
at pin 11	V_{11-18}	0 to (V_P–3V)	V
at pin 17	V_{17-18}	0 to 7	V
Voltage ranges			
at pin 7 to pin 6	V_{7-6}	0 to 5	V
at pin 8 to pin 9	V_{8-9}	0 to 5	V
Currents			
at pins 6,9	$\pm I_{6,9}$	max. 15	mA
at I_7, I_8, I_{11}, I_{12}		internally limited	
Total power dissipation	P_{tot}	max. 1,1	W
Storage temperature range	T_{stg}	–25 to +150	°C
Operating ambient temperature range	T_{amb}	0 to +70	°C

Note

Pins 3, 4, 5, 6, 9, 13 and 14 d.c. potential not published.

CHARACTERISTICS

$V_P = V_{10-18} = 12$ V; $T_{amb} = 25$ °C; measured in application circuit Fig. 2; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 10)					
Supply voltage	$V_P = V_{10-18}$	10,8	12	13,2	V
Supply current	$I_P = I_{10}$	–	35	50	mA
Colour difference channels (pins 1 and 2);					
(R-Y) input voltage (peak-to-peak value) 75% colour bar signal	V_{1-18}	–	1,05	–	V
(B-Y) input voltage (peak-to-peak value) 75% colour bar signal	V_{2-18}	–	1,33	–	V
Input resistance	$R_{1,\ 2-18}$	–	12	–	kΩ
Internal bias (input)	$V_{1,\ 2-18}$	–	4,3	–	V
(B-Y), (R-Y) signal attenuation $\frac{V_8}{V_1}, \frac{V_7}{V_2}$	α_{cd}	–	0	–	dB
Output voltage (d.c.)	$V_{7,\ 8-18}$	–	4,4	–	V
Output current (emitter follower with constant current source 0,65 mA)	$-I_{7,8}$	–	1,2	–	mA
(R-Y) and B-Y) output signal transient time	t_{tr}	–	150	–	ns
Y-signal path (pin 17)					
Y-input voltage (composite signal) (peak-to-peak value)	$V_{17-18(p-p)}$	–	1	–	V
Internal bias voltage (during clamping)	V_{17-18}	–	1,5	–	V
Input current during picture content	I_{17}	–	8	–	μA
during synchronizing pulse	$-I_{17}$	–	100	–	μA
Y-signal attenuation $\frac{V_{11}}{V_{17}}$	α_Y	–	8	–	dB
Y-signal attenuation $\frac{V_{12}}{V_{17}}$	α_Y	–	7	–	dB
Output voltage (d.c.)	V_{11-18}	–	2,3	–	V
Output voltage (d.c.)	V_{12-18}	–	10,3	–	V
Output current (emitter follower with constant current source 0,45 mA)	$-I_{11,12}$	–	1,2	–	mA
Frequency response (note 1) $R_{14-18} = 1{,}2$ kΩ; $V_{15-18} = 12$ V	f_{12-17}	–	5	–	MHz

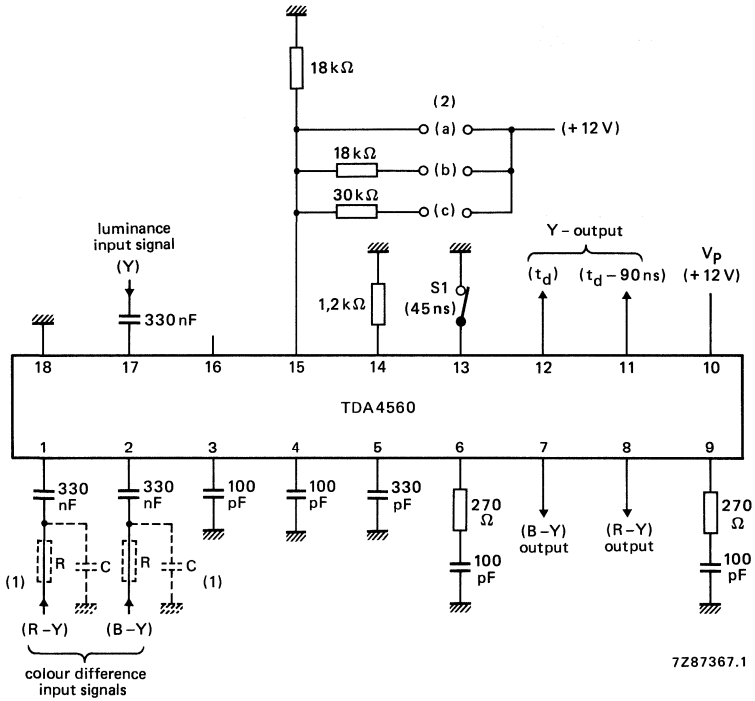
CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Y-signal path (pin 17)					
Adjustable delay (note 2) (switch open)					
at V_{15-18} = 0 to 2,5 V; R_{14-18} = 1,2 kΩ	t_d	–	720	–	ns
at V_{15-18} = 3,5 to 5,5 V; R_{14-18} = 1,2 kΩ	t_d	–	810	–	ns
at V_{15-18} = 6,5 to 8,5 V; R_{14-18} = 1,2 kΩ	t_d	–	900	–	ns
at V_{15-18} = 9,5 to 12 V; R_{14-18} = 1,2 kΩ	t_d	–	990	–	ns
Fine adjustment delay (switch S1 closed)					
at V_{13-18} = 0 V	Δt_d	–	45	–	ns
Signal delay for velocity modulation (pin 11)	t		t_d – 90 ns		
Thermal resistance					
From junction to ambient (in free air)	$R_{th\ j-a}$	–	–	70	K/W

NOTES TO THE CHARACTERISTICS

1. R_{14-18} influences the bandwidth.
2. Delay time is proportional to resistor R_{14-18}.

APPLICATION INFORMATION



(1) Residual carrier reduced to 20 mV peak-to-peak (R = 1 kΩ, C = 100 pF).
(2) Switching sequence for delay times shown in Table 1.

Fig. 2 Application diagram and test circuit.

Table 1 Switching sequence for delay times.

connection			voltage at pin 15	delay time (ns)*
(a)	(b)	(c)		
O	O	O	0 to 2,5 V	720
O	O	X	3,5 to 5,5 V	810
O	X	X	6,5 to 8,5 V	900
X	X	X	9,5 to 12 V	990

Where: X = connection closed; O = connection open.

* When switch (S1) is closed the delay time is increased by 45 ns.

COLOUR TRANSIENT IMPROVEMENT CIRCUIT

GENERAL DESCRIPTION

The TDA4565 is a monolithic integrated circuit for coulour transient improvement (CTI) and luminance delay line in gyrator technique in colour television receivers.

Features

- Colour transient improvement for colour difference signals (R-Y) and (B-Y) with transient detecting-, storage- and switching stages resulting in high transients of colour difference output signals
- A luminance signal path (Y) which substitutes the conventional Y-delay coil with an integrated Y-delay line
- Switchable delay time from 730 ns to 1000 ns in steps of 90 ns and additional fine adjustment of 50 ns
- Two Y output signals; one of 180 ns less delay

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 10)		V_P	10.8	12	13.2	V
Supply current (pin 10)		I_P	–	35	50	mA
Y-signal delay at pin 12	S1 open; $R_{14\text{-}18}$ = 1.2 kΩ*					
$V_{15\text{-}18}$ = 0 to 2.5 V		$t_{17\text{-}12}$	670	730	790	ns
$V_{15\text{-}18}$ = 3.5 to 5.5 V		$t_{17\text{-}12}$	760	820	880	ns
$V_{15\text{-}18}$ = 6.5 to 8.5 V		$t_{17\text{-}12}$	850	910	970	ns
$V_{15\text{-}18}$ = 9.5 to 12 V		$t_{17\text{-}12}$	940	1000	1060	ns
Y-signal attenuation	0.5 MHz	α_Y	0	6.5	8.0	dB
(R-Y) and (B-Y) signal attenuation		α_{cd}	−1	0	+1	dB
output transient time		t_{tr}	–	100	200	ns

* Delay time is proportional to resistor $R_{14\text{-}18}$.
$R_{14\text{-}18}$ also influences the bandwidth; a value of 1.2 kΩ results in a bandwidth of 5 MHz (typ.).

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

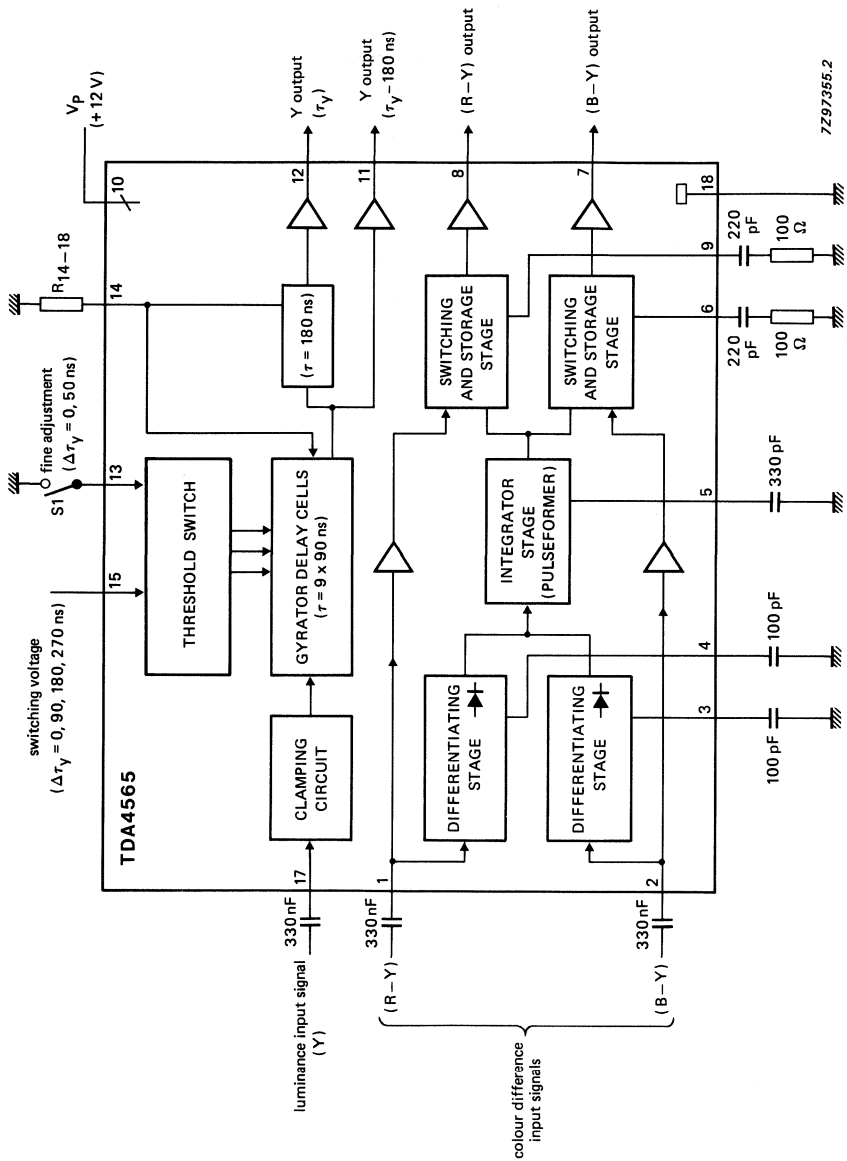


Fig.1 Block diagram.

DEVELOPMENT DATA

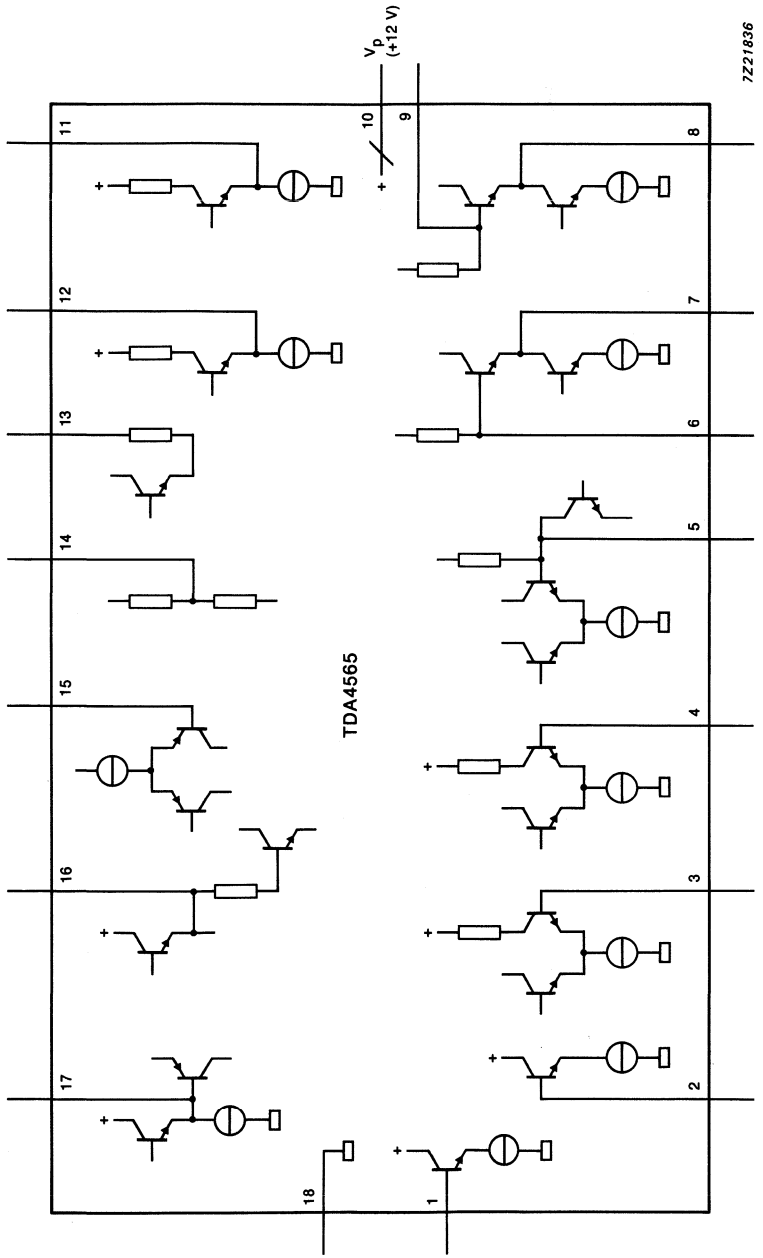


Fig.2 Internal pin circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 10)	$V_p = V_{10\text{-}18}$	0	13.2	V
Voltage ranges to pin 18 (ground)				
at pins 1, 2, 12 and 15	$V_{n\text{-}18}$	0	V_p	V
at pin 11	$V_{11\text{-}18}$	0	(V_p −3 V)	V
at pin 17	$V_{17\text{-}18}$	0	7	V
Voltage ranges				
at pin 7 to pin 6	$V_{7\text{-}6}$	0	5	V
at pin 8 to pin 9	$V_{8\text{-}9}$	0	5	V
Currents				
at pins 6, 9	$I_{6,\,9}$	−10	+10	mA
at pins 7, 8, 11 and 12	$I_{7,\,8,\,11,\,12}$	internally limited		
Total power dissipation (T_j = 150 °C; T_{amb} = 70 °C)	P_{tot}	–	1.1	W
Storage temperature range	T_{stg}	−25	+150	°C
Operating ambient temperature range	T_{amb}	0	+70	°C

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j\text{-}a}$ = 70 K/W

Note

Pins 3, 4, 5, 6, 9, 13 and 14 DC potential not published.

CHARACTERISTICS

$V_p = V_{10-18} = 12$ V; $T_{amb} = 25$ °C; measured in application circuit Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply (pin 10)						
Supply voltage		V_p	10.8	12	13.2	V
Supply current		I_p	–	35	50	mA
Colour difference paths						
(R-Y) input voltage (75% colour bar signal) (peak-to-peak value)		$V_{1(p-p)}$	–	1.05	1.5	V
(B-Y) input voltage (75% colour bar signal) (peak-to-peak value)		$V_{2(p-p)}$	–	1.33	1.9	V
Input resistance						
(R-Y)		R_{1-18}	8	12	16	kΩ
(B-Y)		R_{2-18}	8	12	16	kΩ
Internal bias voltage						
(R-Y)		V_{1-18}	3.8	4.3	4.8	V
(B-Y)		V_{1-18}	3.8	4.3	4.8	V
Signal attenuation						
(R-Y)		V_8/V_1	−1	0	+1	dB
(B-Y)		V_7/V_2	−1	0	+1	dB
Output transient time	note 1	t_{tr}	–	100	200	ns
Output resistance						
(B-Y)		R_{7-18}	–	100	–	Ω
(R-Y)		R_{8-18}	–	100	–	Ω
DC output voltage						
(B-Y)		V_{7-18}	3.8	4.3	4.8	V
(R-Y)		V_{8-18}	3.8	4.3	4.8	V
Output current	note 2					
source		$I_{7,8}$	0.4	–	–	mA
sink		$-I_{7,8}$	1.0	–	–	mA

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Y-signal path						
Y-input voltage (composite signal) (peak-to-peak value)	capacitive coupling	$V_{17(p\text{-}p)}$	–	1	1.4	V
Internal bias voltage	during clamping	$V_{17\text{-}18}$	1.3	1.5	1.7	V
Input current						
during picture content		I_{17}	–	8	12	μA
during sync. pulse		$-I_{17}$	–	100	150	μA
Y-signal delay at pin 12	S1 open; R_{14} = 1.2 kΩ; notes 3 and 4)					
at $V_{15\text{-}18}$ = 0 to 2.5 V		$t_{17\text{-}18}$	670	730	790	ns
at $V_{15\text{-}18}$ = 3.5 to 5.5 V		$t_{17\text{-}18}$	760	820	880	ns
at $V_{15\text{-}18}$ = 6.5 to 8.5 V		$t_{17\text{-}18}$	850	910	970	ns
at $V_{15\text{-}18}$ = 9.5 to 12 V		$t_{17\text{-}18}$	940	1000	1060	ns
Fine adjustment of Y-signal delay for all 4 steps	S1 closed	$t_{17\text{-}12}$	30	50	70	ns
Signal delay between pin 11 and pin 12	S1 open	$t_{11\text{-}12}$	160	180	200	ns
Dependency of delay time						
on temperature		$\frac{\Delta t_{17\text{-}12}}{t_{17\text{-}12}.\Delta T_j}$	–	0.001	–	K^{-1}
on supply voltage		$\frac{\Delta t_{17\text{-}12}}{t_{17\text{-}12}.\Delta V_p}$	–	–0.03	–	V^{-1}
Input switching current		$-I_{15}$	–	15	25	μA
Y-signal attenuation	f = 0.5 MHz					
pin 11 from pin 17		V_{11}/V_{17}	5.0	6.5	8.0	dB
pin 12 from pin 17		V_{12}/V_{17}	5.0	6.5	8.0	dB
Frequency response at 3 MHz referred to 0.5 MHz	note 5					
pin 11		$\frac{V_{11}\ (3\ MHz)}{V_{11}\ (0.5\ MHz)}$	0	–	3.0	dB
pin 12		$\frac{V_{12}\ (3\ MHz)}{V_{12}\ (0.5\ MHz)}$	0	–	3.0	dB
Frequency response at 5 MHz referred to 0.5 MHz	note 5					
pin 11		$\frac{V_{11}\ (5\ MHz)}{V_{11}\ (0.5\ MHz)}$	–3.0	–	2.0	dB
pin 12		$\frac{V_{12}\ (5\ MHz}{V_{12}\ (0.5\ MHz)}$	–3.0	–	2.0	dB

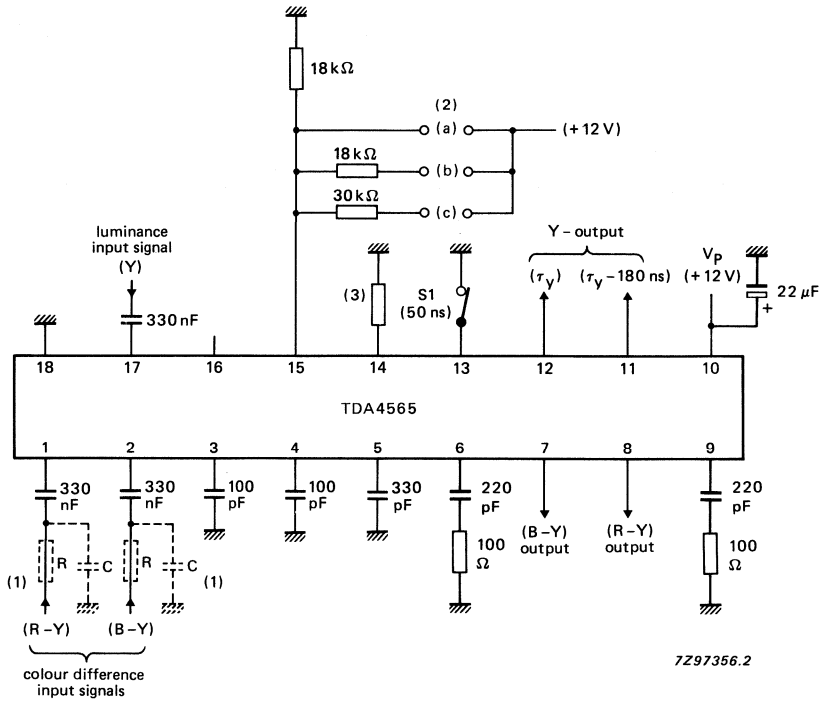
parameter	conditions	symbol	min.	typ.	max.	unit
DC output voltage						
pin 11		$V_{11\text{-}18}$	1.8	2.3	2.6	V
pin 12		$V_{12\text{-}18}$	9.8	10.3	10.8	V
Output current	note 2					
source		$I_{11, 12}$	–	–	0.4	mA
sink		$-I_{11, 12}$	–	–	1.0	mA

Notes to the characteristics

1. Output signal transient time measured with $C_{6\text{-}18} = C_{9\text{-}18} = 220$ pF without resistor (see Fig.3).
2. Output current measured with emitter follower with constant current source of 0.6 mA.
3. $R_{14\text{-}18}$ influences the bandwidth; a value of 1.2 kΩ results in a bandwidth of 5 MHz (typ.).
4. Delay time is proportional to resistor $R_{14\text{-}18}$. Devices with suffix "A" require the value of the resistor to be 1.15 kΩ; a 27 kΩ resistor connected in parallel with $R_{14\text{-}18} = 1.2$ kΩ.
5. Frequency response measured with $V_{15\text{-}18} = 9.5$ V and switch S1 open.

DEVELOPMENT DATA

APPLICATION INFORMATION



(1) Residual carrier reduced to 20 mV peak-to-peak (R = 1 kΩ, C = 100 pF).
(2) Switching sequence for delay times shown in Table 1.
(3) $R_{14\text{-}18}$ = 1.2 kΩ for TDA4565
$R_{14\text{-}18}$ = 1.15 kΩ for TDA4565A (27 kΩ resistor connected in parallel to 1.2 kΩ).

Fig.3 Application diagram and test circuit.

Table 1 Switching sequence for delay times.

connection			voltage at pin 15	delay time (ns)*
(a)	(b)	(c)		
0	0	0	0 to 2.5 V	730
0	0	X	3.5 to 5.5 V	820
0	X	X	6.5 to 8.5 V	910
X	X	X	9.5 to 12 V	1000

Where: X = connection closed; 0 = connection open.

* When switch (S1) is closed the delay time is increased by 50 ns.

COLOUR TRANSIENT IMPROVEMENT CIRCUIT

GENERAL DESCRIPTION

The TDA4566 is a monolithic integrated circuit for colour transient improvement (CTI) and luminance delay line in gyrator technique in colour television receivers.

Features

- Colour transient improvement for colour difference signals (R-Y) and (B-Y) with transient detecting-, storage- and switching stages resulting in high transients of colour difference output signals
- A luminance signal path (Y) which substitutes the conventional Y-delay coil with an integrated Y-delay line
- Switchable delay time from 550 ns to 820 ns in steps of 90 ns and additional fine adjustment of 37 ns
- Two Y output signals; one of 180 ns less delay

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 10)		V_P	10.8	12	13.2	V
Supply current (pin 10)		I_P	–	35	50	mA
Y-signal delay at pin 12	S1 open; $R_{14\text{-}18}$ = 1.2 kΩ*					
$V_{15\text{-}18}$ = 0 to 2.5 V		$t_{17\text{-}12}$	490	550	610	ns
$V_{15\text{-}18}$ = 3.5 to 5.5 V		$t_{17\text{-}12}$	580	640	700	ns
$V_{15\text{-}18}$ = 6.5 to 8.5 V		$t_{17\text{-}12}$	670	730	790	ns
$V_{15\text{-}18}$ = 9.5 to 12 V		$t_{17\text{-}12}$	760	820	880	ns
Y-signal amplification	0.5 MHz	α_Y	0	1	2	dB
(R-Y) and (B-Y) signal attenuation		α_{cd}	−1	0	+ 1	dB
output transient time		t_{tr}	–	100	200	ns

* Delay time is proportional to resistor $R_{14\text{-}18}$.
$R_{14\text{-}18}$ also influences the bandwidth; a value of 1.2 kΩ results in a bandwidth of 5 MHz (typ.).

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

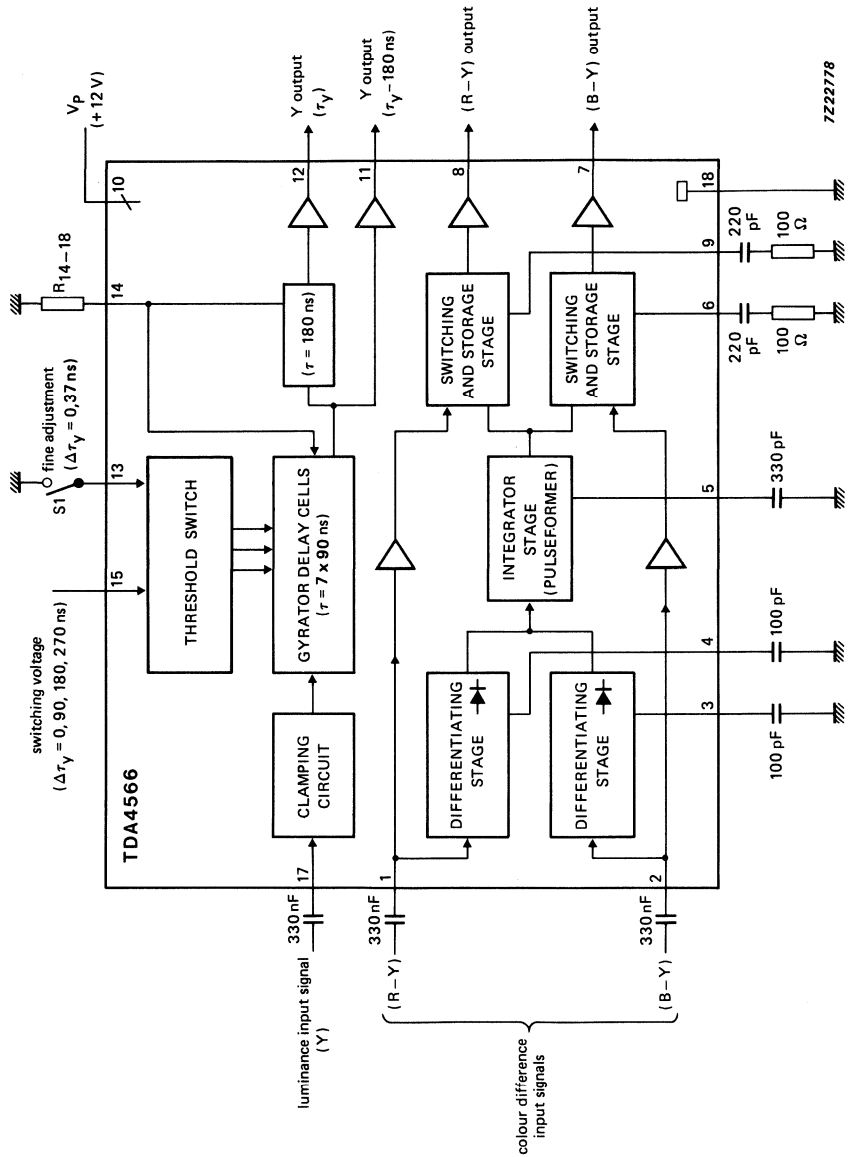


Fig.1 Block diagram.

DEVELOPMENT DATA

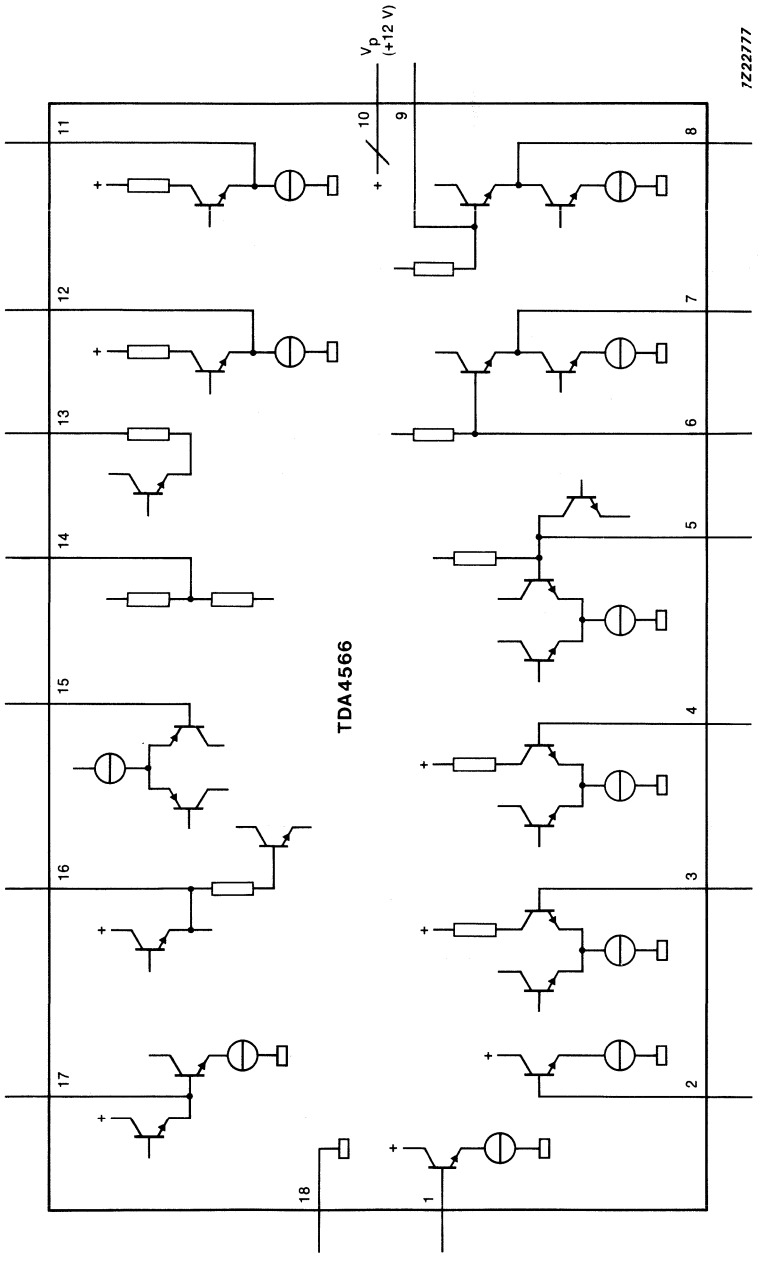


Fig.2 Internal pin circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 10)	$V_P = V_{10\text{-}18}$	0	13.2	V
Voltage ranges to pin 18 (ground)				
at pins 1, 2, 12 and 15	$V_{n\text{-}18}$	0	V_P	V
at pin 11	$V_{11\text{-}18}$	0	(V_P–3 V)	V
at pin 17	$V_{17\text{-}18}$	0	7	V
Voltage ranges				
at pin 7 to pin 6	$V_{7\text{-}6}$	0	5	V
at pin 8 to pin 9	$V_{8\text{-}9}$	0	5	V
Currents				
at pins 6, 9	$I_{6,9}$	–10	+ 10	mA
at pins 7, 8, 11 and 12	$I_{7,8,11,12}$		internally limited	
Total power dissipation (T_j = 150 °C; T_{amb} = 70 °C)	P_{tot}	–	1.1	W
Storage temperature range	T_{stg}	–25	+ 150	°C
Operating ambient temperature range	T_{amb}	0	+ 70	°C

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j\text{-}a}$ = 70 K/W

Note

Pins 3, 4, 5, 6, 9, 13 and 14 DC potential not published.

CHARACTERISTICS

$V_P = V_{10-18} = 12$ V; $T_{amb} = 25$ °C; measured in application circuit Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply (pin 10)						
Supply voltage		V_P	10.8	12	13.2	V
Supply current		I_P	–	35	50	mA
Colour difference paths						
(R-Y) input voltage (75% colour bar signal) (peak-to-peak value)		$V_{1(p-p)}$	–	0.63	1.5	V
(B-Y) input voltage (75% colour bar signal) (peak-to-peak value)		$V_{2(p-p)}$	–	0.8	1.9	V
Input resistance						
(R-Y)		R_{1-18}	8	12	16	kΩ
(B-Y)		R_{2-18}	8	12	16	kΩ
Internal bias voltage						
(R-Y)		V_{1-18}	3.8	4.3	4.8	V
(B-Y)		V_{1-18}	3.8	4.3	4.8	V
Signal attenuation						
(R-Y)		V_8/V_1	−1	0	+ 1	dB
(B-Y)		V_7/V_2	−1	0	+ 1	dB
Output transient time	note 1	t_{tr}	–	100	200	ns
Output resistance						
(B-Y)		R_{7-18}	–	100	–	Ω
(R-Y)		R_{8-18}	–	100	–	Ω
DC output voltage						
(B-Y)		V_{7-18}	3.8	4.3	4.8	V
(R-Y)		V_{8-18}	3.8	4.3	4.8	V
Output current	note 2					
source		$I_{7,8}$	0.4	–	–	mA
sink		$-I_{7,8}$	1.0	–	–	mA

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Y-signal path						
Y-input voltage (composite signal) (peak-to-peak value)	capacitive coupling	$V_{17(p\text{-}p)}$	–	0.45	0.62	V
Internal bias voltage	during clamping	$V_{17\text{-}18}$	2.1	2.4	2.7	V
Input current						
during picture content		I_{17}	–	8	12	μA
during sync. pulse		$-I_{17}$	–	100	150	μA
Y-signal delay at pin 12	S1 open; R_{14} = 1.2 kΩ; notes 3 and 4					
at $V_{15\text{-}18}$ = 0 to 2.5 V		$t_{17\text{-}18}$	490	550	610	ns
at $V_{15\text{-}18}$ = 3.5 to 5.5 V		$t_{17\text{-}18}$	580	640	700	ns
at $V_{15\text{-}18}$ = 6.5 to 8.5 V		$t_{17\text{-}18}$	670	730	790	ns
at $V_{15\text{-}18}$ = 9.5 to 12 V		$t_{17\text{-}18}$	760	820	880	ns
Fine adjustment of Y-signal delay for all 4 steps	S1 closed	$t_{17\text{-}12}$	–	37	–	ns
Signal delay between pin 11 and pin 12	S1 open	$t_{11\text{-}12}$	160	180	200	ns
Dependency of delay time						
on temperature		$\frac{\Delta t_{17\text{-}12}}{t_{17\text{-}12} \cdot \Delta T_j}$	–	0.001	–	K^{-1}
on supply voltage		$\frac{\Delta t_{17\text{-}12}}{t_{17\text{-}12} \cdot \Delta V_P}$	–	–0.03	–	V^{-1}
Input switching current		$-I_{15}$	–	15	25	μA
Y-signal attenuation	f = 0.5 MHz					
pin 11 from pin 17		V_{11}/V_{17}	–1	0	+ 1	dB
pin 12 from pin 17		V_{12}/V_{17}	0	+ 1	+ 2	dB
Frequency response at 3 MHz referred to 0.5 MHz	note 5					
pin 11		$\frac{V_{11}\ (3\ MHz)}{V_{11}\ (0.5\ MHz)}$	0	–	3.0	dB
pin 12		$\frac{V_{12}\ (3\ MHz)}{V_{12}\ (0.5\ MHz)}$	0	–	3.0	dB

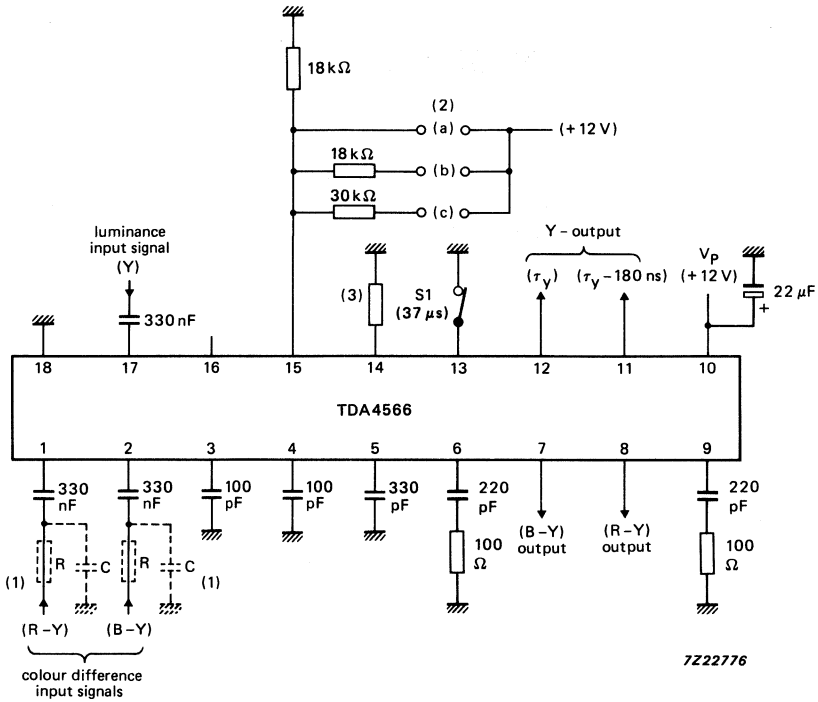
parameter	conditions	symbol	min.	typ.	max.	unit
Frequency response at 5 MHz referred to 0.5 MHz	note 5					
pin 11		$\frac{V_{11}\ (5\ MHz)}{V_{11}\ (0.5\ MHz)}$	−3.0	–	2.0	dB
pin 12		$\frac{V_{12}\ (5\ MHz)}{V_{12}\ (0.5\ MHz)}$	−3.0	–	2.0	dB
DC output voltage						
pin 11		$V_{11\text{-}18}$	1.8	2.3	2.6	V
pin 12		$V_{12\text{-}18}$	9.8	10.3	10.8	V
Output current	note 2					
source		$I_{11,\ 12}$	–	–	0.4	mA
sink		$-I_{11,\ 12}$	–	–	1.0	mA

Notes to the characteristics

1. Output signal transient time measured with $C_{6\text{-}18} = C_{9\text{-}18} = 220$ pF without resistor (see Fig.3).
2. Output current measured with emitter follower with constant current source of 0.6 mA.
3. $R_{14\text{-}18}$ influences the bandwidth; a value of 1.2 kΩ results in a bandwidth of 5 MHz (typ.).
4. Delay time is proportional to resistor $R_{14\text{-}18}$. Devices with suffix "A" require the value of the resistor to be 1.15 kΩ; a 27 kΩ resistor connected in parallel with $R_{14\text{-}18} = 1.2$ kΩ.
5. Frequency response measured with $V_{15\text{-}18} = 9.5$ V and switch S1 open.

DEVELOPMENT DATA

APPLICATION INFORMATION



(1) Residual carrier reduced to 20 mV peak-to-peak (R = 1 kΩ, C = 100 pF).
(2) Switching sequence for delay times shown in Table 1.
(3) $R_{14\text{-}18}$ = 1.2 kΩ for TDA4566.
$R_{14\text{-}18}$ = 1.15 kΩ for TDA4566A (27 kΩ resistor connected in parallel to 1.2 kΩ).

Fig.3 Application diagram and test circuit.

Table 1 Switching sequence for delay times.

connection			voltage at pin 15	delay time (ns)*
(a)	(b)	(c)		
0	0	0	0 to 2.5 V	550
0	0	X	3.5 to 5.5 V	640
0	X	X	6.5 to 8.5 V	730
X	X	X	9.5 to 12 V	820

Where : X = connection closed; 0 = connection open.

* When switch (S1) is closed the delay time is increased by 37 ns.

NTSC DECODER

GENERAL DESCRIPTION

The TDA4570 is an integrated 3,58 MHz or 4,43 MHz NTSC decoder. It is pin sequence compatible with multi-standard decoder TDA4555 and pin compatible with the PAL decoder TDA4510.

Features:

Chrominance part

- Gain controlled amplifier with operating point control stage
- ACC (automatic chrominance control) with sampled rectification during burst-key signal
- Blanking circuit for the colour burst signal

Oscillator and control voltage part

- Voltage controlled reference oscillator for double subcarrier frequency
- Divider stages which provide the correct 90^{o} phase between −(R-Y) and −(B-Y) reference signals for the demodulators
- Phase comparator which controls the frequency and phase of the reference oscillator and compares the (R-Y) reference with the burst pulse
- HUE control stage provides phase shifting via the combined service and hue control input (pin 11)
- Identification demodulator provides a positive-going identification signal at pin 14 for NTSC signals and acts as the automatic colour killer
- Two-function service switch:
  position one ($V_{14-3} < 1$ V): switches the colour-ON and switches the hue control and burst for the PLL oscillator-OFF, allowing the adjustment of the reference oscillator
  position two ($V_{14-3} > 5$ V): switches the colour-ON, the hue control OFF and allows the output signal to be observed
- Sandcastle pulse detector for burst-gate, horizontal and horizontal/vertical blanking pulse detection. The vertical part of the sandcastle pulse is used for the internal colour-ON and colour-OFF delay
- Pulse processing part for the prevention of premature switching ON of the colour. The colour-ON delay, two or three field periods after identification of the NTSC signal, is achieved by a counter. When there is no identification voltage present the colour is switched OFF immediately or, at the most, one field period later.

Demodulator part

- Two synchronous demodulators for the (R-Y) and (B-Y) signals, which incorporate stages for the blanking during line and field flyback
- Internal filtering of the residual carrier in the demodulated colour difference signals
- Colour switching stages controlled by the pulse processing part in front of the output stages
- The output stages for (R-Y) and (B-Y) signals are low resistance n-p-n emitter followers
- Separate colour switching output

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

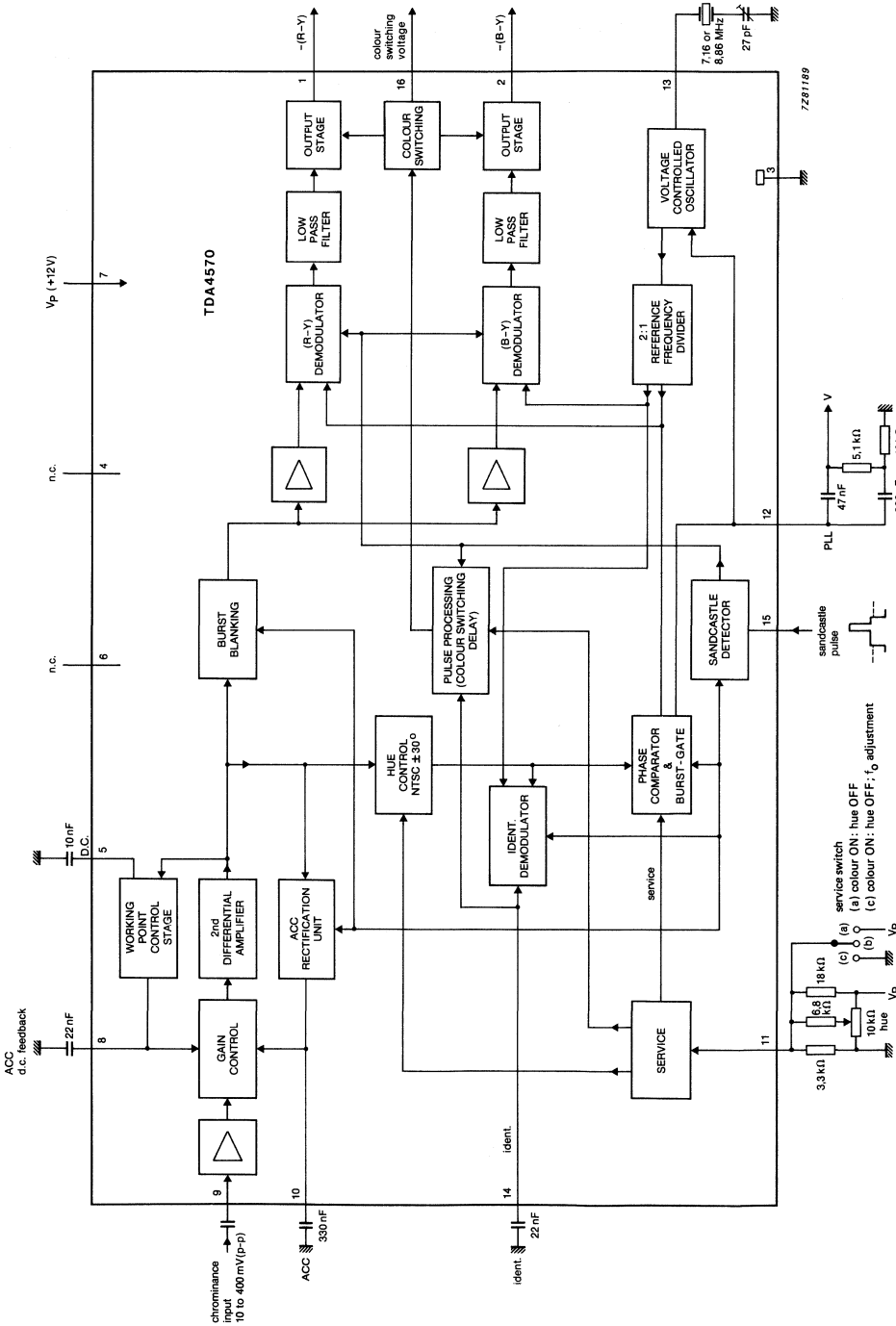


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	$V_P = V_{7-3}$	10,8 to 13,2		V
Currents at:				
pins 1 and 2	$-I_{1,2}$	max.	5	mA
pin 16	$-I_{16}$	max.	5	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature range	T_{stg}	−25 to + 150		°C
Operating ambient temperature range	T_{amb}	0 to + 70		°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	max.	80	K/W

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; measured in Fig. 2 unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply current	$I_P = I_7$	–	50	–	mA
Chrominance part					
Input voltage range (peak-to-peak value)	$V_{9-3(p-p)}$	10	–	400	mV
Nominal input voltage (peak-to-peak value) with 75% colour bar signal	$V_{9-3(p-p)}$	–	100	–	mV
Input impedance	$\lvert Z_{9-3}\rvert$	–	3,3	–	kΩ
Input capacitance	C_{9-3}	–	4,0	–	pF
Oscillator and control voltage part					
Oscillator frequency for subcarrier frequency					
3,58 MHz	f_{osc}	–	7,16	–	MHz
4,43 MHz	f_{osc}	–	8,86	–	MHz
Input resistance	R_{13-3}	–	350	–	Ω
Catching range (depending on RC network between pins 12 and 3)	Δf	± 300	–	–	Hz
Control voltage					
without burst signal	V_{14-3}	–	6,0	–	V
colour switching threshold	V_{14-3}	–	6,6	–	V
hysteresis of colour switching	V_{14-3}	–	150	–	mV
Colour-ON delay	$t_{d\ on}$	–	–	3	*
Colour-OFF delay	$t_{d\ off}$	–	–	1	*

* Expressed as field periods.

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Colour switching output (open n-p-n emitter)					
output current	$-I_{16}$	–	–	5,0	mA
colour-ON voltage	V_{16-3}	–	6,0	–	V
colour-OFF voltage	V_{16-3}	–	0	–	V
HUE control and service switches					
Phase shift of reference carrier relative to the input signal V_{11-3} = 3 V	ϕ	–5	0	+ 5	deg
Phase shift of reference carrier relative to phase at V_{11-3} = 3 V					
V_{11-3} = 2 V	$-\phi$	30	–	–	deg
V_{11-3} = 4 V	$+\phi$	30	–	–	deg
Internal source (open pin)		–	3	–	V
First service position (PLL is inactive for oscillator adjustment, colour ON, HUE OFF)	V_{11-3}	0	–	1	V
Second service position (colour ON, HUE OFF)	V_{11-3}	5	–	V_P	V
Demodulator part					
Colour difference signals output voltage (peak-to-peak value)					
–(R-Y) signal	$V_{1-3(p-p)}$	0,84	1,05	1,32	V
–(B-Y) signal	$V_{2-3(p-p)}$	1,06	1,33	1,67	V
Ratio of colour difference output signals (R-Y)/(B-Y)	$\frac{V_{1-3}}{V_{2-3}}$	0,71	0,79	0,87	
D.C. voltage at colour difference outputs	$V_{1,\,2-3}$	–	7,7	–	V
Residual carrier at colour difference outputs (peak-to-peak value)					
(1 x subcarrier frequency)	$V_{1,\,2-3(p-p)}$	–	–	20	mV
(2 x subcarrier frequency)	$V_{1,\,2-3(p-p)}$	–	–	30	mV

parameter	symbol	min.	typ.	max.	unit
Sandcastle pulse detector (note 1)					
Input voltage level (pin 15) to separate vertical and horizontal blanking pulses	V_{15-3}	1,3	1,6	1,9	V
required pulse amplitude	V_{15-3}	2,0	2,5	3,0	V
to separate horizontal blanking pulse	V_{15-3}	3,3	3,6	3,9	V
required pulse amplitude	V_{15-3}	4,1	4,5	4,9	V
to separate burst gating pulse	V_{15-3}	6,6	7,1	7,6	V
required pulse amplitude	V_{15-3}	7,7	–	–	V
Input voltage during horizontal scanning	V_{15-3}	–	–	1,1	V
Input current	$-I_{15}$	–	–	100	μA

Note

1. The sandcastle pulse is compared with three internal threshold levels, which are proportional to the supply voltage.

DEVELOPMENT DATA

APPLICATION INFORMATION

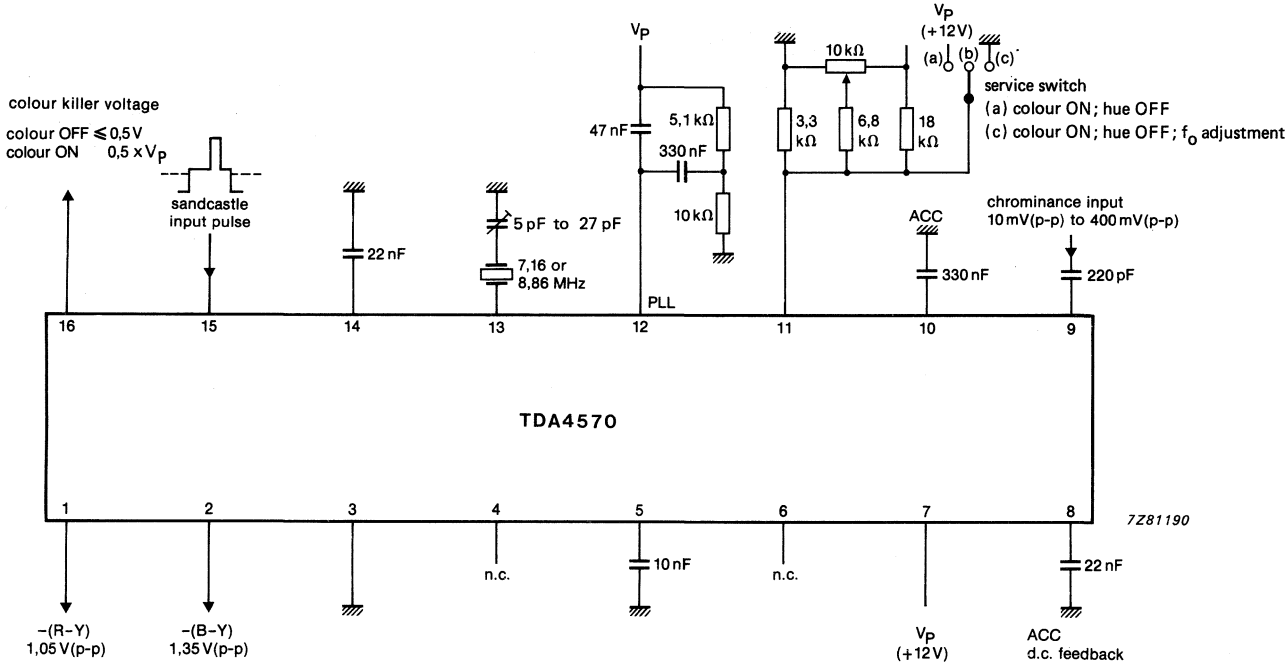


Fig. 2 Application diagram.

Crystal frequency 7, 16 or 8,86 MHz; resonance resistance 60 Ω; load capacitance 20 pF; dynamic capacitance 22 fF and static capacitance 5,5 pF.

VIDEO CONTROL COMBINATION CIRCUIT

with automatic cut-off control

GENERAL DESCRIPTION

The TDA4580 is a monolithic integrated circuit which performs video control functions in television receivers with a colour difference interface. For example it operates in conjunction the multistandard colour decoder TDA4555. The required input signals are: luminance and negative colour difference −(R-Y) and −(B-Y), and a 3-level sandcastle pulse for control purposes. Analogue RGB signals can be inserted from two sources. One with full performance adjustment possibilities. RGB output signals are available for driving the video output stages. This circuit provides automatic cut-off control of the picture tube.

Features

- Capacitive coupling of the colour difference, luminance and RGB input signals with black level clamping
- Two sets of analogue RGB inputs via fast switch 1 and fast switch 2
- First RGB inputs and fast switch 1 in accordance with peritelevision connector specification
- Saturation, contrast and brightness control acting on first RGB inputs
- Brightness control acting on second RGB inputs
- Equal black levels for television and inserted signals
- Clamping, horizontal and vertical blanking, and timing of automatic cut-off, controlled by a 3-level sandcastle pulse
- Automatic cut-off control with compensation for leakage current of the picture tube
- Measuring pulses of cut-off control start immediately after end of vertical part of sandcastle pulse
- Three selectable blanking intervals for PAL, SECAM and NTSC/PAL-M
- Two switch-on delays for run-in without discolouration
- Adjustable peak drive limiter
- Average beam current limiter
- G-Y and RGB matrix coefficients selectable for PAL/SECAM and NTSC (correction for FCC primaries)
- Bandwidth 10 MHz (typ.)
- Emitter-follower outputs for driving the RGB output stages

QUICK REFERENCE DATA

Supply voltage (pin 6)	$V_P = V_{6-24}$	typ.	12 V
Supply current (pin 6)	$I_P = I_6$	typ.	110 mA
Luminance input (pin 15)			
Composite video input signal (VBS) (peak-to-peak value)	$V_{15-24(p-p)}$	typ.	0,45 V
Colour difference input signals (peak-to-peak values)			
−(B-Y)	$V_{18-24(p-p)}$	typ.	1,33 V
−(R-Y)	$V_{17-24(p-p)}$	typ.	1,05 V
Inserted RGB signals (black to white values)	$V_{14, 13, 12-24}$	typ.	0,7 V
Inserted RGB signals for teletext use (black to white values)	$V_{23, 22, 21-24}$	typ.	1 V
Three-level sandcastle pulse (required input voltage)	V_{10-24}	typ.	2,5/4,5/8,0 V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

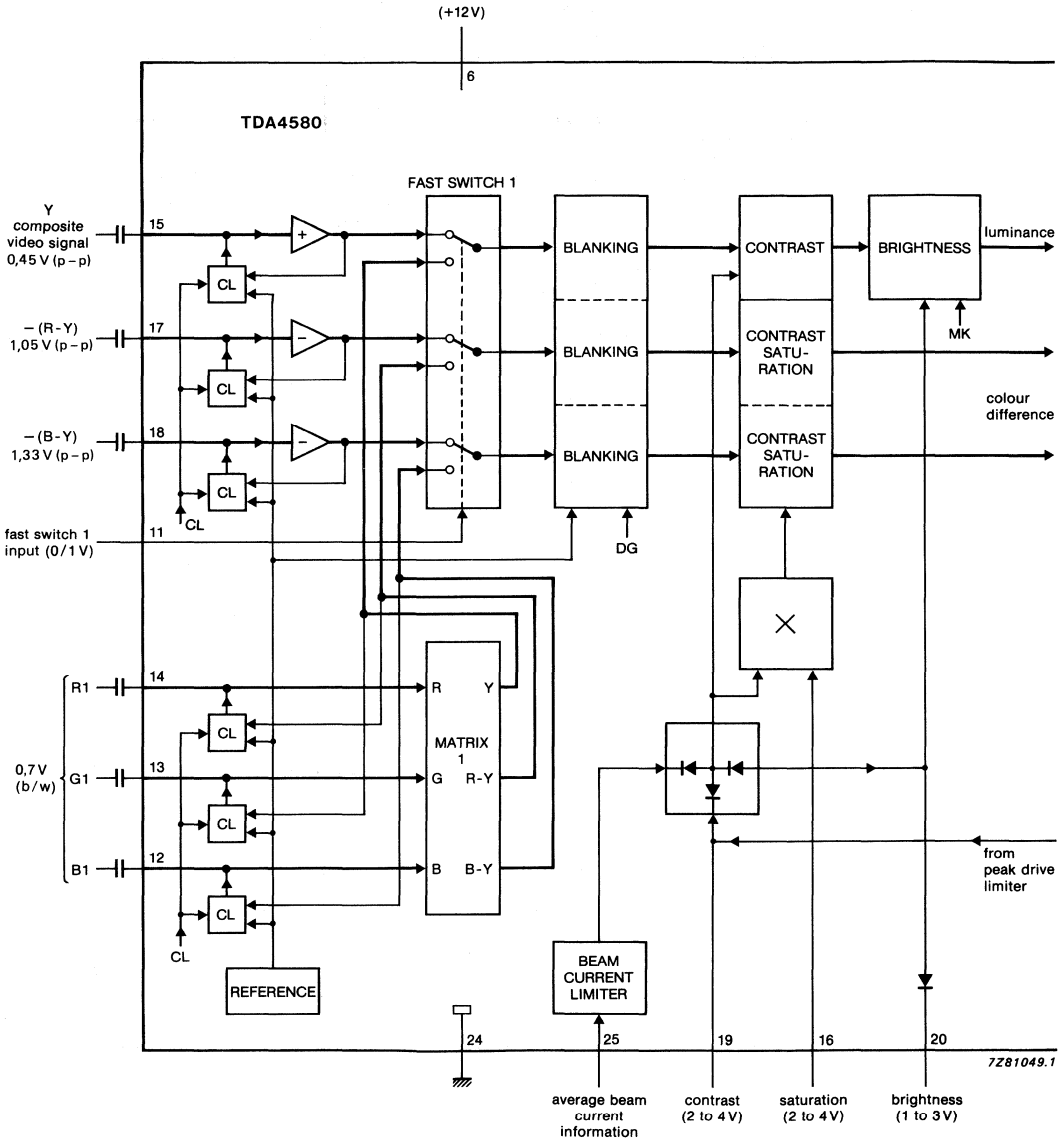


Fig. 1a Part of block diagram; continued in Fig. 1b.

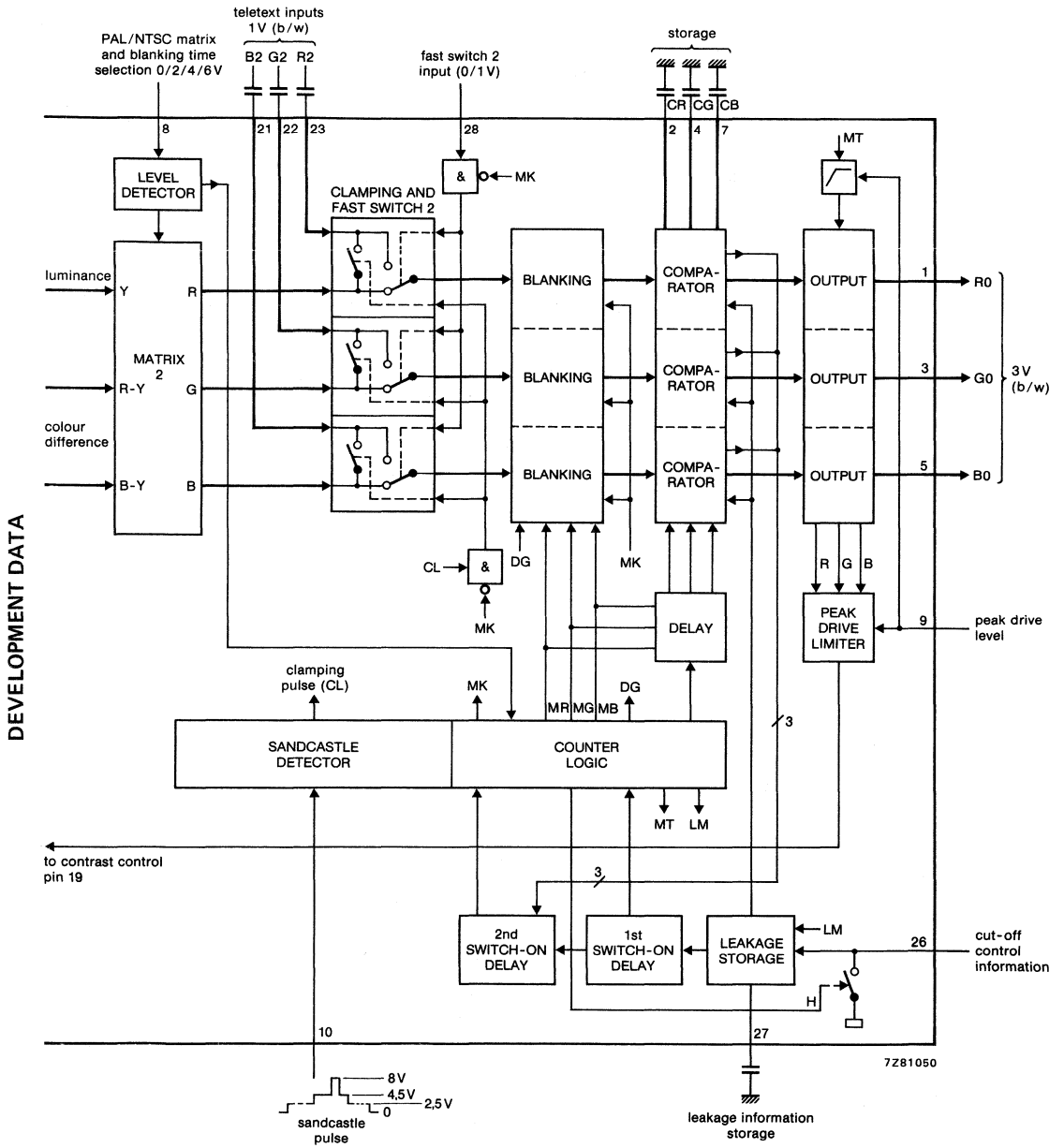


Fig. 1b Part of block diagram; continued from Fig. 1a.

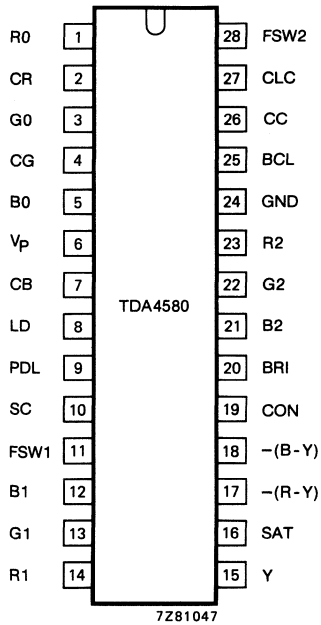


Fig. 2 Pinning diagram.

DEVELOPMENT DATA

PINNING

pin no.	mnemonic	description
1	R0	Red output
2	CR	Red storage capacitor for cut-off control
3	G0	Green output
4	CG	Green storage capacitor for cut-off control
5	B0	Blue output
6	V_P	Positive supply voltage (+ 12 V)
7	CB	Blue storage capacitor for cut-off control
8	LD	PAL/NTSC matrix and blanking time level detector input
9	PDL	Peak drive limiting input
10	SC	Sandcastle pulse input
11	FSW1	Fast switch 1 for Y, CD and RGB inputs
12	B1	Blue input (external signal)
13	G1	Green input (external signal)
14	R1	Red input (external signal)
15	Y	Luminance input
16	SAT	Saturation control input
17	−(R-Y)	Colour difference input −(R-Y)
18	−(B-Y)	Colour difference input −(B-Y)
19	CON	Contrast control input
20	BRI	Brightness control input
21	B2	Teletext blue input
22	G2	Teletext green input
23	R2	Teletext red input
24	GND	Ground
25	BCL	Average beam current limiting input
26	CC	Automatic cut-off control input
27	CLC	Storage capacitor for leakage current
28	FSW2	Fast switch 2 for teletext inputs

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 6)	$V_P = V_{6-24}$		0 to 13,2	V
Voltage range at pins 2, 4, 7, 9, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 25, 27 to pin 24 (ground)	V_{n-24}		0 to V_P	V
Voltages ranges				
at pins 8, 11, 28	$V_{8, 11, 28-24}$		−0,5 to V_P	V
at pin 10	V_{10-24}		0 to V_P + 0,7	V
at pin 26	V_{26-24}		−0,7 to V_P + 0,7	V
Currents				
at pins 1, 3, 5 (average)	$-I_{1, 3, 5(AV)}$	max.	3	mA
at pins 1, 3, 5 (peak)	$-I_{1, 3, 5(M)}$	max.	10	mA
at pin 19 (average)	$I_{19(AV)}$	max.	5	mA
at pin 26	I_{26}	max.	1	mA
Total power dissipation	P_{tot}	max.	2	W
Storage temperature range	T_{stg}		−20 to + 150	°C
Operating ambient temperature range	T_{amb}		0 to + 70	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	37	K/W

DEVELOPMENT DATA

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; measured in a circuit similar to Fig. 4 at nominal settings (saturation, contrast, brightness), no beam current or peak drive limiting; all voltages with respect to pin 24 (ground) unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply (pin 6)					
Supply voltage range	$V_P = V_{6-24}$	10,8	–	13,2	V
Supply current	$I_P = I_6$	–	110	–	mA
Colour difference inputs (pins 17 and 18)					
–(R-Y) input signal at pin 17 (notes 1 and 2) (peak-to-peak value)	$V_{17-24(p-p)}$	–	1,05	–	V
–(B-Y) input signal at pin 18 (notes 1 and 2) (peak-to-peak value)	$V_{18-24(p-p)}$	–	1,33	–	V
Input current during scanning	$\|I_{17, 18}\|$	–	–	0,3	μA
Input resistance	$R_{17, 18}$	5	–	–	MΩ
Internal d.c. bias voltage during clamping time	$V_{17, 18-24}$	–	7,5	–	V
Luminance input (pin 15; note 2)					
Composite video input signal (VBS) (peak-to-peak value)	$V_{15-24(p-p)}$	–	0,45	–	V
Input current during scanning	$\|I_{15}\|$	–	–	0,3	μA
Input resistance	R_{15}	5	–	–	MΩ
Internal d.c. bias voltage during clamping time	V_{15-24}	–	7,4	–	V
Signal switch 1 input (pin 11)					
Input voltage level for insertion of Y and CD signals	V_{11-24}	–	–	0,4	V
RGB1 signals	V_{11-24}	0,9	–	3,0	V
Internal resistor to ground	R_{11}	–	10	–	kΩ
RGB1 inputs (R1 pin 14, G1 pin 13, B1 pin 12; note 2) (signals controlled by saturation, contrast and brightness)					
Input signal (black to white value)	$V_{12, 13, 14-24}$	–	0,7	–	V
Input current during scanning	$\|I_{12, 13, 14}\|$	–	–	0,3	μA
Input resistance	$R_{12, 13, 14}$	5	–	–	MΩ
Internal d.c. bias voltage during clamping time	$V_{12, 13, 14-24}$	–	8,2	–	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
RGB/Y, (R-Y), (B-Y) – Matrix					
Matrixed according to the equations $V_{(R-Y)} = 0{,}7\ V_R - 0{,}59\ V_G - 0{,}11\ V_B$ $V_{(B-Y)} = -0{,}3\ V_R - 0{,}59\ V_G + 0{,}89\ V_B$ $V_{(Y)} = 0{,}3\ V_R + 0{,}59\ V_G + 0{,}11\ V_B$					
Contrast control input (pin 19; note 3) (contrast control acts on Y and CD signals or RGB1 signals respectively)					
Maximum contrast	$V_{19\text{-}24}$	–	4	–	V
Nominal contrast (6 dB below max.)	$V_{19\text{-}24}$	–	3	–	V
Attenuation of contrast at $V_{19\text{-}24}$ = 2 V (related to max.)		–	22	–	dB
Input current at $V_{19\text{-}24}$ = 2 to 4 V	$-I_{19}$	–	–	3	μA
Peak drive limiting input (pin 9; note 4)					
Internal d.c. bias voltage	$V_{9\text{-}24}$	–	9	–	V
Input resistance at $V_{9\text{-}24} > 9$ V	R_9	–	10	–	kΩ
Control current into contrast input (pin 19) during peak drive $V_{1,\ 2\ \text{or}\ 3\text{-}24} > V_{9\text{-}24}$	I_{19}	–	20	–	mA
Average beam current limiting input (pin 25; note 5)					
Start of contrast reduction at maximum contrast setting	$V_{25\text{-}24}$	–	8,5	–	V
Input range for full contrast reduction	$\Delta V_{25\text{-}24}$	–	1,0	–	V
Input resistance at $V_{25\text{-}24} < 6$ V	R_{25}	–	2,2	–	kΩ
Saturation control input (pin 16) (saturation control acts on CD signals or RGB1 signals respectively)					
Maximum saturation	$V_{16\text{-}24}$	–	4	–	V
Nominal saturation (6 dB below max.)	$V_{16\text{-}24}$	–	3	–	V
Attenuation of saturation at $V_{16\text{-}24}$ = 1,8 V (related to max. at 100 kHz)		50	–	–	dB
Input current at $V_{16\text{-}24}$ = 1,8 to 4 V	I_{16}	–	–	10	μA

parameter	symbol	min.	typ.	max.	unit
Brightness control input (pin 20; note 6 and 7)					
Control voltage range	V_{20-24}	1	–	3	V
Input current at V_{20-24} = 1 to 3 V	$-I_{20}$	–	–	10	μA
Control voltage for nominal brightness	V_{20-24}	–	2,2	–	V
Change of black level in the control range related to the nominal output signal (black/white) for ΔV_{20-24} = 1 V		–	33	–	%
Signal switched off and black level equal to cut-off measuring level at	V_{20-24}	11,5	–	–	V
Y, (R-Y), (B-Y)/RGB – Matrix (note 8)					
PAL matrix ($V_{8-24} = < 4,5$ V)					
Matrixed according to the equation $V_{(G-Y)} = -0,51\ V_{(R-Y)} - 0,19\ V_{(B-Y)}$					
NTSC matrix ($V_{8-24} = > 5,5$ V)					
(Adaption for NTSC-FCC primaries, nominal hue control set on -5^{o})					
Matrixed according to the equation $V_{(G-Y)}^{*} = -0,43\ V_{(R-Y)} - 0,11\ V_{(B-Y)}$					
$V_{(R-Y)}^{*} = 1,57\ V_{(R-Y)} - 0,41\ V_{(B-Y)}$					
$V_{(B-Y)}^{*} = V_{(B-Y)}$					
RGB2 inputs (Teletext) (R2 pin 23, G2 pin 22, B2 pin 21; note 2)					
(RGB signals controlled by brightness control)					
Input signal for 100% output signals (black to white value)	$V_{21, 22, 23-24}$	–	1	–	V
Input current during scanning	$I_{21, 22, 23}$	–	–	0,3	μA
Input resistance	$R_{21, 22, 23}$	5	–	–	MΩ
Signal switch 2 input (pin 28)					
Input voltage level for insertion of Y, CD signals or RGB1 signals respectively RGB signals from matrix (note 9)	V_{28-24}	–	–	0,4	V
RGB2 signals (note 9)	V_{28-24}	0,9	–	3,0	V
Internal resistor to ground	R_{28-24}	–	10	–	kΩ

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Automatic cut-off control input (pin 26; note 10) (leakage current measuring time and insertion of RGB cut-off measuring lines see Fig. 5; types of ultra-black level see Fig. 3)					
Allowed maximum external D.C. bias voltage	$V_{26\text{-}24}$	5,5	–	–	V
Voltage difference between cut-off current measurement and leakage current measurement	$\Delta V_{26\text{-}24}$	–	0,5	–	V
Warm-up test pulse	$V_{1,\ 3,\ 5\text{-}24}$	–	$V_{9\text{-}24}$*	–	V
Threshold for warm-up detector	$V_{26\text{-}24}$	–	8	–	V
Storage input for leakage current (pin 27)					
Internal resistance during leakage current measuring time (current limiting at I_{27} = 0,2 mA)	R_{27}	–	400	–	Ω
Input current except during cut-off control cycle	$\lvert I_{27}\rvert$	–	–	0,5	μA
Storage inputs for automatic cut-off control (pins 2, 4, 7)					
Charge and discharge currents	$\lvert I_{2,\ 4,\ 7}\rvert$	–	0,3	–	mA
Input currents of storage inputs out of control time	$\lvert I_{2,\ 4,\ 7}\rvert$	–	–	0,1	μA
Switch input for PAL/NTSC matrix and vertical blanking time (pin 8; note 11)					
Switching voltage input for					
PAL matrix and vertical blanking period of					
25 lines	$V_{8\text{-}24}$	–	0	0,5	V
22 lines	$V_{8\text{-}24}$	1,5	2	2,5	V
18 lines	$V_{8\text{-}24}$	3,5	4	4,5	V
NTSC matrix and vertical blanking period of					
18 lines	$V_{8\text{-}24}$	5,5	6	12	V
Input current	I_8	–	–	50	μA

* Maximum 8 V.

parameter	symbol	min.	typ.	max.	unit
Sandcastle pulse detector (pin 10; note 12)					
The following amplitudes are required for separating the various pulses:					
horizontal and vertical blanking pulses	V_{10-24}	2,0	2,5	3,0	V
horizontal pulses for counter logic	V_{10-24}	4,0	4,5	5,0	V
clamping pulses	V_{10-24}	7,5	–	–	V
delay of leading edge of clamping pulse	t_d	–	1	–	μs
Input current at V_{10-24} = 0 V	$-I_{10}$	–	–	100	μA
Outputs for positive RGB signals (R0 pin 1, G0 pin 3, B0 pin 5; note 13)					
Nominal signal amplitude (black/white)	$V_{1, 3, 5-24}$	–	3	–	V
Spreads between channels		–	–	10	%
Maximum signal amplitude (black/white)	$V_{1, 3, 5-24}$	4	–	–	V
Internal current source	$I_{1, 3, 5}$	–	3	–	mA
Output resistance	$R_{1, 3, 5}$	–	160	220	Ω
Minimum output voltage	$V_{1, 3, 5-24}$	–	1	–	V
Maximum output voltage	$V_{1, 3, 5-24}$	–	10	–	V
Horizontal and vertical blanking to ultra-black level 2 related to nominal signal black level in percentage of nominal signal amplitude		45	55	–	%
Vertical blanking to ultra-black level 1 related to cut-off measuring level in percentage of nominal signal amplitude		25	35	–	%
Recommendation:					
Range for cut-off measuring level 1,5 to 5,0 V; nominal value at 3 V (note 14)					
Gain data (note 15)					
Frequency response of Y path (0 to 8 MHz) pins 1, 3 and 5 to pin 15	d	–	–	3	dB
Frequency response of CD path (0 to 8 MHz) pin 1 to pin 17 = pin 5 to pin 18	d	–	–	3	dB
Frequency response of RGB1 path (0 to 8 MHz) pin 1 to pin 14 = pin 3 to pin 13 = pin 5 to pin 12	d	–	–	3	dB
Frequency response of RGB2 path (0 to 10 MHz) pin 1 to pin 23 = pin 3 to pin 22 = pin 5 to pin 21	d	–	–	3	dB

DEVELOPMENT DATA

Notes to the characteristics

1. The value of the colour difference input signals, −(B-Y) and −(R-Y), is given for saturated colour bar with 75% of maximum amplitude.
2. Capacitive coupled to a low ohmic source; recommended value 600 Ω (max.).
3. At pin 19 for $V_{19-24} \leqslant 2{,}0$ V, no further decrease of contrast is possible.
4. The peak drive limiting of output signals is achieved by contrast reduction. The limiting level of the output signals is equal to the voltage V_{9-24}, adjustable in the range 5 to 11 V. After exceeding the adjusted limiting level at peak drive limiter will not be active during the first line.
5. The average beam current limiting acts on contrast and at minimum contrast on brightness (the external contrast voltage at pin 19 is not affected).
6. At nominal brightness the black level at the output is 0,3 V ($\hat{=}$ −10% of nominal signal amplitude) below the measuring level.
7. The internal control voltage can never be more positive than 0,7 V above the internal contrast voltage.
8. Matrix equation

   $V_{(R-Y)}$, $V_{(B-Y)}$: output of NTSC decoder of PAL type demodulating axis and amplitudes

   $V_{(G-Y)}^*$, $V_{(R-Y)}^*$, $V_{(B-Y)}^*$: for NTSC modified CD signals; equivalent to demodulation with the following axes and amplification factors:−

(B-Y)* demodulator axis	0°	
(R-Y)* demodulator axis	115°	(PAL 90°)
(R-Y)* amplification factor	1,97	(PAL 1,14)
(B-Y)* amplification factor	2,03	(PAL 2,03)

   $V_{(G-Y)}^* = -0{,}27\ V_{(R-Y)}^* - 0{,}22\ V_{(B-Y)}^*$.
9. During clamping time, in each channel the black level of the inserted signal is clamped on the black level of the internal signal behind the matrix (dependent on brightness control).
10. During warm-up time of the picture tube, the RGB outputs (pins 1, 3 and 5) are blanked to minimum output voltage. An inserted white pulse during the vertical flyback is used for beam current detection. If the beam current exceeds the threshold of the warm-up detector at pin 26, the cut-off current control starts operating, but the video signal is still blanked. After run-in of the cut-off current control loop, the video signal will be released.
    The first measuring pulse occurs in the first complete line after the end of the vertical part of the sandcastle pulse. The absolute minimum vertical part must contain 9 line-pulses. The cycle time of the counter is 63 lines. When the vertical pulse is longer than 61 lines, the IC is reset to the switch-on condition. In this event the video signal is blanked and the RGB-outputs are blanked to minimum output voltage as during warm-up time.
    During leakage current measurement, all three channels are blanked to ultra-black level 1. With the measuring level only in the controlled channel, the other two channels are blanked to ultra-black level 1. The brightness control shifts both the signal black level and the ultra-black level 2. The brightness control is disabled from line 4 to the end of the last measuring line (see Fig. 3).
    With the most adverse conditions (maximum brightness and minimum black level 2) the blanking level is located 30% of nominal signal amplitude below the cut-off measuring level.

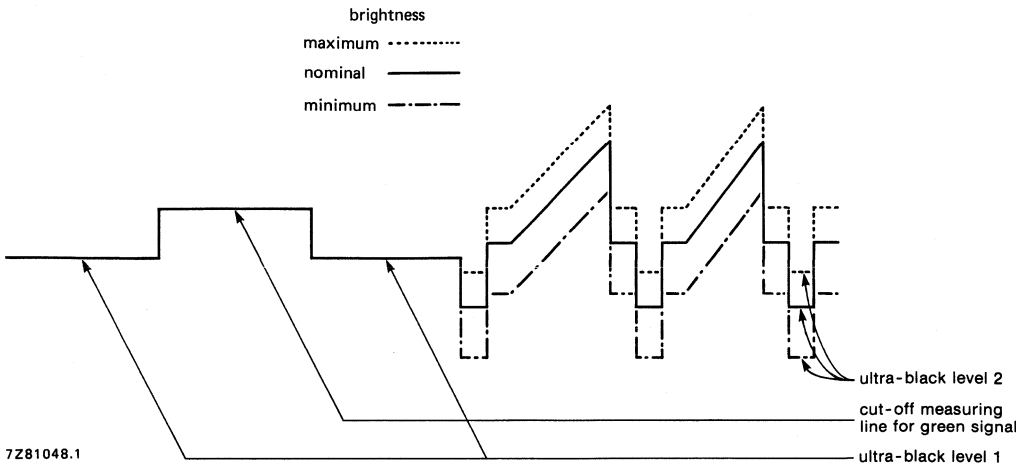
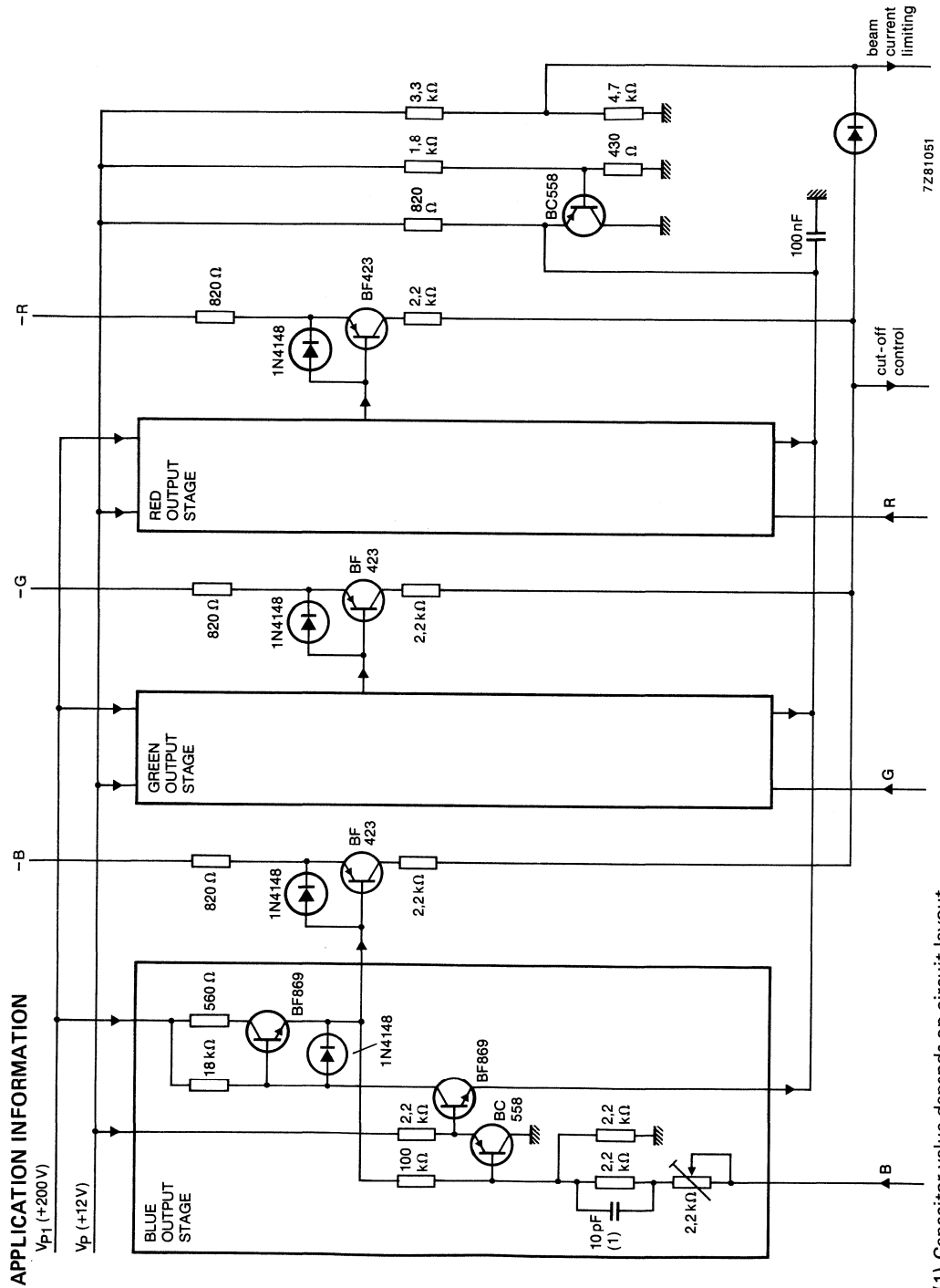


Fig. 3 Types of ultra-black levels.

DEVELOPMENT DATA

11. The given blanking times are valid for the vertical part of the sandcastle pulse of 9 to 15 lines. If the vertical part is longer and the cut-off lines are outside the vertical blanking period of 18, 22 or 25 lines respectively, the blanking of the signal ends with the end of last of the three cut-off measuring pulses as shown in Fig. 5.
12. The sandcastle pulse is compared with three internal thresholds (proportional to V_P) to separate the various pulses. The internal pulses are generated when the input pulse at pin 10 exceeds the thresholds. The thresholds are for:
    - Horizontal and vertical blanking $V_{10\text{-}24} = 1{,}5$ V
    - Horizontal pulse $V_{10\text{-}24} = 3{,}5$ V
    - Clamping pulse $V_{10\text{-}24} = 7{,}0$ V
13. The outputs at pins 1, 3 and 5 are emitter followers with current sources and emitter protection resistors.
14. The value of the cut-off control range for the positive RGB output signals is given for a nominal output signal. If the signal amplitude is reduced, the cut-off range can be increased.
15. The gain data is given for a nominal setting of the contrast and saturation controls, measured without load at the RGB outputs (pins 1, 3 and 5).



(1) Capacitor value depends on circuit layout.

Fig. 4a Part of typical application circuit diagram using the TDA4580; continued in Fig. 4b.

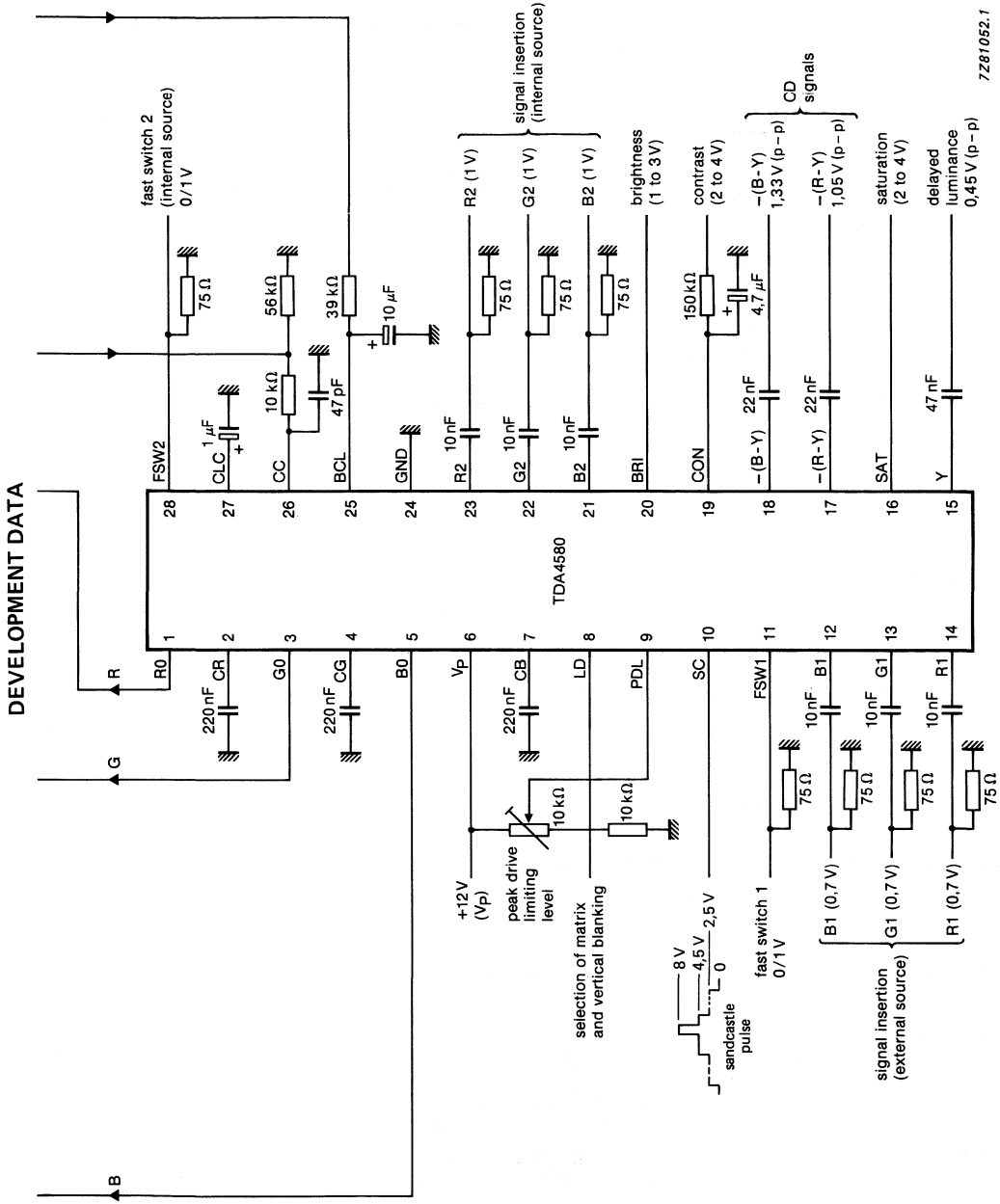
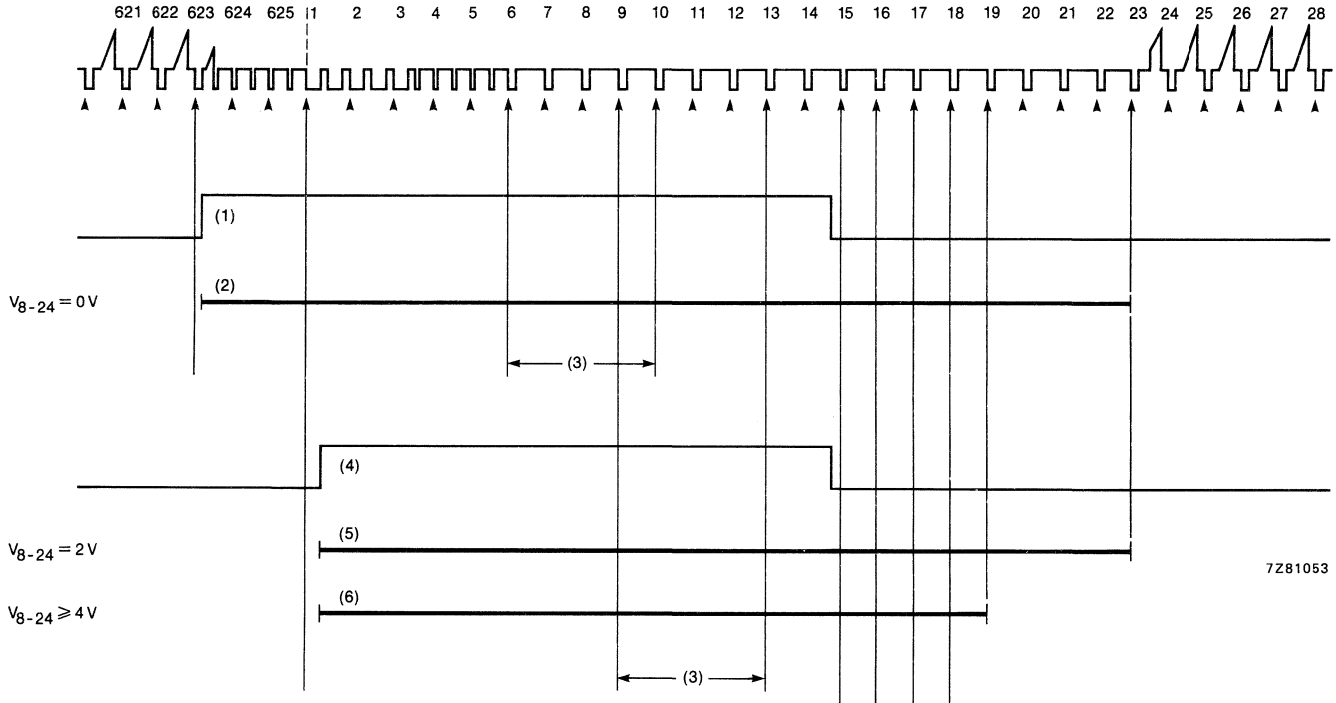


Fig. 4b Part of typical application circuit diagram using the TDA4580; continued from Fig. 4a.

APPLICATION INFORMATION (continued)



(1) vertical part of sandcastle pulse starts with equalizing pulses and ends with flyback.
(2) blanking period of 25 complete lines.
(3) leakage measuring period (LM).
(4) vertical part of sandcastle pulse starts and ends with flyback.
(5) blanking period of 22 complete lines.
(6) blanking period of 18 complete lines.
(7) cut-off measuring line for red signal (MR).
(8) cut-off measuring line for green signal (MG).
(9) cut-off measuring line for blue signal (MB).

Fig. 5 Blanking and measuring lines.

SECAM IDENTIFICATION AND CHROMINANCE CORRECTION CIRCUIT

The TDA4720T is a monolithic integrated circuit for SECAM identification and chrominance signal correction in VHS video cassette recorders (VCR). It can be applied as a stand-alone SECAM identification circuit and, when used in conjunction with TDA4710, together they provide all the functions necessary for PAL/SECAM B, G chrominance processing in VHS VCRs.

Features

- Very reliable SECAM identification by means of chrominance burst amplitude, presence of both SECAM colour carriers and line alternation of both carriers
- Two identification outputs: SECAM YES/NO
- Internal phase correction of the demodulated burst
- Internal detection and switching for SECAM long-play VCR (for 'trick' modes)
- Internal buffers and switches for correction of the line-alternating colour carriers

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 13)	V_P	4,5	5,0	5,5	V
Supply current	I_P	–	16	17	mA
Chrominance input signal to phase detector (peak-to-peak value)	$V_{14,15\text{-}4(p\text{-}p)}$	60	–	300	mV
Chrominance input signal to line correction circuit (peak-to-peak value)	$V_{5,12\text{-}4(p\text{-}p)}$	–	–	1	V
Chrominance output signal from line correction circuit (peak-to-peak value)	$V_{7\text{-}4(p\text{-}p)}$	–	–	1	V

PACKAGE OUTLINES

TDA4720: 16-lead DIL; plastic (SOT38).
TDA4720T: 16-lead mini-pack; plastic (SO16; SOT109A).

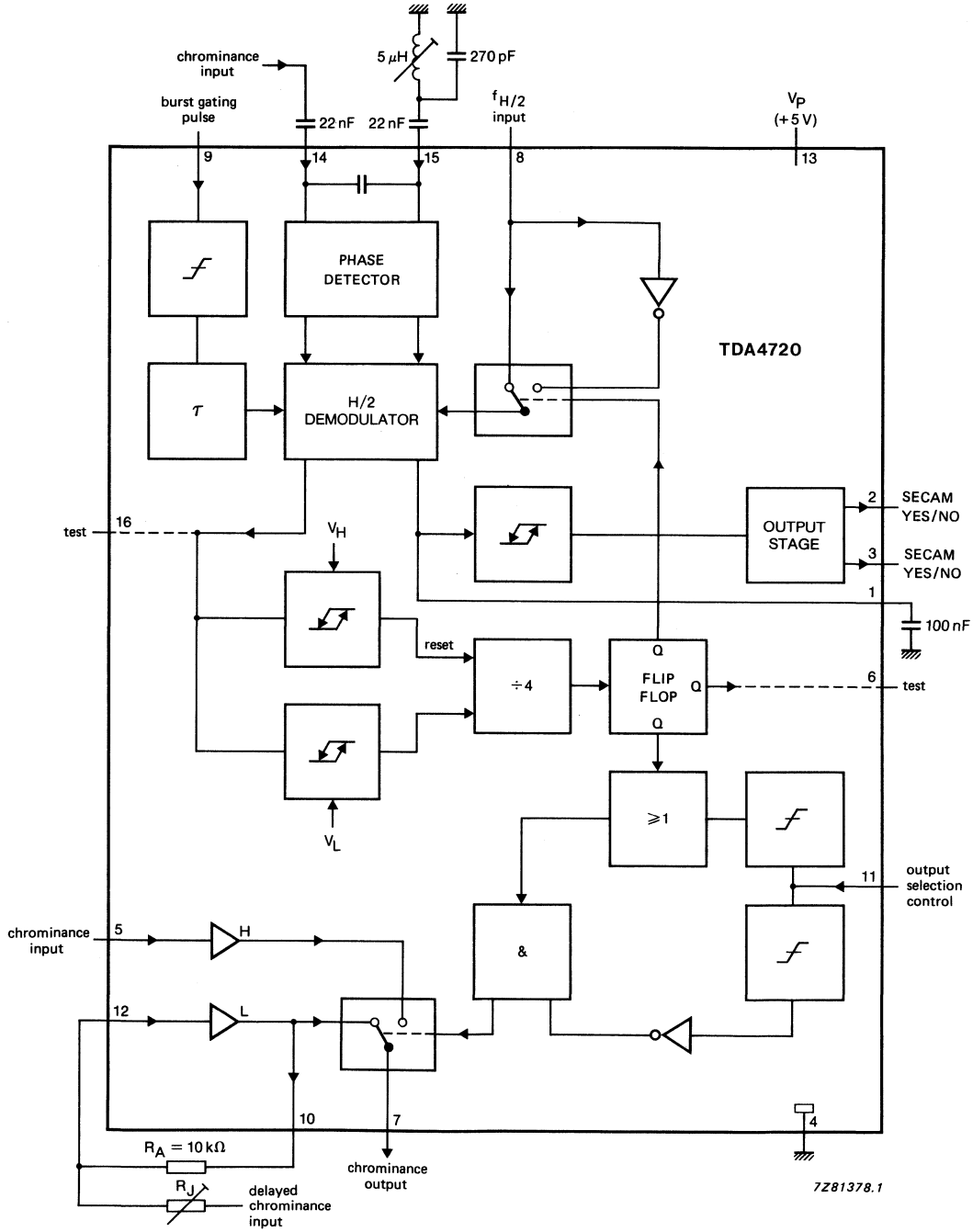


Fig. 1 Block diagram and test circuit.

DEVELOPMENT DATA

PINNING

pin. no.	function
1	Integration of demodulated bursts.
2	Buffered output; SECAM YES/NO.
3	Buffered output; SECAM YES/NO.
4	Ground.
5	Chrominance input (only if line correction of SECAM carrier is used).
6	Test pin (internal connection).
7	Chrominance output (of line-corrected SECAM; only if line correction of SECAM carrier is used).
8	$f_{H/2}$ frequency input for chrominance burst demodulation.
9	Burst gating pulse input.
10	Feedback resistor for pin 12 signal path (only if line correction of SECAM carrier is used).
11	Output selection control (selects signal path to pin 7).
12	Delayed chrominance input (delayed by 1H; only if line correction of SECAM carrier is used).
13	Positive supply voltage (V_P = + 5 V).
14,15	The LC circuit at pin 15 has to be tuned to the centre frequency between the two chrominance carriers (at pin 14). The phase detector then provides a positive or negative output voltage depending on the first or second chrominance carrier.
16	Test pin (internal connection).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 13)	$V_P = V_{13-4}$	–	6,0	V
Voltage range on pins 6, 8, 9, 11, 12, 14 and 15	V_{n-4}	0	V_P	V
Maximum current at pins 1, 2, 3, 7, 15, 16 and 18	I_n	–	2	mA
Total power dissipation	P_{tot}	–	120	mW
Storage temperature range	T_{stg}	–25	+ 150	°C
Operating ambient temperature range	T_{amb}	0	+ 70	°C

CHARACTERISTICS

$V_P = V_{13-4} = 5$ V; $T_{amb} = 25$ °C; test circuit as per Fig. 1; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage (pin 13)		V_P	4,5	5,0	5,5	V
Supply current		I_{13}	–	16	17	mA
Identification						
AC input voltage (peak-to-peak value)		$V_{14,15-4}$	60	125	300	mV
Input resistance		$R_{14,15-4}$	14	18	22	kΩ
Charge capacitor		C_{1-4}	–	100	–	nF
Forced SECAM-ON voltage		V_{1-4}	3,8	–	–	V
Forced SECAM-OFF voltage		V_{1-4}	–	–	2	V
Sensitivity of phase detector	$V_{14,15-4(p-p)}$ = 125 mV	α	–	1,6	–	V/rad.
Output voltage						
in SECAM mode		$V_{2,3-4}$	4,3	–	–	V
in non-SECAM mode		$V_{2,3-4}$	–	–	0,8	V
Output current						
in SECAM mode		$I_{2,3}$	1	–	–	mA
in non-SECAM mode		$I_{2,3}$	–	–	0,3	μA
Burst gating						
Input resistance		R_{9-4}	20	25	–	kΩ
Threshold voltage HIGH (phase detector active)		V_{9-4}	3,0	3,25	3,5	V
H/2 demodulator						
Input resistance		R_{8-4}	20	25	–	kΩ
Threshold voltage for changing conditions of H/2 demodulator		V_{8-4}	3,0	3,25	3,5	V
Chrominance correction						
Chrominance input signal (peak-to-peak value)		$V_{5-4(p-p)}$	–	–	1	V
Input resistance		R_{5-4}	10	13	16	kΩ
Input capacitance		C_{5-4}	–	–	10	pF

parameter	conditions	symbol	min.	typ.	max.	unit
Delayed chrominance input signal (peak-to-peak value)		$V_{12\text{-}4(p\text{-}p)}$	–	–	1	V
Input resistance		$R_{12\text{-}4}$	–	50	–	kΩ
Input capacitance		$C_{12\text{-}4}$	–	–	10	pF
Voltage gain		$\frac{V_{7\text{-}4}}{V_{12\text{-}4}}$	–	$\frac{R_A}{R_J}$	–	
Gain adjustment range		ΔG	19	–	–	dB
Gain bandwidth product		f_G	30	–	–	MHz
Output signal (peak-to-peak value)		$V_{7\text{-}4(p\text{-}p)}$	–	–	1	V
Output resistance		$R_{7\text{-}4}$	$\frac{V_T}{I_C}$	–	–	Ω
DC output voltage		$V_{7\text{-}4}$	–	–	2,5	V
Difference in DC output levels at pin 7 with pin 5/pin 12 switching		$\Delta V_{7\text{-}4}$	–	–	20	mV
Output selection control						
Input resistance		$R_{11\text{-}4}$	20	25	30	kΩ
Input voltage to select pin 5 signal for output		$V_{11\text{-}4}$	0	–	1,5	V
Input voltage to select pin 12 signal for output		$V_{11\text{-}4}$	2,75	–	5,0	V
Input voltage for automatic output switching*		$V_{11\text{-}4}$	2,0	–	2,6	V

DEVELOPMENT DATA

* This voltage is generated internally if pin 11 is not connected.

TV VHF MIXER/OSCILLATOR/UHF PREAMPLIFIER

GENERAL DESCRIPTION

The TDA5030A provides VHF local oscillator, VHF mixer and UHF IF preamplifier functions for VHF/UHF television receivers. It includes a buffered output from the VHF local oscillator, a VHF/UHF switching circuit and an IF amplifier stage for an external SAW filter.

Features

- Balanced VHF mixer
- Voltage-controlled VHF local oscillator
- IF amplifier for SAW filter
- UHF IF preamplifier
- Local oscillator buffer output for external prescaler
- Voltage stabilizer
- UHF/VHF switching circuit
- Electrostatic discharge protection diodes at pins 10, 11, 12 and 13

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 15	V_P	10	–	13,2	V
Supply current		I_P	–	42	–	mA
VHF mixer frequency range		f	50	–	470	MHz
Conversion gain			–	24,5	–	dB
Conversion noise	300 MHz		–	10	–	dB
Input signal for 1% cross modulation			–	99	–	dBμV
Storage temperature range		T_{stg}	−55	–	+ 125	°C
Operating ambient temperature range		T_{amb}	−25	–	+ 85	°C

PACKAGE OUTLINE

18-lead DIL, plastic (SOT102).

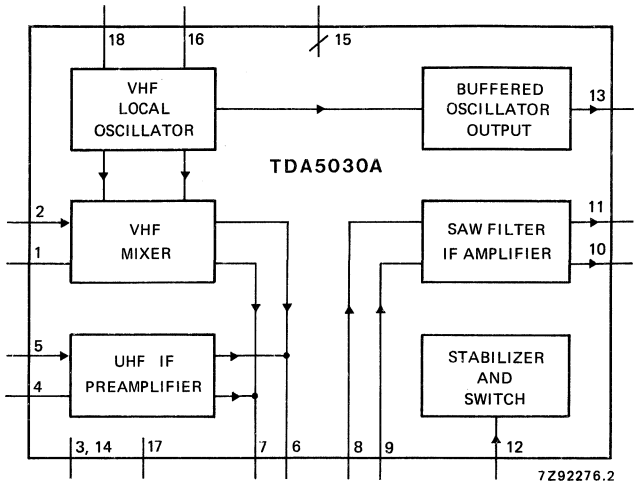


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	pin 15	$V_P = V_{15-3}$	–	14	V
Input voltage	pins 1, 2, 4 and 5	V_i	0	5	V
VHF switching voltage	pin 12	V_{12}	0	$V_{15}+0,3$	V
Output current	pins 10, 11 or 13	$-I_{10, 11, 13}$	–	10	mA
Short-circuit time on outputs	pins 10 and 11	t_{ss}	–	10	s
Storage temperature range		T_{stg}	–55	+ 125	°C
Operating ambient temperature range		T_{amb}	–25	+ 85	°C
Junction temperature range		T_j	–	+ 125	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j-a}$ 55 K/W

CHARACTERISTICS

Measured in circuit of Fig. 2, $V_P = V_{15-3} = 12$ V, $T_{amb} = 25\ ^oC$, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	pin 15	V_{15-3}	10	–	13,2	V
Supply current		I_{15}	–	42	55	mA
Switch voltage level for VHF	pin 12	V_{12}	0	–	2,5	V
Switch voltage level for UHF	pin 12	V_{12}	9,5	–	$V_{15}+0,3$	V
Switch current	UHF selected	I_{12}	–	–	0,7	mA
VHF mixer (including IF amplifier)						
Frequency range		f	50	–	470	MHz
Noise factor	pin 2					
	f = 50 MHz	F	–	7,5	9	dB
	f = 225 MHz	F	–	9	10	dB
	f = 300 MHz	F	–	10	12	dB
	f = 470 MHz	F	–	11	13	dB
Optimum source conductance	pin 2					
	f = 50 MHz	G	–	0,5	–	mS
	f = 225 MHz	G	–	1,1	–	mS
	f = 300 MHz	G	–	1,2	–	mS
Input conductance	pin 2					
	f = 50 MHz	G_i	–	0,23	–	mS
	f = 225 MHz	G_i	–	0,5	–	mS
	f = 300 MHz	G_i	–	0,67	–	mS
Input capacitance	pin 2					
	f = 50 MHz	C_i	–	2,5	–	pF
Input voltage for 1% cross-modulation (in channel)		V_{2-3}	97	99	–	dBμV
Input voltage for 10 kHz pulling (in channel)	f < 300 MHz	V_{2-14}	100	–	–	dBμV
Voltage gain		A_v	22,5	24,5	26,5	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
UHF preamplifier (including IF amplifier)						
Input conductance	pin 5	G_i	–	0,3	–	mS
Input capacitance	pin 5	C_i	–	3,0	–	pF
Noise factor	pin 5	F	–	5	6	dB
Optimum source conductance	pin 5	G	–	3,3	–	mS
Input voltage for 1% cross-modulation (in channel)		$V_{5\text{-}14}$	88	90	–	dBμV
Voltage gain		A_v	31,5	33,5	35,5	dB
VHF mixer						
Conversion transadmittance	pins 2 to 6,7	$Yc_{2\text{-}6,7}$	–	5,7	–	mS
Output impedance	pins 6 and 7	Z_o	–	1,6	–	kΩ
VHF oscillator						
Frequency range		f	70	–	520	MHz
Frequency shift	ΔV_P = 10%; f = 70–330 MHz	Δf	–	–	200	kHz
Frequency drift	ΔT = 15 K; f = 70–330 MHz	Δf	–	–	250	kHz
Frequency drift	between 5 s and 15 min after switch-on	Δf	–	–	200	kHz
SAW filter IF amplifier						
Input impedance	$Z_{10,11}$ = 2 kΩ; f = 36 MHz	$Z_{8,9}$	–	300+ j100	–	Ω
Transimpedance		$Z_{8,9\text{-}10,11}$	–	2,2	–	kΩ
Output reflection coefficient:	f = 36 MHz					
modulus			0,45	0,37	0,41	
phase			–63	–112	–134	deg

parameter	conditions	symbol	min.	typ.	max.	unit
VHF local oscillator output buffer						
Output voltage	pin 13 R_L = 75 Ω f < 100 MHz	V_{13}	14	20	–	mV
	f > 100 MHz	V_{13}	10	20	–	mV
Output impedance	f = 100 MHz	Z_{13}	–	90	–	Ω
RF signal on local oscillator output	R_L = 75 Ω V_i = 1 V; f ⩽ 225 MHz	RF/(RF+LO)	–	–	10	dB
	V_i = 0,3 V; f = 225–300 MHz	RF/(RF+LO)	–	–	10	dB
IF signal on local oscillator output	UHF selected; R_L = 75 Ω; V_i = 350 mV	IF/(IF+LO)	–	–	3	mV
Local oscillator harmonics w.r.t. local oscillator output signal	R_L = 75 Ω		–	–	−14	dB

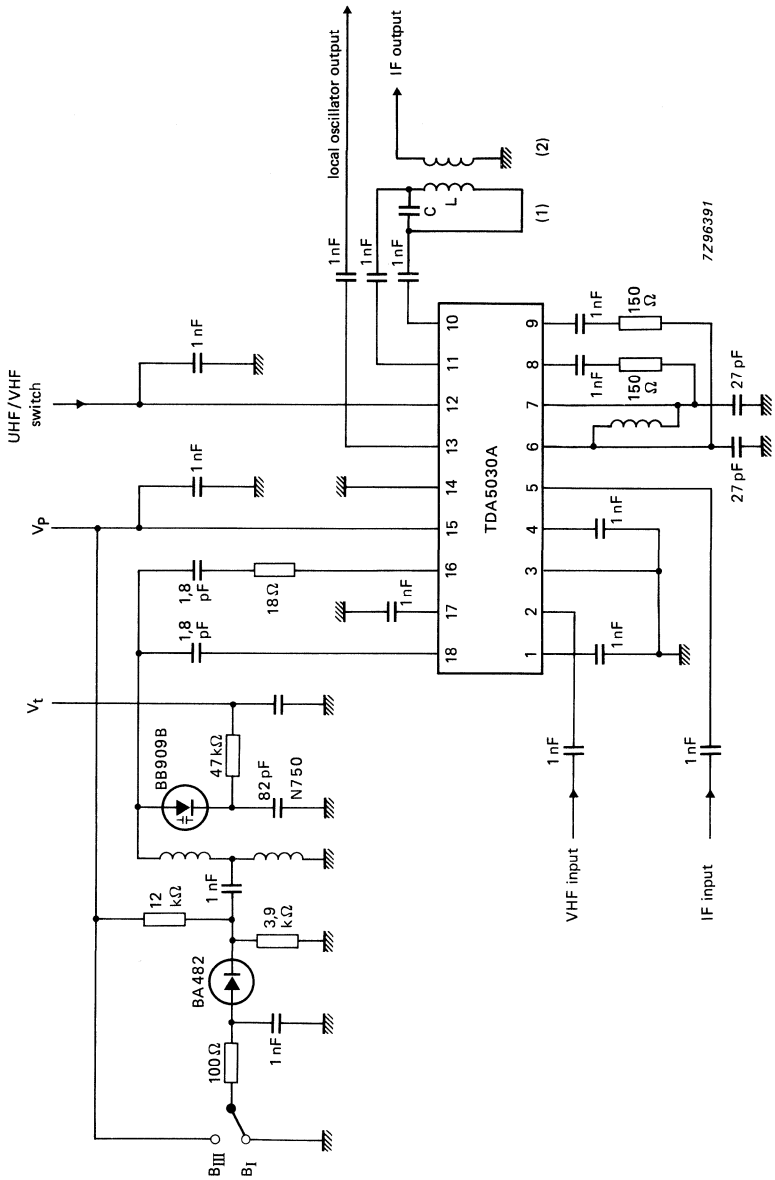


Fig. 2 Test circuit.

(1) C = 18 pF, L = 2,2 μH, f_{CL} = 36,5 MHz.

(2) Turns ratio = 7 : 1, load = 50 Ω.

TV VHF MIXER/OSCILLATOR/UHF PREAMPLIFIER

GENERAL DESCRIPTION

The TDA5030AT provides VHF local oscillator, VHF mixer and UHF IF preamplifier functions for VHF/UHF television receivers. It includes a buffered output from the VHF local oscillator, a VHF/UHF switching circuit and an IF amplifier stage for an external SAW filter.

Features

- Balanced VHF mixer
- Voltage-controlled VHF local oscillator
- IF amplifier for SAW filter
- UHF IF preamplifier
- Local oscillator buffer output for external prescaler
- Voltage stabilizer
- UHF/VHF switching circuit
- Electrostatic discharge protection diodes at pins 11, 12, 13 and 14

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 17)		V_P	10	–	13,2	V
Supply current		I_P	–	42	–	mA
VHF mixer frequency range		f	50	–	470	MHz
Conversion gain			–	25	–	dB
Conversion noise	300 MHz		–	10	–	dB
Input signal for 1% cross modulation			–	99	–	dBμV
Storage temperature range		T_{stg}	−55	–	+ 125	°C
Operating ambient temperature range		T_{amb}	−25	–	+ 80	°C

PACKAGE OUTLINE

20-lead mini-pack; plastic (SO20; SOT163A).

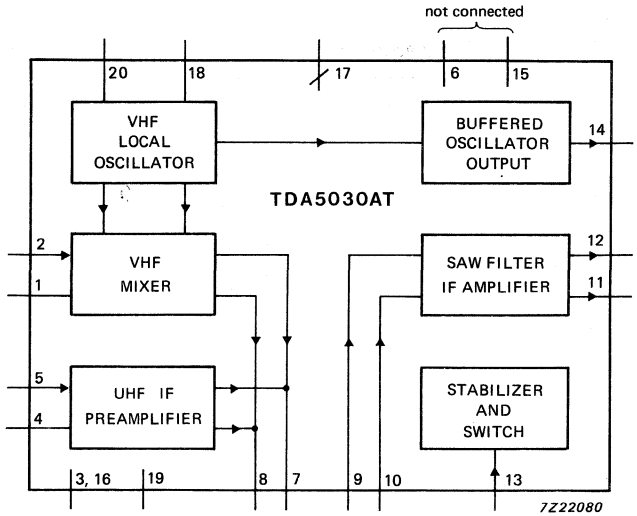


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 17)	$V_P = V_{17-3}$	–	14	V
Input voltage (pins 1, 2, 4 and 5)	V_i	0	5	V
VHF switching voltage (pin 13)	V_{13}	0	V_P+0,3	V
Output current (pins 11, 12 or 14)	$-I_{11,12,14}$	–	10	mA
Short-circuit time on outputs (pins 11, 12 and 14)	t_{sc}	–	10	s
Storage temperature range	T_{stg}	–55	+125	°C
Operating ambient temperature range	T_{amb}	–25	+ 80	°C
Junction temperature range	T_j	–	+150	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 75 K/W

CHARACTERISTICS

$V_P = V_{17-3} = 12$ V; $T_{amb} = 25$ °C; measured in circuit of Fig. 2; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage (pin 17)		V_{17-3}	10	–	13,2	V
Supply current		I_{17}	–	42	55	mA
Switch voltage level for VHF (pin 13)		V_{13}	0	–	2,5	V
Switch voltage level for UHF (pin 13)		V_{13}	9,5	–	V_P+0,3	V
Switch current	UHF selected	I_{13}	–0,05	–	0,7	mA
VHF mixer (including IF amplifier)						
Frequency range		f	50	–	470	MHz
Noise factor (pin 2)	f = 50 MHz	NF	–	7,5	9	dB
	f = 225 MHz	NF	–	9	10	dB
	f = 300 MHz	NF	–	10	12	dB
	f = 470 MHz	NF	–	11	13	dB
Optimum source conductance (pin 2)	f = 50 MHz	G	–	0,5	–	mS
	f = 225 MHz	G	–	1,1	–	mS
	f = 300 MHz	G	–	1,2	–	mS
	f = 470 MHz	G	–	1,9	–	mS
Input conductance (pin 2)	f = 50 MHz	G_i	–	0,23	–	mS
	f = 225 MHz	G_i	–	0,5	–	mS
	f = 300 MHz	G_i	–	0,67	–	mS
	f = 470 MHz	G_i	–	1,45	–	mS
Input capacitance (pin 2)	f = 50 MHz	C_i	–	2,5	–	pF
Input voltage for 1% cross-modulation (in channel)		V_{2-3}	96	99	–	dBμV
Input voltage for 10 kHz pulling (in channel)	f < 300 MHz	V_{2-16}	100	–	–	dBμV
Input voltage for 100 kHz pulling	f = 470 MHz	V_{2-3}	73	–	–	dBμV
Voltage gain		A_v	23	25	27	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
UHF preamplifier (including IF amplifier)						
Input conductance (pin 5)		G_i	–	0,3	–	mS
Input capacitance (pin 5)		C_i	–	3,0	–	pF
Noise factor (pin 5)		NF	–	5	6	dB
Optimum source conductance (pin 5)		G	–	3,3	–	mS
Input voltage for 1% cross-modulation (in channel)		V_{5-16}	88	90	–	dBμV
Voltage gain		A_v	32	34	36	dB
VHF mixer						
Conversion transadmittance (pins 2 to 7, 8)		$Yc_{2-7,8}$	–	5,7	–	mS
Output impedance (pins 7 and 8)		Z_o	–	1,6	–	kΩ
VHF oscillator						
Frequency range		f	70	–	520	MHz
Frequency shift	ΔV_P = 10%; f = 70 to 330 MHz	Δf	–	–	200	kHz
Frequency drift	ΔT = 15 K; f = 70 to 330 MHz	Δf	–	–	250	kHz
Frequency drift	between 5 s and 15 min after switch-on	Δf	–	–	200	kHz
SAW filter IF amplifier						
Input impedance	$Z_{11,12}$ = 2 kΩ; f = 36 MHz	$Z_{9,10}$	–	300+ j100	–	Ω
Transimpedance		$Z_{9,10-11,12}$	–	2,2	–	kΩ
Output reflection coefficient:	f = 36 MHz					
modulus			0,45	0,37	0,41	
phase			–63	–112	–134	deg

parameter	conditions	symbol	min.	typ.	max.	unit
VHF local oscillator output buffer						
Output voltage (pin 14)	R_L = 75 Ω					
	f < 100 MHz	V_{14}	14	20	–	mV
	f > 100 MHz	V_{14}	10	20	–	mV
Output impedance	f = 100 MHz	Z_{14}	–	90	–	Ω
RF signal on local oscillator output	R_L = 75 Ω					
	V_i = 1 V; f ≤ 225 MHz	RF/(RF+LO)	–	–	10	dB
	V_i = 0,3 V; f = 225–300 MHz	RF/(RF+LO)	–	–	10	dB
IF signal on local oscillator output	UHF selected; R_L = 75 Ω; V_i = 350 mV	IF/(IF+LO)	–	–	3	mV
Local oscillator harmonics w.r.t. local oscillator output signal	R_L = 75 Ω		–	–	–14	dB

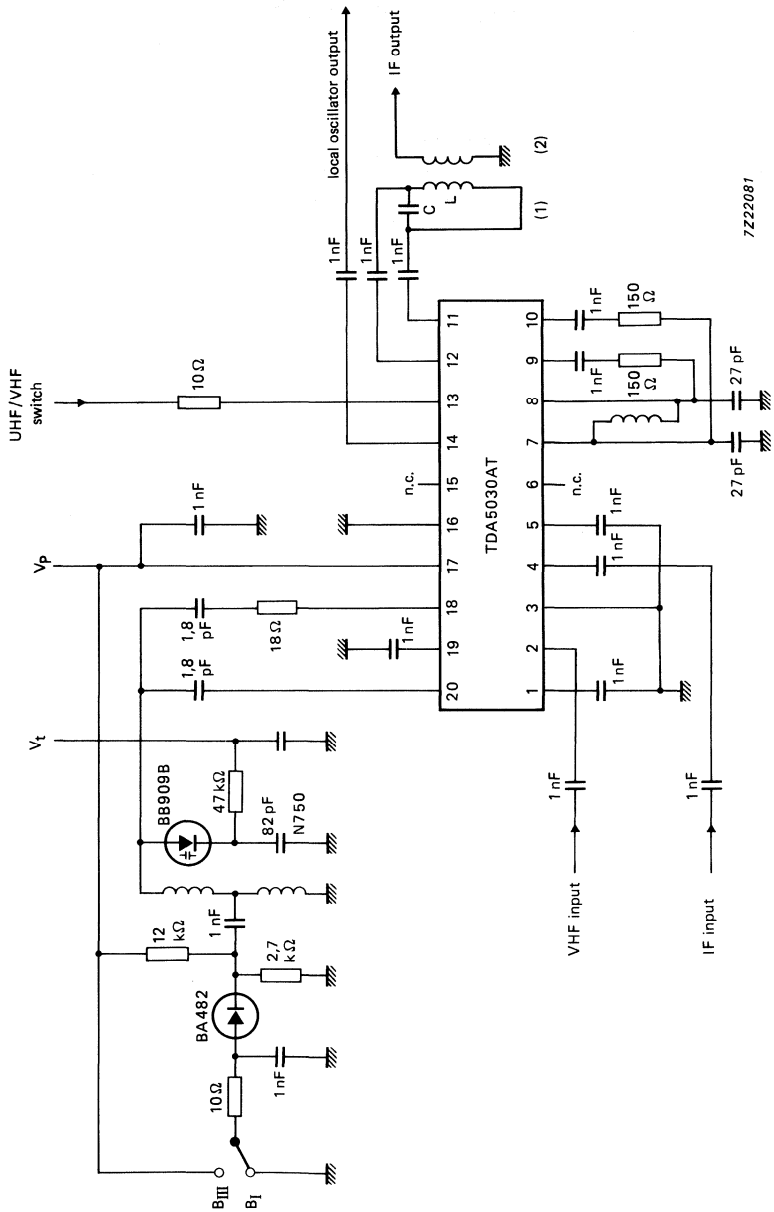


Fig. 2 Test circuit.

(1) C = 18 pF, L = 2,2 μH, f_{CL} = 36,5 MHz.
(2) Turns ratio = 7 : 1, load = 50 Ω.

VHF, UHF AND HYPERBAND MIXER/OSCILLATOR FOR TV AND VCR 3-BAND TUNERS

GENERAL DESCRIPTION

The TDA5330T is a monolithic integrated circuit that performs the band A, band B and band C mixer/oscillator functions in TV and VCR tuners. This device gives the designer the capability to design an economical and physically small 3-band tuner which will be capable of meeting the most stringent requirements e.g. FTZ or FCC. The tuner development time can be drastically reduced by using this device.

Features

- Balanced mixer with a common emitter input for band A
- Amplitude-controlled oscillator for band A
- Balanced mixer with common base input for band B and C
- Balanced oscillator for band B and C
- Local oscillator buffer output for external prescaler
- SAW filter preamplifier with an output impedance of 100 Ω
- Bandgap voltage stabilizer for oscillator stability
- Electronic bandswitch

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		$V_{19\text{-}2,\ 26}$	–	12	–	V
Band A frequency range		f_A	48	–	180	MHz
Band B frequency range		f_B	160	–	470	MHz
Band C frequency range		f_C	430	–	860	MHz
Conversion noise		F	7	–	11	dB
Band A input voltage	1% cross-modulation	$V_{24\text{-}26}$	–	100	–	dBμV
Band B and C input power	1% cross-modulation	P_I	–	–21	–	dBm
Band A voltage gain		G_v	–	24	–	dB
Band B voltage gain		G_v	–	37	–	dB
Band C voltage gain		G_v	–	36	–	dB

PACKAGE OUTLINE

28-lead mini-pack, plastic (SO20; SOT163A).

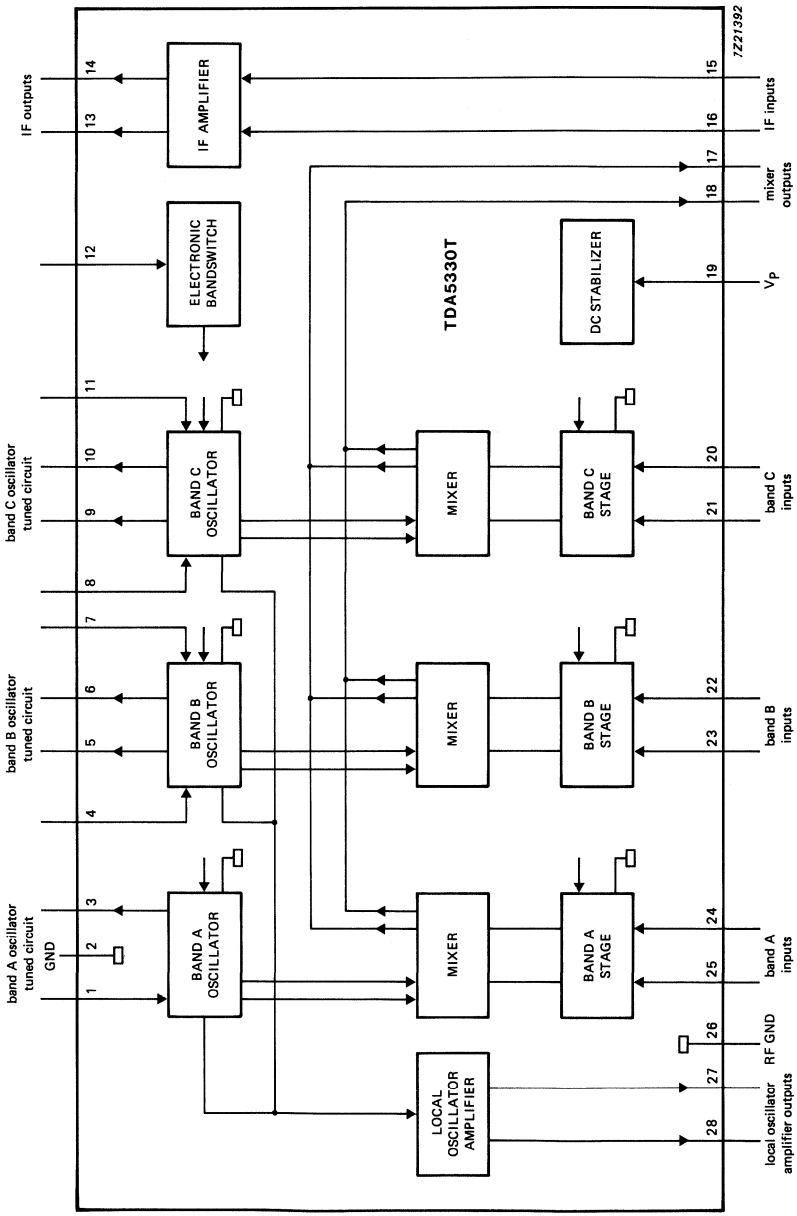


Fig. 1 Block diagram.

DEVELOPMENT DATA

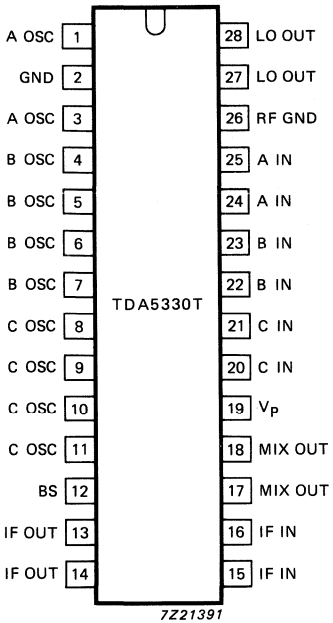


Fig. 2 Pinning diagram.

PINNING

1	A OSC	band A oscillator input
2	GND	ground (0 V)
3	A OSC	band A oscillator output
4	B OSC	band B oscillator input
5	B OSC	band B oscillator output
6	B OSC	band B oscillator output
7	B OSC	band B oscillator input
8	C OSC	band C oscillator input
9	C OSC	band C oscillator output
10	C OSC	band C oscillator output
11	C OSC	band C oscillator input
12	BS	electronic bandswitch
13	IF OUT	IF amplifier output
14	IF OUT	IF amplifier output
15	IF IN	IF amplifier input
16	IF IN	IF amplifier input
17	MIX OUT	mixer output
18	MIX OUT	mixer output
19	V_P	positive supply voltage
20	C IN	band C input
21	C IN	band C input
22	B IN	band B input
23	B IN	band B input
24	A IN	band A input
25	A IN	band A input
26	RF GND	ground for RF inputs
27	LO OUT	local oscillator amplifier output
28	LO OUT	local oscillator amplifier output

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		$V_P = V_{19-2, 26}$	−0.3	14	V
Switching voltage		V_{12}	0	14	V
Output current of each pin to ground		I_O	–	−10	mA
Maximum short-circuit time (all pins)		t_{sc}	–	10	s
Storage temperature range		T_{stg}	−55	+150	°C
Operating ambient temperature range		T_{amb}	−25	+80	°C

THERMAL RESISTANCE

From junction to ambient in free air $R_{th\ j\text{-}a}$ typ. 75 K/W

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		$V_{19\text{-}2,\ 26}$	10	–	13.2	V
Supply current		I_{19}	–	42	55	mA
Switching voltage; band A		V_{12}	0	–	1.1	V
band B		V_{12}	1.6	–	2.4	V
band C		V_{12}	3.0	–	5.0	V
Switching current; band C		I_{12}	–	–	50	μA
Band A Mixer (including IF amplifier)	measured using circuit shown in Fig. 9					
Frequency range		f_A	48	–	180	MHz
Noise figure	note 1;					
	50 MHz	NF	–	7.5	9	dB
	180 MHz	NF	–	9	10	dB
Optimum source conductance	50 MHz	$G_{24\text{-}26}$	–	0.5	–	mS
	180 MHz	$G_{24\text{-}26}$	–	1.1	–	mS
Input admittance	see Fig. 9					
Input capacitance	50 - 180 MHz	$C_{24\text{-}26}$	–	2	–	pF
Input voltage	1% cross-modulation; in channel	$V_{24\text{-}26}$	97	100	–	dBμV
Input voltage	10 kHz pulling; in channel	$V_{24\text{-}26}$	100	108	–	dBμV
Voltage gain	20 log $(V_{13\text{-}14}/V_{24})$	G_v	22.5	25.0	27.5	dB
Band A mixer						
Conversion transadmittance mixer	$Sc = I_{17}/V_{24}$ $= -I_{18}/V_{24}$	$Sc_{24\text{-}17,\ 18}$	–	3.5	–	mS
Mixer output admittance	pins 15 and 16		–	0.1	–	mS
Mixer output capacitance		$C_{17\text{-}18}$	–	2	–	pF

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Band A oscillator						
Frequency range		f_A	80	–	216	MHz
Frequency shift	ΔV_P = 10%	Δf	–	–	200	kHz
Frequency drift	ΔT = 25 °C	Δf	–	–	400	kHz
Frequency drift	5 s to 15 min after switching on	Δf	–	–	200	kHz
Band B mixer (including IF)	measured using circuit shown in Fig. 9; measurements using hybrid; note 2					
Frequency range		f_B	160	–	470	MHz
Noise figure	pins 22 and 23;					
	200 MHz	NF	–	8	10	dB
	470 MHz	NF	–	8	10	dB
Input admittance	see Fig. 5					
Available input power	1% cross-modulation; in channel; pins 22 and 23;					
	200 MHz	P_{AI}	–24	–21	–	dBm
	470 MHz	P_{AI}	–24	–21	–	dBm
10 kHz pulling	pins 22 and 23; in channel;					
	470 MHz		–	–11	–	dBm
N+5 – 1 MHz pulling	note 3;					
	430 MHz		–	–11	–	dBm
Voltage gain	note 4;					
	200 MHz	G_V	33	36	39	dB
	470 MHz	G_V	33	36	39	dB
Band B oscillator						
Frequency range		f_B	200	–	500	MHz
Frequency shift	ΔV_P = 10%	Δf	–	–	400	kHz
Frequency drift	ΔT = 25 °C	Δf	–	–	500	kHz
Frequency drift	5 s to 15 min after switching on	Δf	–	–	200	kHz

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.		max.	unit
Band C mixer (including IF)	measured using circuit shown in Fig. 9; measurements using hybrid; note 2						
Frequency range		f_C	430	–		860	MHz
Noise figure	pins 20 and 21;						
	430 MHz	NF	–	9		11	dB
	860 MHz	NF	–	9		11	dB
Input admittance	see Fig. 6						
Available input power	1% cross-modulation in channel; pins 20 and 21;						
	430 MHz	P_{AI}	–25	–21		–	dBm
	860 MHz	P_{AI}	–25	–21		–	dBm
10 kHz pulling	pins 20 and 21; in channel;						
	860 MHz		–	–20		–	dBm
N+5 – 1 MHz pulling	note 3;						
	820 MHz		–42	–35		–	dBm
Voltage gain	note 4;						
	430 MHz	G_v	33	36		39	dB
	860 MHz	G_v	33	36		39	dB
Band C oscillator							
Frequency range		f_C	470	–		900	MHz
Frequency shift	$\Delta V_b = 10\%$	Δf	–	–		400	kHz
Frequency drift	$\Delta T = 25\ ^oC$	Δf	–	–		800	kHz
Frequency drift	5 s to 15 min after switching on	Δf	–	–		200	kHz
				mod.	phase		
IF Amplifier	note 5; differentially measured at 36 MHz; see Fig. 7						
Input reflection coefficient		S_{11}	–	–0,5	–2.0	–	dB/deg
Reverse transmission coefficient		S_{12}	–	–41	–7	–	dB/deg
Forward transmission coefficient		S_{21}	–	12	160	–	dB/deg
Output reflection coefficient	see Fig. 8	S_{22}	–	–9	10	–	dB/deg

parameter	conditions	symbol	min.	typ.	max.	unit
LO output						
Output voltage into 50 Ω resistor		V_{27-28}	14	35	100	mV
Spurious signal on LO output with respect to LO output signal	note 6	SRF	–	–	−10	dB
LO signal harmonics with respect to LO signal	measured at 50 Ω	SHD	–	–	−10	dB

Notes to the characteristics

1. Measured with an input circuit for optimum noise. (See Fig. 3).

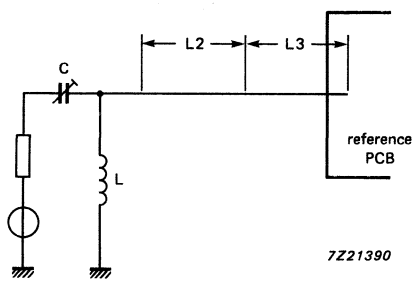


Fig. 3 Input circuit for optimum noise.

Table 1 Component values

component	f = 50 MHz	f = 180 MHz
L	13 t, ϕ 5.5 mm, wire 0.7 mm	*
L2	rigid cable, 2.9 cm	*
L3	rigid cable, 4 cm	*
C	9.6 pF	*

* Value to be fixed.

Notes to the characteristics (continued)

Table 2 Electrical parameters of the circuit (for appropriate impedance and selectivity)

parameter	f = 50 MHz	f = 180 MHz	unit
Insertion loss	0.3	*	dB
Bandwidth	8	*	MHz
Image suppression	15	*	dB
Output impedance (source for IC)	2	*	kΩ

2. The values have been corrected for hybrid and cable losses. The symmetrical output impedance of the circuit is 100 Ω.
3. The input level of a N+5 — 1 MHz signal (just visible).
4. The gain is defined as the transducer gain (measured in Fig. 9) plus the voltage transformation ratio of L6 to L7 (6:1, 16 dB).
5. All S parameters are referred to a 50 Ω system.
6. Measured with 50 Ω output impedance on pins 26 and 27 and a RF input signal level of:
   RF level = 1 V at $f < 180$ MHz
   RF power = 0.5 dBm at 100 MHz $< f <$ 225 MHz
   RF power = −10 dBm at 225 MHz $< f <$ 860 MHz

* Value to be fixed.

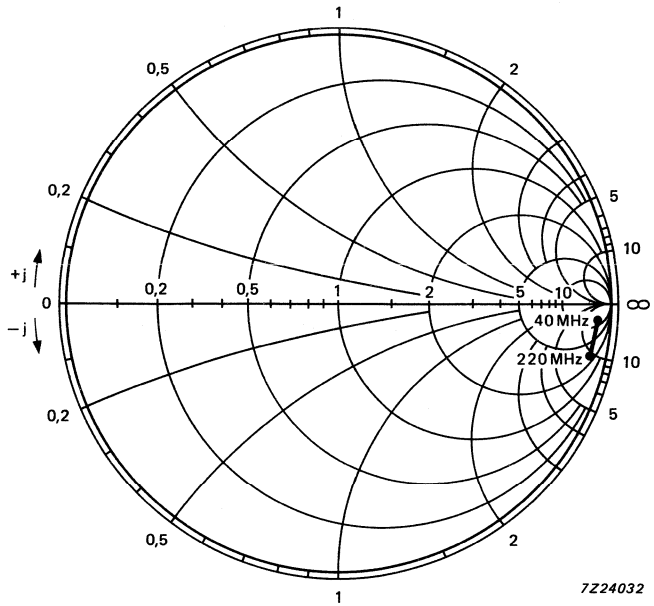


Fig. 4 S11 of the band A mixer input (40 to 220 MHz).

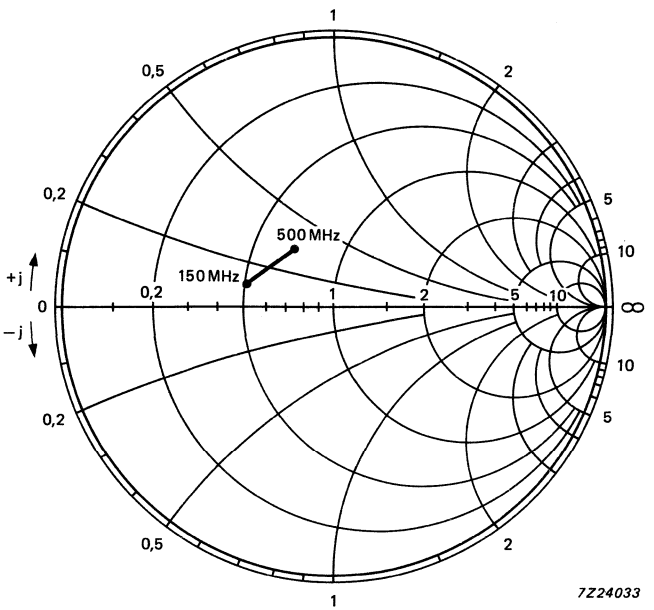


Fig. 5 S11 of the band B mixer input (150 to 500 MHz).

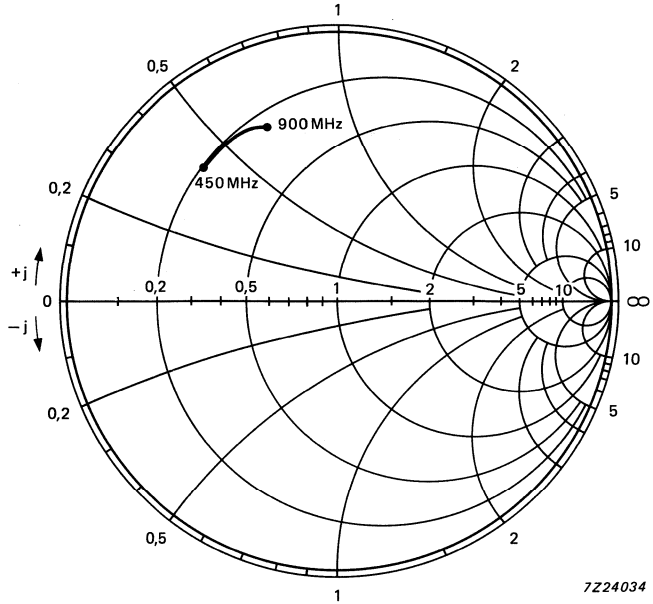


Fig. 6 S11 of the band C mixer input (450 to 900 MHz).

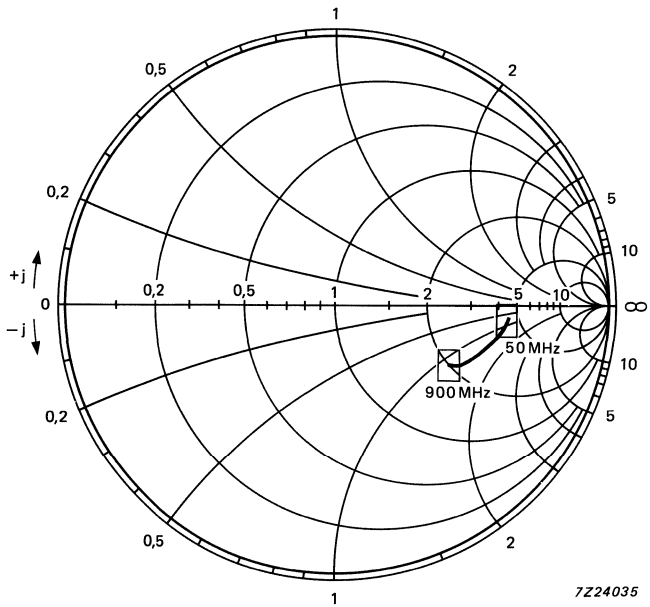


Fig. 7 S11 of the LO output (50 to 900 MHz).

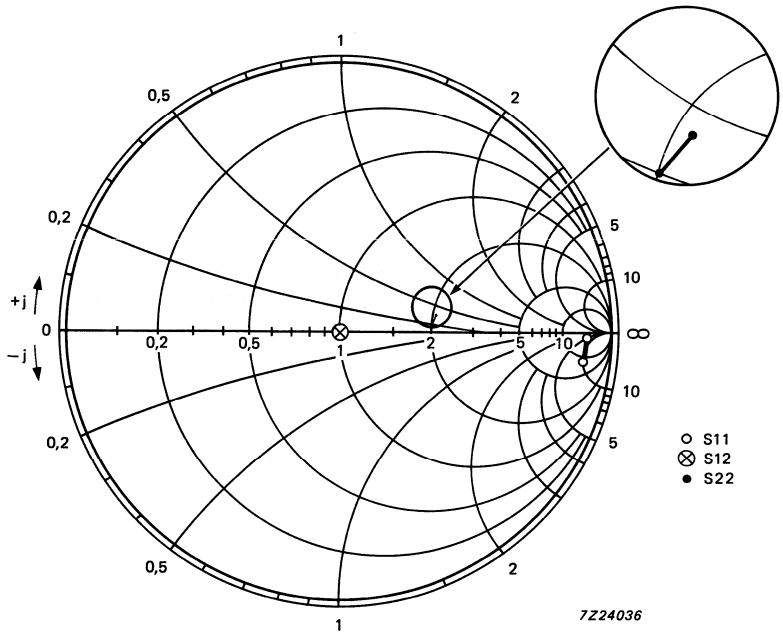


Fig. 8 S11, S12 and S22 of the IF amplifier (30 to 60 MHz).

DEVELOPMENT DATA

APPLICATION INFORMATION

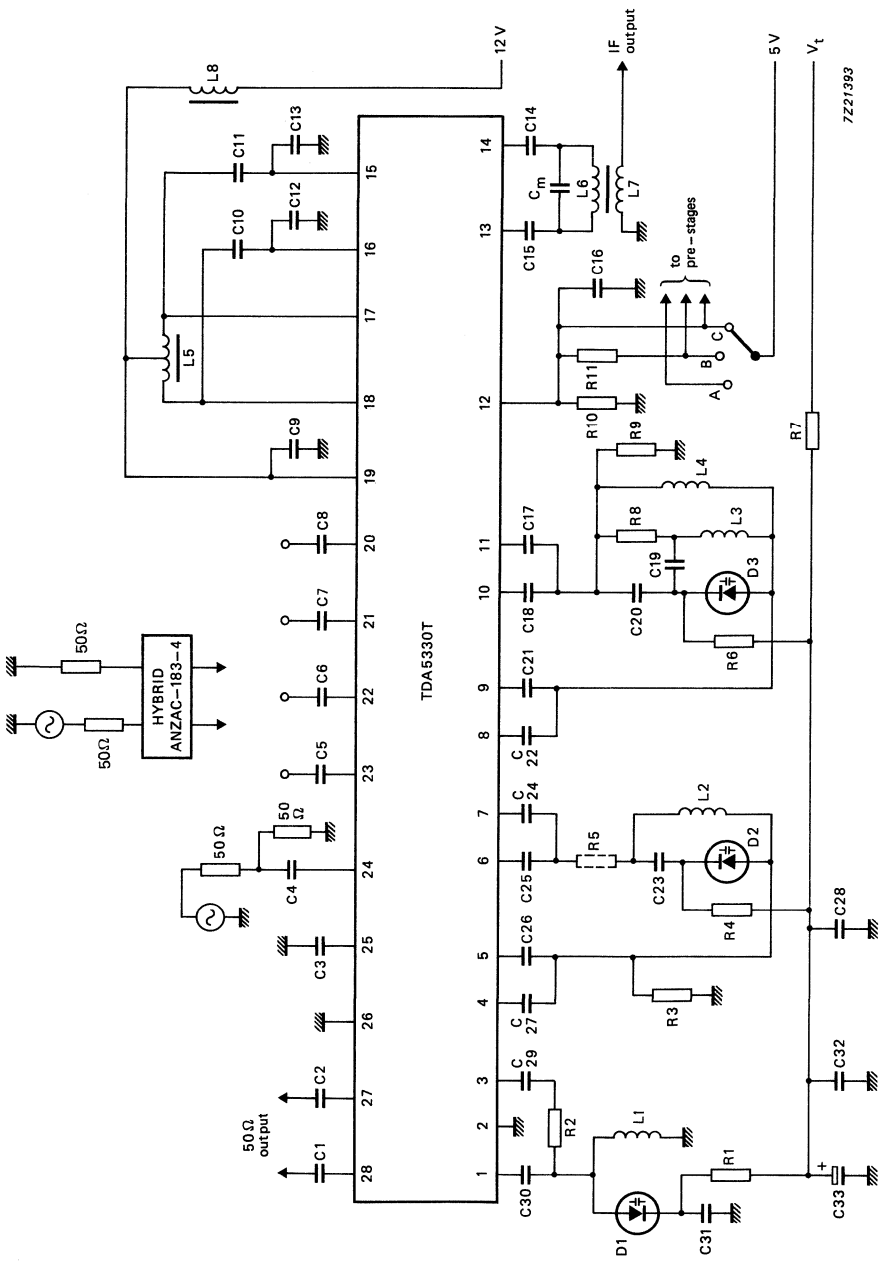


Fig. 9 Test circuit diagram.

Component values of the test circuit

resistors

R1 = 47 kΩ	R2 = 18 Ω	R3 = 22 kΩ	R4 = 22 kΩ
R5 = 22 Ω (SMD)	R6 = 22 kΩ	R7 = 1 kΩ	R8 = 2.2 kΩ
R9 = 22 kΩ	R10 = 15 kΩ	R11 = 22 kΩ	

capacitors

C1 = 1 nF	C2 = 1 nF	C3 = 1 nF	C4 = 1 nF
C5 = 1 nF	C6 = 1 nF	C7 = 1 nF	C8 = 1 nF
C9 = 1 nF	C10 = 1 nF	C11 = 1 nF	C12 = 15 pF (N750)
C13 = 15 pF (N750)	C14 = 1 nF	C15 = 1 nF	C16 = 1 nF
C17 = 0.68 pF (SMD)	C18 = 1 pF (SMD)	C19 = 100 pF (SMD)	C20 = 5.6 pF (SMD)
C21 = 1 pF	C22 = 0.68 pF (SMD)	C23 = 150 pF (N750)	C24 = 1.8 pF (N750)
C25 = 3.3 pF (SMD)	C26 = 3.3 pF (SMD)	C27 = 1.8 pF (SMD)	C28 = 1 nF
C29 = 1 pF (NPO)	C30 = 1 pF (NPO)	C31 = 82 pF (N750)	C32 = 1 nF
C33 = 1 μF (40 V)	Cm = 18 pF (N750)		

diodes and IC

D1 = BB911	D2 = BB909B	D3 = BB405B
IC = TDA5330T		

coils

L1 = 6.5 t (ϕ3)	L2 = 1.5 t (ϕ3)	L3 = 1.5 t (ϕ3)	L4 = 1.5 t (ϕ3)
L5 = 2 x 6 t*	L6 = 12 t*	L7 = 2 t (mounted on L6)	L8 = 5 μH (choke coil)

wire size for L1 to L4 = 0.4 and for L5 to L7 = 0.1 mm.

DEVELOPMENT DATA

* Coil type: TOKO 7 kN; material: 113 kN, screw core (03-0093), pot core (04-0026).

DOUBLE MIXER/OSCILLATOR FOR TV AND VCR TUNERS

GENERAL DESCRIPTION

The TDA5332T is an integrated circuit that performs the mixer/oscillator functions in TV and VCR tuners. This device gives the designer the capability to design an economical and physically small tuner which will be capable of meeting the most stringent requirements e.g. FTZ or FCC. The tuner development time can be drastically reduced by using this device.

Features

- Balanced mixer with a common emitter input for band A
- Amplitude-controlled oscillator for band A
- Balanced mixer with common base input for band B
- Balanced oscillator for band B
- SAW filter preamplifier with an output impedance of 75 Ω in application
- Bandgap voltage stabilizer for oscillator stability
- Electronic bandswitch

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	–	12	–	V
Band A frequency range	depending on application	f_A	45	–	470	MHz
Band B frequency range	depending on application	f_B	160	–	860	MHz
Band A noise factor	50 MHz	NF_A	–	7.5	–	dB
Band B noise factor	860 MHz	NF_B	–	9	–	dB
Band A input voltage	1% cross-modulation	$V_{18\text{-}20}$	–	100	–	dBμV
Band B input power	1% cross-modulation note 5	P_I	–	–21	–	dBm
Band A voltage gain		G_{VA}	–	25	–	dB
Band B voltage gain		G_{VB}	–	36	–	dB

PACKAGE OUTLINE

20-lead mini-pack, plastic (SO20L; SOT163A).

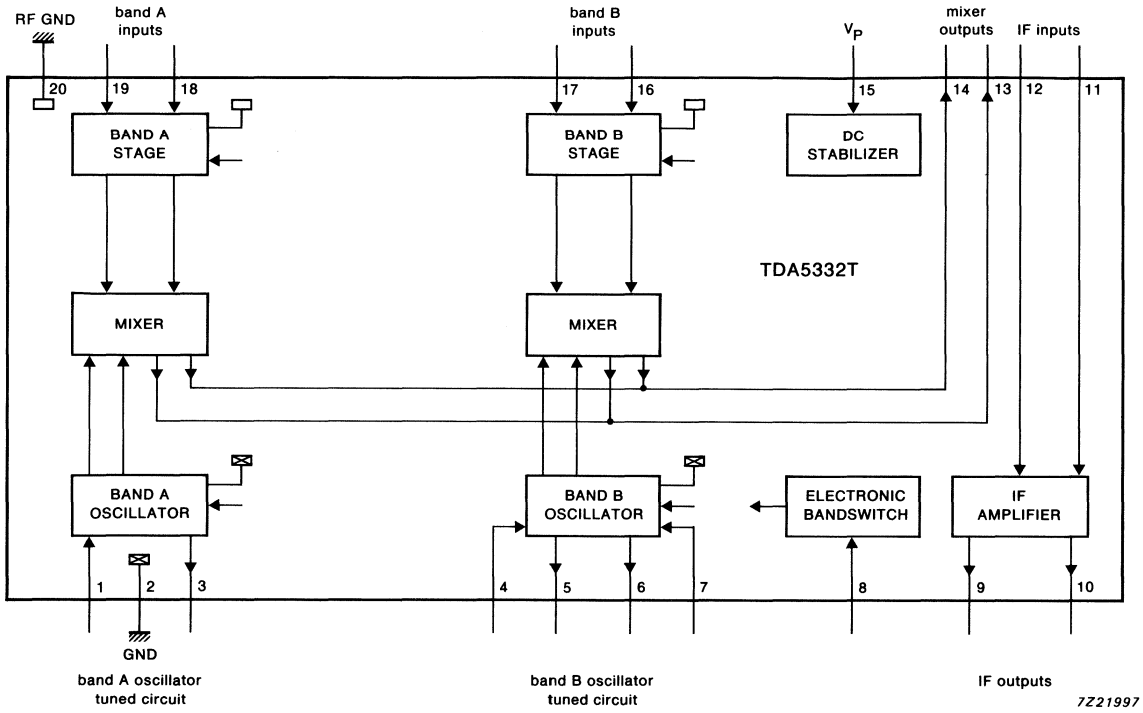


Fig.1 Block diagram.

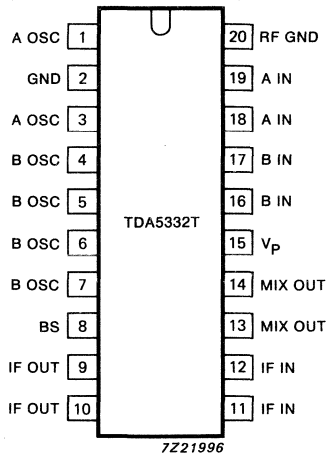


Fig.2 Pinning diagram.

PINNING

1	A OSC	band A oscillator input
2	GND	ground (0 V)
3	A OSC	band A oscillator output
4	B OSC	band B oscillator input
5	B OSC	band B oscillator output
6	B OSC	band B oscillator output
7	B OSC	band B oscillator input
8	BS	electronic bandswitch
9	IF OUT	IF amplifier output
10	IF OUT	IF amplifier output
11	IF IN	IF amplifier input
12	IF IN	IF amplifier input
13	MIX OUT	mixer output
14	MIX OUT	mixer output
15	V_P	positive supply voltage
16	B IN	band B input
17	B IN	band B input
18	A IN	band A input
19	A IN	band A input
20	RF GND	ground for RF inputs

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_P	−0.3	14	V
Switching voltage		V_8	0	14	V
Output current of each pin to ground		I_O	−	−10	mA
Maximum short-circuit time (all pins)		t_{sc}	−	10	s
Storage temperature range		T_{stg}	−55	+150	°C
Operating ambient temperature range		T_{amb}	−25	+80	°C
Junction temperature		T_j	−	+150	°C

THERMAL RESISTANCE

From junction to ambient in free air $R_{th\ j\text{-}a}$ typ. 100 K/W

HANDLING

Pins 8, 9 and 10 withstand the ESD test in accordance with MIL-STD-883C category B (2000 V).

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; all voltages are referenced to ground (pins 2 and 20); measured in Fig.3; unless otherwise specified.

parameter	conditions	symbol	min.	typ.		max.	unit
Supply voltage		V_{15}	10	–		13.2	V
Supply current		I_{15}	–	42		55	mA
Switching voltage;							
band A		V_{SA}	0	–		1.1	V
band B		V_{SB}	3	–		5	V
Switching current							
band A		I_{SA}	–	–		10	μA
band B		I_{SB}	–	–		50	μA
IF Amplifier	differentially measured at 36 MHz			mod.	phase		
Input reflection coefficient	note 4	S_{11}	–	–0.5	–2	–	dB/°
Reverse transmission coefficient		S_{12}	–	–41	–7	–	dB/°
Forward transmission coefficient		S_{21}	–	12	160	–	dB/°
Output reflection coefficient		S_{22}	–	–9	10	–	dB/°
Input admittance in application		Y_I	–	–	1.4	–	mS
					0.9	–	pF
Output admittance in application		Z_O	–	–	55	–	Ω
					230	–	nH
Band A mixer (including IF amplifier)	measured using circuit shown in Fig.3						
Frequency range		f_A	45	–		470	MHz
Noise factor	50 MHz	NF	–	7.5		9	dB
	225 MHz	NF	–	9		11	dB
	300 MHz	NF	–	10		12	dB
	470 MHz	NF	–	11		13	dB
Optimum source conductance	50 MHz	$G_{18\text{-}20}$	–	0.5		–	mS
	225 MHz	$G_{18\text{-}20}$	–	1.1		–	mS
	300 MHz	$G_{18\text{-}20}$	–	1.2		–	mS
	470 MHz	$G_{18\text{-}20}$	–	1.9		–	mS

parameter	conditions	symbol	min.	typ.	max.	unit
Input capacitance	50 - 470 MHz	C_{18-20}	–	2.5	–	pF
Input voltage	1% cross-modulation; in channel	V_{18-20}	97	100	–	dBμV
Input voltage	10 kHz pulling; in channel; f < 300 MHz	V_{18-20}	100	108	–	dBμV
Voltage gain	20 log (V_{9-10}/V_{18})	G_V	22.5	25.0	27.5	dB
Band A mixer						
Conversion transadmittance mixer	$I_{13}/V_{18} = -I_{14}/V_{18}$	C_t	–	3.5	–	mS
Mixer output admittance	pins 13 and 14		–	0.1	–	mS
Mixer output capacitance		C_{13-14}	–	2	–	pF
Band A oscillator						
Frequency range		f_A	80	–	520	MHz
Frequency shift	ΔV_P = 10% note 6; f = 330 MHz	Δf	–	–	200	kHz
Frequency drift	ΔT = 25 °C note 7; f = 330 MHz	Δf	–	–	400	kHz
Frequency drift	5 s to 15 min after switching on; f = 330 MHz	Δf	–	–	200	kHz
Band B mixer (including IF)	measured using circuit shown in Fig.3; measurements using hybrid; note 1					
Frequency range		f_B	160	–	860	MHz
Noise factor not corrected for image	pins 16 and 17					
	160 MHz	NF_B	–	9	11	dB
	860 MHz	NF_B	–	9	11	dB
Available input power	note 5; 1% cross-modulation; in channel; pins 16 and 17;					
	160 MHz	P_{IB}	–25	–21	–	dBm
	860 MHz	P_{IB}	–25	–21	–	dBm
10 kHz pulling	note 5; pins 16 and 17; in channel;					
	860 MHz		–	–20	–	dBm

DEVELOPMENT DATA

CHARACTERISTICS (continued)

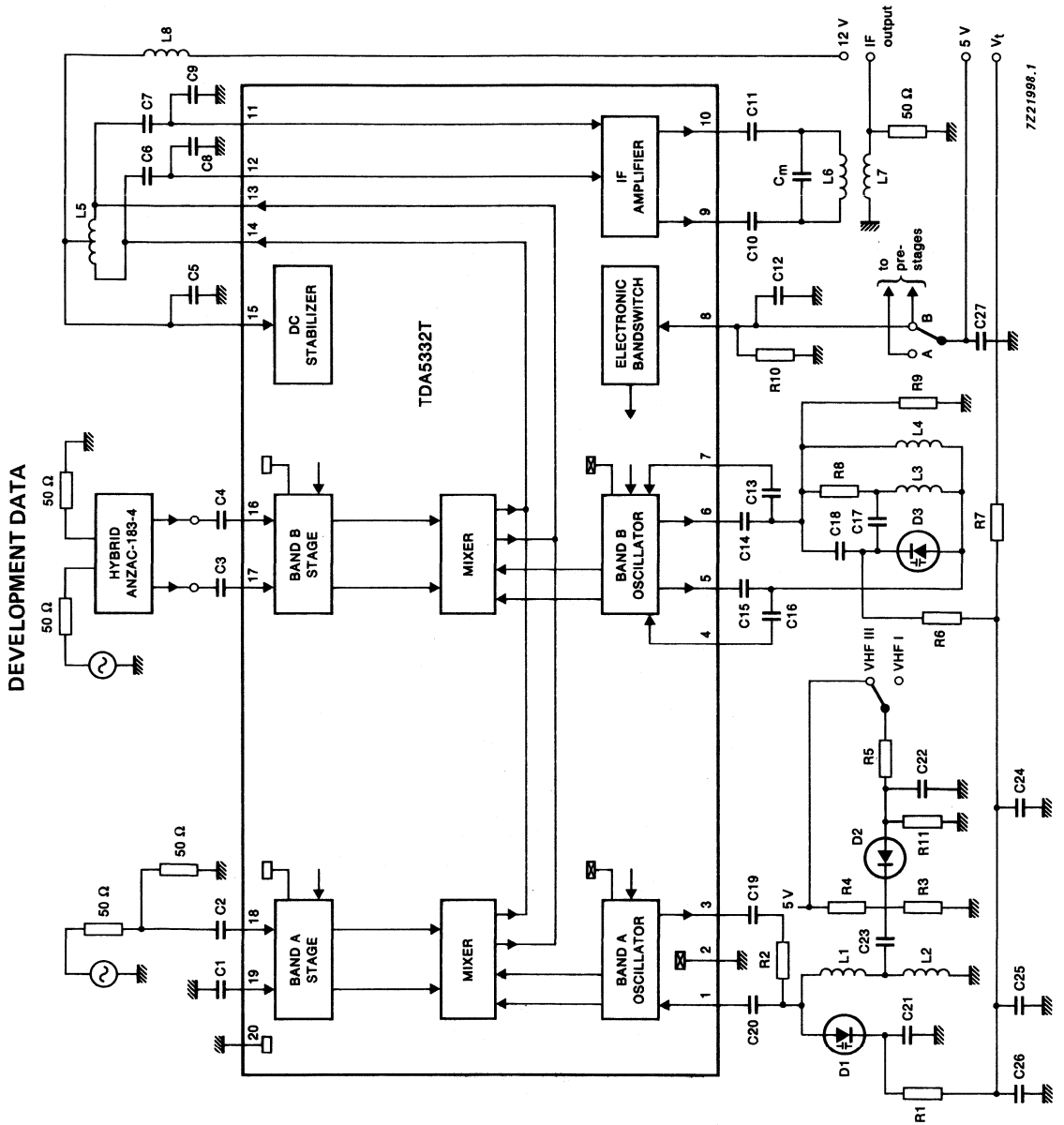
parameter	conditions	symbol	min.	typ.	max.	unit
N + 5 – 1 MHz pulling	notes 2 and 5; 820 MHz		–42	–35	–	dBm
Voltage gain	note 3;					
	160 MHz	G_{VB}	33	36	39	dB
	860 MHz	G_{VB}	33	36	39	dB
Band B oscillator						
Frequency range		f_B	200	–	900	MHz
Frequency shift	note 6; ΔV_P = 10%	Δf	–	–	400	kHz
Frequency drift	note 7; ΔT = 25 °C	Δf	–	–	800	kHz
Frequency drift	5 s to 15 min after switching on	Δf	–	–	400	kHz

Notes to the characteristics

1. The values have been corrected for hybrid and cable losses. The symmetrical output impedance of the circuit is 100 Ω.
2. The input level of a N + 5 – 1 MHz signal (just visible).
3. The gain is defined as the transducer gain (measured in Fig.3) plus the voltage transformation ratio of L6 to L7 (6:1, 16 dB).
4. All S parameters are referred to a 50 Ω system.
5. The input power is defined as the power delivered by the generator on a 50 Ω load.
6. The frequency shift is defined for a variation of power supply from;
   (a) V_P = 12 V to V_P = 10.8 V
   (b) V_P = 12 V to V_P = 13.2 V
   In both cases the frequency shift is below the specified value.
7. The frequency drift is defined for a variation of ambient temperature from;
   (a) T_{amb} = 25 °C to T_{amb} = 0 °C
   (b) T_{amb} = 25 °C to T_{amb} = 50 °C
   In both cases the frequency shift is below the specified value.

APPLICATION INFORMATION

DEVELOPMENT DATA



Proposal of VHF/UHF tuner band A = VHF I + VHF III (45 to 300 MHz)
band B = UHF (470 to 900 MHz)

Fig.3 Application diagram.

Component values of the application diagram

resistors

R1 = 47 kΩ	R2 = 18 Ω	R3 = 1.2 kΩ	R4 = 4.7 kΩ
R5 = 100 Ω	R6 = 22 kΩ	R7 = 1 kΩ	R8 = 2.2 kΩ
R9 = 22 kΩ	R10 = 15 kΩ	R11 = 47 kΩ	

capacitors

C1 = 1 nF	C2 = 1 nF	C3 = 1 nF	C4 = 1 nF
C5 = 1 nF	C6 = 1 nF	C7 = 1 nF	C8 = 15 pF (N750)
C9 = 15 pF (N750)	C10 = 1 nF	C11 = 1 nF	C12 = 1 nF
C13 = 0.68 pF (SMD)	C14 = 1 pF (SMD)	C15 = 1 pF (SMD)	
C16 = 0.68 pF (SMD)	C17 = 100 pF (SMD)	C18 = 5.6 pF (SMD)	C19 = 1 pF (NPO)
C20 = 1 pF (NPO)	C21 = 82 pF (N750)	C22 = 1 nF	C23 = 1 nF
C24 = 1 nF	C25 = 1 nF	C26 = 1 μF (40V)	C27 = 1 nF

Cm = 18 pF (N750)

diodes and IC

D1 = BB911	D2 = BA482	D3 = BB405B	IC = TDA5332T

coils

L1 = 2.5 t (ϕ3)	L2 = 8.5 t (ϕ3)	L3 = 1.5 t (ϕ3)
L4 = 1.5 t (ϕ3)	L5 = 2 x 5 t*	L8 = 5 μH (choke coil)

transformer

L6 = 12 t*	L7 = 2 t

wire size for L1 to L4 = 0.4 and for L5 to L7 = 0.1 mm.

* Coil type: TOKO 7 kN; material: 113 kN, screw core (03-0093), pot core (04-0026).

VIDEO MODULATOR CIRCUIT

GENERAL DESCRIPTION

The TDA6800 is a modulator circuit for modulation of video signals on a VHF/UHF carrier. The circuit requires a 5 V power supply and few external components for the negative modulation mode. For positive modulation an external clamp circuit is required. This circuit can be used as a general purpose modulator without additional external components.

Features

- Balanced modulator
- Symmetrical oscillator
- Video clamp circuit for negative modulation
- Frequency range 50 to 800 MHz

QUICK REFERENCE DATA

		min.	typ.	max.	
Supply voltage range	V_{5-4}	4,5	–	5,5	V
Supply current consumption	I_5	–	9	–	mA
Video input voltage	$V_{8(p-p)}$	–	1	–	V
Input impedance	R_8	30	–	–	kΩ
Output voltage (50 MHz)	V_{6-7}	–	13	–	mV
Output voltage (600 MHz)	V_{6-7}	–	10	–	mV
Differential gain	Δ_G	–	–	10	%
Differential phase	Δ_ϕ	–	–	10	deg.
Intermodulation distortion	d_{int}	–	–80	–	dB

PACKAGE OUTLINE

TDA6800 : 8-lead dual in-line; plastic (SOT97A).
TDA6800T: 8-lead mini-pack; plastic (SO8; SOT96A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{5-4}	max.	7 V
Input voltage	V_{8-4}	max.	4 V
Output voltage	$V_{6,7-4}$	max.	9 V
Storage temperature	T_{stg}	max.	125 °C
Junction temperature	T_j	max.	125 °C
Operating ambient temperature range	T_{amb}	−25 to + 85	°C

THERMAL RESISTANCE

From junction to ambient in free air

TDA6800T	$R_{th\ j-a}$	260 K/W
TDA6800	$R_{th\ j-a}$	120 K/W

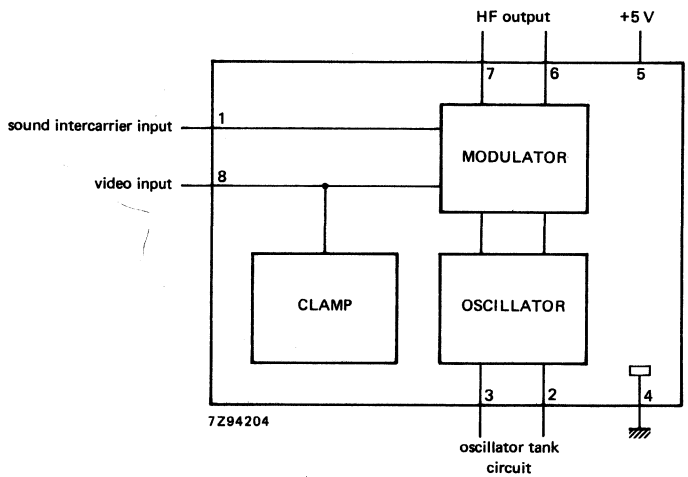


Fig. 1 Block diagram TDA6800 and TDA6800T.

DEVELOPMENT DATA

CHARACTERISTICS

V_P = 5 V; T_{amb} = 25 °C; measured in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage range	V_{5-4}	4,5	–	5,5	V
Supply current consumption	I_5	–	9	13	mA
Video input voltage	$V_{8(p-p)}$	–	1	–	V
Input impedance	R_8	30	–	–	kΩ
Voltage (d.c.) at video input (clamp voltage)	V_8	–	1,4	–	V
Voltage (d.c.) at sound input	V_1	–	2,5	–	V
Output voltage f = 50 MHz; R_L = 75 Ω	V_{6-7}	–	13	–	mV
Output voltage f = 600 MHz; R_L = 75 Ω	V_{6-7}	–	10	–	mV
Differential gain	Δ_G	–	–	10	%
Differential phase	Δ_ϕ	–	–	10	deg.
Intermodulation (1,1 MHz) (note 1)		–	–80	–60	dB
Frequency shift V_b = 5%, f = 600 MHz	Δ_f	–	–	100	kHz
Frequency shift V_b = 5%, f = 800 MHz	Δ_f	–	tbf	–	kHz
Frequency drift 25 to 40 °C	Δ_f	–	–	100	kHz
Frequency drift 15 to 55 °C	Δ_f	–	–	300	kHz
Positive modulation (see Fig. 3)					
Residual carrier voltage	V_r	–	–	2,5	%
Cross modulation (note 2)	α	–	0,1	0,25	%

NOTES TO THE CHARACTERISTICS

1. Input signal: d.c. 0,45 V (V_{8-4} = 1,85 V)
   4,4 MHz; input voltage (p-p) = 0,6 V
   5,5 MHz; input voltage (p-p) = 1,26 V
   measured with respect to picture carrier, at f = 600 MHz.
2. Input signal: d.c. 1 V (V_{8-4} = 3,5 V)
   5,5 MHz AM modulated, f_m = 100 kHz
   m = 0,8; input voltage (p-p) = 2,27 V (including modulation)
   measured with respect to the picture carrier, at f = 600 MHz.

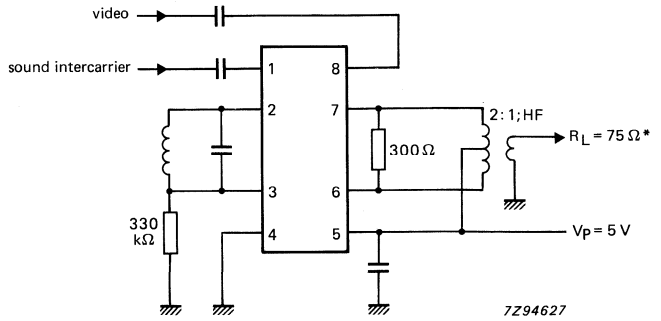


Fig. 2.
Application for negative modulation.

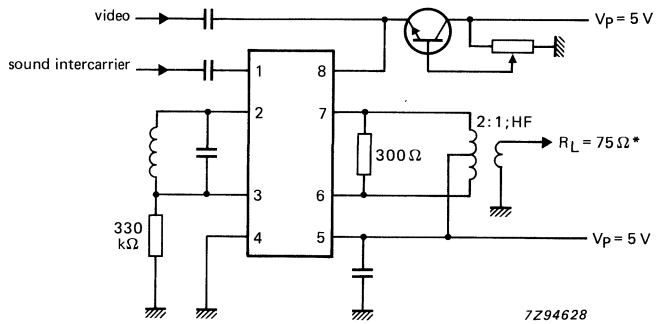


Fig. 3.
Application for positive modulation.

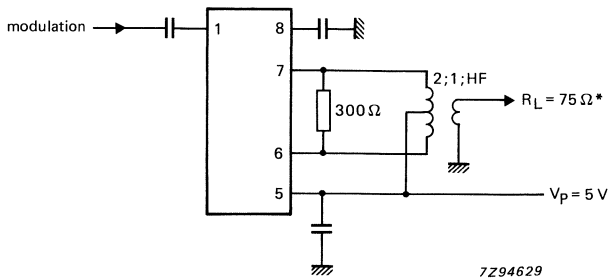


Fig. 4.
Application for general purpose modulation.

* Close to output transformer.

TELEVISION IF AMPLIFIER AND DEMODULATOR

The TDA8340;Q and TDA8341;Q are integrated IF amplifier and demodulator circuits for colour or black/white television receivers, the TDA8340;Q is for application with n-p-n tuners and the TDA8341;Q for p-n-p tuners.

The TDA8340;Q and TDA8341;Q are pin-compatible successors with improved performance to types TDA2540/2541;Q and TDA3540/3541;Q.

Features

- Full range gain-controlled wide-band IF amplifier
- Linear synchronous demodulator with excellent intermodulation performance
- White spot inverter
- Wide-band video amplifier with noise protection
- AFC circuit with AFC on/off switching and sample-and-hold function
- Low impedance AFC output
- AGC circuit with noise gating
- Tuner AGC output for n-p-n tuners (TDA8340) or p-n-p tuners (TDA8341)
- External video switch for switching-off the video output
- Reduced sensitivity for high sound carriers
- Integrated filter to limit second harmonic IF signals
- Wide supply voltage range
- Requires few external components

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 11)		$V_{CC} = V_{11-13}$	9,4	12	13,2	V
Supply current (pin 11)		I_{11}	30	42	55	mA
IF input sensitivity (r.m.s. value)		$V_{1-16(rms)}$	20	40	80	μV
IF gain control range		G_v	–	67	–	dB
Video output voltage (peak-to-peak value)	white signal; 10% top sync	$V_{12-13(p-p)}$	2,4	2,7	3,0	V
Signal-to-noise ratio	V_i = 10 mV	S/(S+N)	50	58	–	dB
AFC output voltage swing (peak-to-peak value)		$V_{5-13(p-p)}$	–	10	–	V

PACKAGE OUTLINES

TDA8340; TDA8341: 16-lead DIL; plastic (SOT38).
TDA8340Q; TDA8341Q: 16-lead QIL; plastic (SOT58).

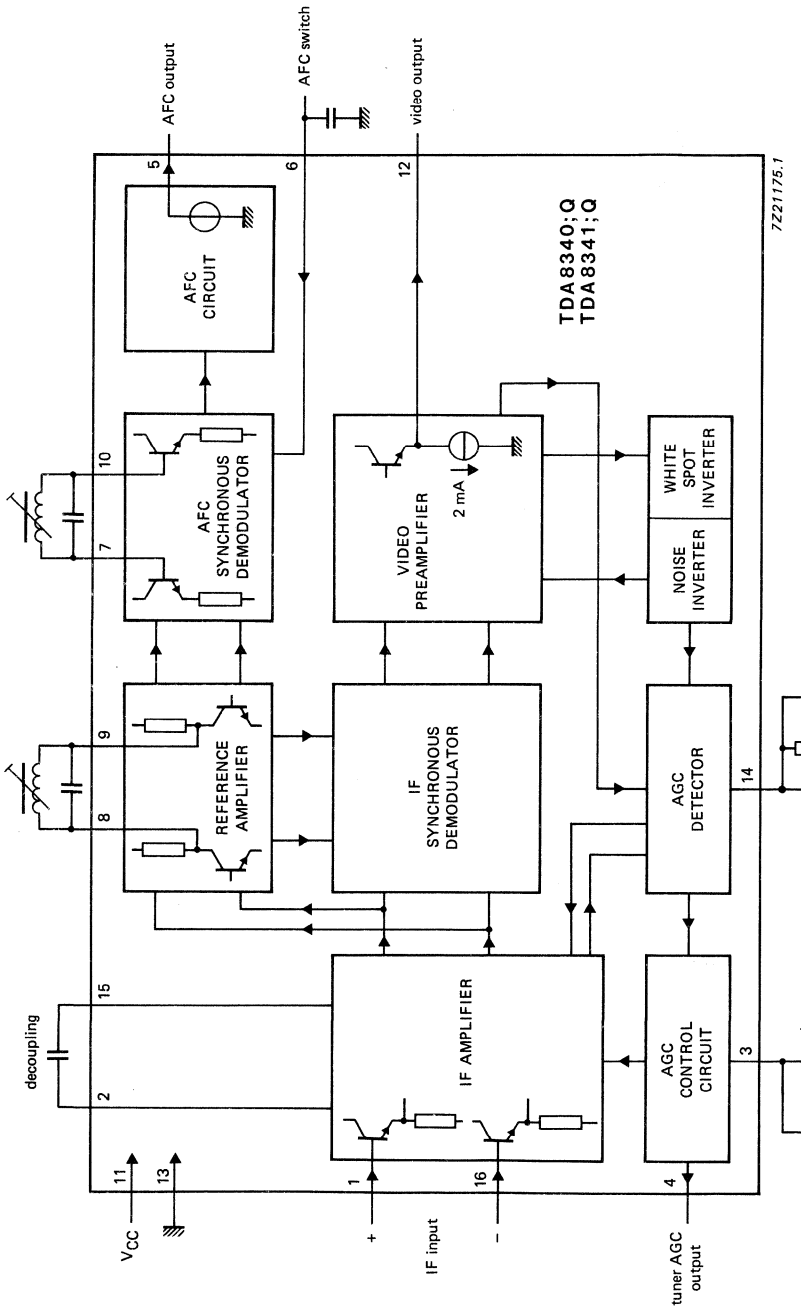


Fig. 1 Block diagram.

PINNING

1 and 16	Balanced IF inputs
2 and 15	IF amplifier decoupling
3	Tuner AGC starting point adjustment
4	Tuner AGC output
5	AFC output
6	AFC on/off switch and sample-and-hold capacitor
7 and 10	Reference carrier $\pi/2$ rad. phase shift
8 and 9	IF picture carrier passive regeneration
11	Positive supply voltage (V_{CC})
12	Video output
13	Ground (V_{EE})
14	IF AGC capacitor and VCR switch

FUNCTIONAL DESCRIPTION

IF amplifier

This is a 3-stage, gain-controlled IF amplifier with a wide dynamic range. On-chip capacitors in the d.c. feedback loop of the amplifier maintain stability at maximum gain. Internal stabilization of the supply voltage ensures the desired sensitivity and gain control range over the whole supply voltage range and also gives very good power supply ripple rejection in this part of the circuit.

DEVELOPMENT DATA

Demodulator

The redesigned IF demodulator is a quasi-synchronous circuit that employs passive carrier regeneration and logarithmic clamping to give improved signal handling. The demodulator input is a.c. coupled to the IF amplifier to reduce d.c. offsets and thus minimize residual IF carrier in the output signal.

Video amplifier

The linearity and bandwith of the video amplifier are sufficient to meet all wide band requirements, e.g. for teletext transmissions. Second harmonics of the IF carrier are effectively reduced by a Sallen-Key low pass interstage filter between the demodulator output and the video amplifier input. An integrated filter in the noise inverter reduces the sensitivity of the video amplifier for high sound carriers.

White spot protection comprises a white spot clamp system combined with a delayed-action inverter which is also highly resistant to high sound carriers.

Note. To prevent radiated video output at the input pins, connect a 6,8 μH inductor in series with pin 12 and fit as close as possible to the IC body. Use short leads.

AGC dectector

A Bessel low-pass filter between the video output and the AGC detector improves the detector function in the presence of high sound carriers. No 'hang-up' occurs in the detector after pin 14 has been short-circuited to ground (VCR switch operated). The detector also generates the sample-and-hold pulse for the AFC system.

AGC control circuit

This converts the AGC detector voltage (pin 14) into a current signal which controls the gain of the IF amplifier. It also provides a tuner AGC control output from pin 4, current limiting is incorporated to prevent internal damage. The AGC starting point is adjusted via pin 3.

FUNCTIONAL DESCRIPTION (continued)

AFC circuit

The AFC circuit provides a voltage output which controls the IF frequency of the tuner. Video information on the AFC output (pin 5) is eliminated by a sample-and-hold circuit (external capacitor at pin 6). Coupling between the AFC and reference tuned circuits is via two small capacitors (or parasitic capacitance) between the respective tracks of the printed circuit board. If the capacitance is less than 1 pF, the steepness of the AFC characteristic is reduced.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 11)	$V_{CC} = V_{11-13}$	9,4	13,2	V
IF AGC voltage/VCR switch	V_{14-13}	–	13,2	V
Tuner AGC voltage	V_{4-13}	–	12	V
AFC switch voltage	V_{6-13}	–	13,2	V
Maximum voltage level with VCR switch active	V_{12-13}	–	5,0	V
DC current at video output	I_{12}	–	10	mA
DC current at AFC output	I_5	–	10	mA
Total power dissipation	P_{tot}	–	1,2	W
Storage temperature range	T_{stg}	–65	+150	°C
Operating ambient temperature	T_{amb}	–25	+70	°C

DEVELOPMENT DATA

CHARACTERISTICS

Measured in circuit of Fig. 3; V_{CC} = 12 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 11)		$V_{CC} = V_{11-13}$	9,4	12	13,2	V
Supply current	no input signal	I_{11}	30	42	55	mA
IF amplifier (note 1)						
Input sensitivity	at onset of AGC	V_{1-16}	20	40	80	μV
Differential input resistance		R_{1-16}	–	2	–	kΩ
Differential input capacitance		C_{1-16}	–	3	–	pF
Gain control range		G_v	–	67	–	dB
Input signal variation	note 2	V_{12-13}	–	–	0,5	dB
Maximum input signal		V_{1-16}	100	–	–	mV
Tuner AGC (note 1)						
Tuner AGC starting point (note 3)	R_{3-11} = 39 kΩ R_{3-13} = 39 kΩ	V_{1-16} V_{1-16}	– 70	– –	3 –	mV mV
Maximum current swing of tuner AGC output		I_4	10	–	–	mA
Input signal variation	note 4; I_4 = 1 to 9 mA	V_{1-16}	–	–	3	dB
Output saturation voltage	I_4 = 7 mA	V_{4-13}	–	200	300	mV
Leakage current	V_4 = 12 V	I_4	–	–	1	μA
Video output (note 4)						
Zero-signal output level	note 5	V_{12-13}	5,7	6,0	6,3	V
Top sync output level		V_{12-13}	2,8	3,0	3,2	V
Video output voltage (peak-to-peak value)	white signal; 10% top sync	$V_{12-13(p-p)}$	2,4	2,7	3,0	V
Internal bias current of emitter follower output transistor			1,4	2,2	3,0	mA
Output impedance		Z_{12}	–	100	–	Ω
Bandwith of demodulated output signal		B	6	7,5	–	MHz
Differential gain	note 6	G_d	–	2	5	%
Differential phase	note 6	φ_d	–	2	5	deg
Luminance non-linearity	note 7		–	2	5	%
Residual carrier signal (r.m.s. value)	note 8	$V_{12-13(rms)}$	–	2	10	mV

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Video output (continued)						
Residual 2nd harmonic of carrier signal (r.m.s. value)	note 8	$V_{12\text{-}13(rms}$	–	2	10	mV
Variation of video voltage for ΔV_{CC} = 1 V		$\frac{\Delta V_{12\text{-}13(p\text{-}p)}}{\Delta V_{11\text{-}13}}$	0,1	0,2	0,3	
Intermodulation	notes 8 and 9;					
	1,1 MHz, blue	α	–	–65	–60	dB
	1,1 MHz, yellow	α	–	–60	–56	dB
	3,3 MHz	α	–	–	–68	dB
Signal-to-noise ratio	note 10;					
	V_i = 10 mV	S/(S+N)	50	58	–	dB
	max. gain	S/(S+N)	54	61	–	dB
Spot inverter (note 11)						
Threshold level		$V_{12\text{-}13}$	6,3	6,8	7,3	V
Insertion level		$V_{12\text{-}13}$	4,2	4,5	4,8	V
Noise inverter (note 11)						
Threshold level		$V_{12\text{-}13}$	1,6	1,8	2,0	V
Insertion level		$V_{12\text{-}13}$	3,5	3,8	4,1	V
VCR switch						
Level below which video output switches off		$V_{14\text{-}13}$	1,8	2,2	2,6	V
Switch current	$V_{12\text{-}13}$ = 0,7 V	$-I_{14}$	40	60	100	μA
AFC circuit (note 12)						
Output voltage swing (peak-to-peak value)		$V_{5\text{-}13(p\text{-}p)}$	–	10	–	V
Change of frequency for an AFC output voltage swing of 10 V		Δf	–	60	120	kHz
AFC output voltage	at f = 38,9 MHz	$V_{5\text{-}13}$	–	6	–	V
	no input signal	$V_{5\text{-}13}$	2	6	10	V
	during AFC off	$V_{5\text{-}13}$	5	6	7	V
AFC output resistance		$R_{5\text{-}13}$	–	500	–	Ω
AFC switch: level below which AFC output switches off		$V_{6\text{-}13}$	1,4	2,0	2,8	V
AFC switch current	during AFC on	I_6	–	200	500	μA
Max. AFC switch current	during AFC off;					
	$V_{6\text{-}13}$ = 0 V	I_6	–	–	5	mA

Notes to the characteristics

1. All input signals are measured r.m.s. at top sync and 38,9 MHz.
2. Measured with 0 dB = 200 μV.
3. Tuner AGC starting point is defined as 'level of input signal when tuner AGC current = 1 mA'.
4. Measured with pin 3 connected via 39 kΩ resistor to V_{CC} (pin 11), with an r.m.s. voltage of 10 mV top sync input signal and with pin 12 not loaded.
5. At the 'projected zero point', e.g. with switched demodulator.
6. Measured in the circuit of Fig. 7:

   the differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier amplitude at blanking level;

   the differential phase is defined as 'the difference (in degrees) between the largest and smallest phase angles'.
7. Measured according to the test line shown in Fig. 9:

   the non-linearity is expressed as a percentage of the maximum deviation of a luminance step from the mean step, with respect to the mean step;

   the mean step is (white level — black level) divided by the number of steps.
8. Measured up to 45 dB gain control.
9. Test set-up and input conditions for intermodulation measurements as in Figs 6 and 7.
10. Measured with a 75 Ω source:

$$S/(S+N) = 20 \log \frac{V_{\text{out black to white}}}{V_{n(rms)} \text{ at } B = 5 \text{ MHz}}.$$

11. Video output waveform showing white spot and noise inverter threshold levels.
12. Measured with input signal $V_{1\text{-}16}$ = 10 mV and with no load at AFC output.

DEVELOPMENT DATA

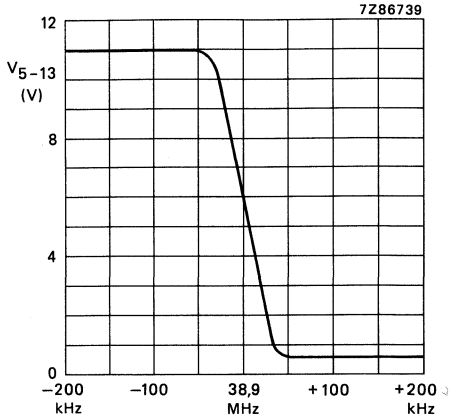


Fig. 2 AFC output voltage as a function of frequency.

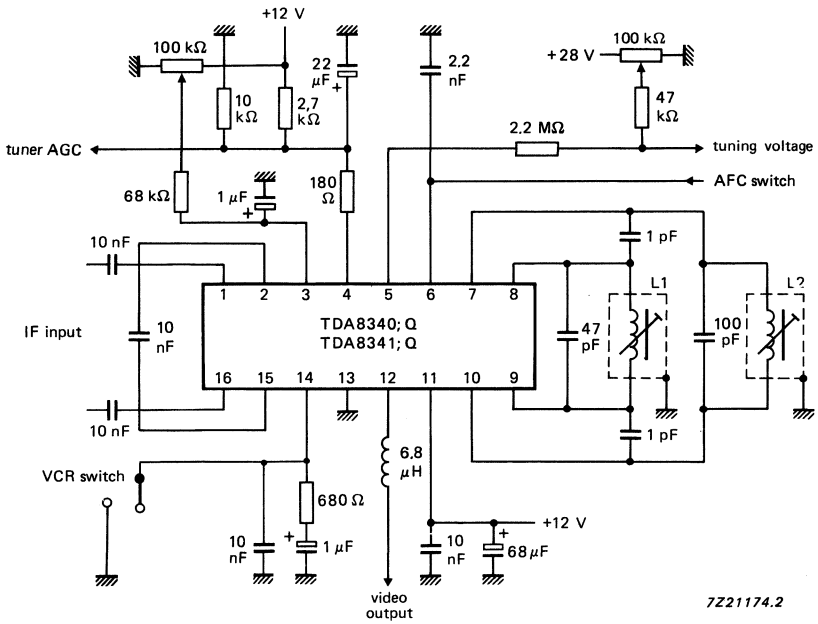


Fig. 3 Typical application circuit diagram;
Q of L1 and L2 = 80; f_o = 38,9 MHz.

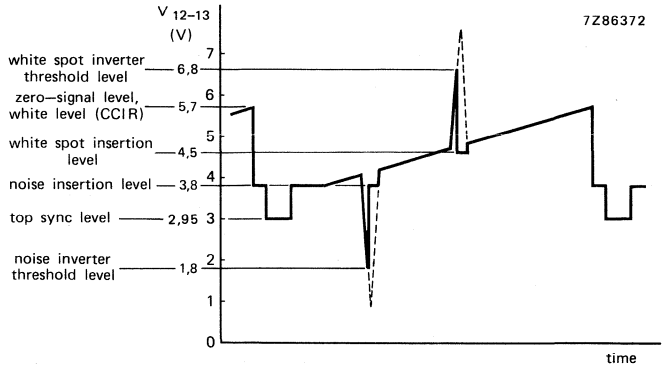


Fig. 4 Video output waveform showing white spot and noise inverter threshold levels.

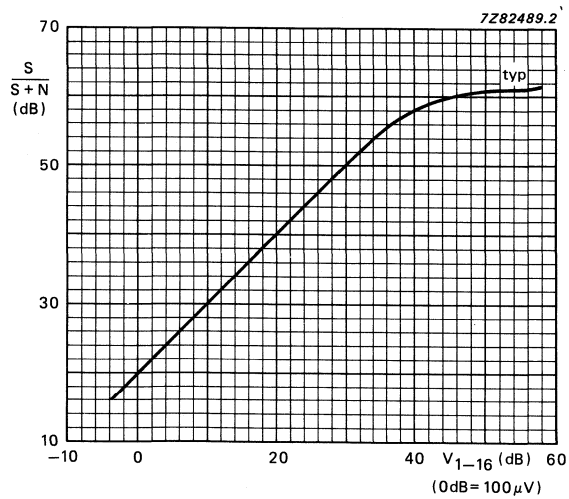
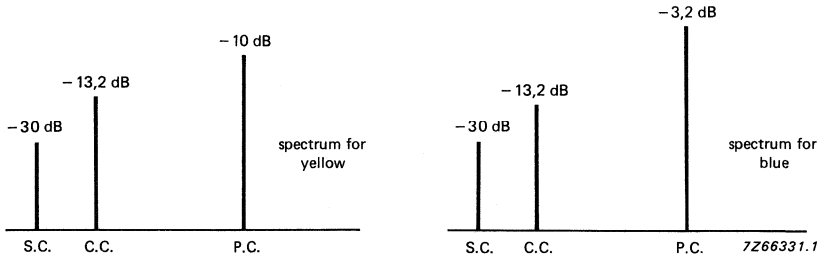


Fig. 5 Signal-to-noise ratio as a function of input voltage.



S.C.: sound carrier level
C.C.: chrominance carrier level
P.C.: picture carrier level
} with respect to top sync level

Fig. 6 Input conditions for intermodulation measurements; standard colour bar with 75% contrast.

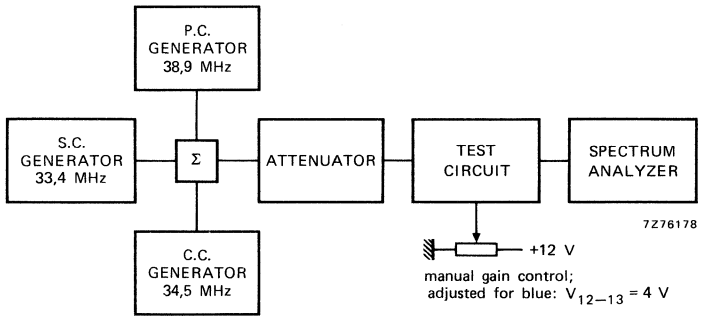


Fig. 7 Test set-up for intermodulation measurements.

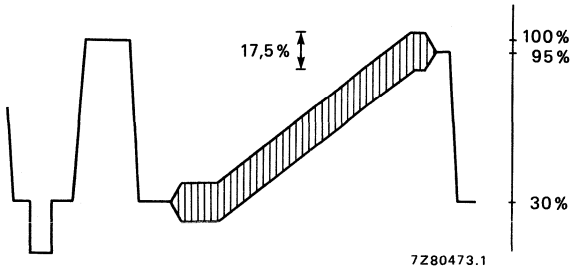


Fig. 8 Video output signal.

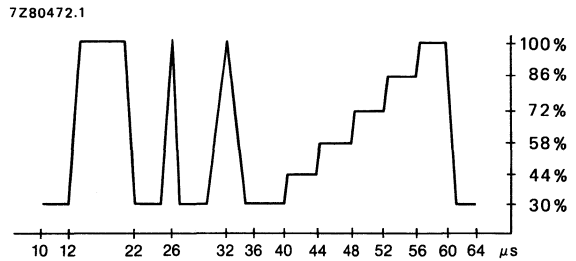


Fig. 9 E.B.U. test signal waveform (line 330).

SYNCHRONIZATION PROCESSOR FOR TELEVISION RECEIVERS

GENERAL DESCRIPTION

The TDA8370 is a sync processor designed to generate and synchronize horizontal and vertical signals in medium and high performance television receivers. The device is particularly suitable for application with teletext decoders and video tape recorders.

A video switch controlled by I^2C bus command or analogue switched voltage selects internal or external composite video signals.
The processing of not line-locked vertical sync in non-standard mode is also possible.

Features

- Two separate video inputs adapted to:
  I.F. detector (front-end output)
  or
  peri-television connector selected by the video switch
- Buffered video output
- Horizontal sync separator with self-aligning levels
- Vertical sync separator 1 with self-aligning levels when standard mode selected
- Vertical sync separator 2 with self-aligning levels when non-standard mode selected (e.g. video tape recorder signal)
- Noise invertor
- Gated phase discriminator with switchable time constant for non-standard applications
- 6 MHz VCO for generation of clock signal for teletext display
- Noise level detector
- Automatic low-current starting circuit
- φ 2 phase control with shift adjustment not affecting gain or time constant
- Horizontal output optimized for operation with self-oscillating power supply
- Vertical divider system with automatic selection of 625 or 525 standard
- 50/60 Hz identification output voltage
- Mute output
- Coincidence detector
- Vertical shaping and feedback system with automatic 60 Hz amplitude correction
- 3-level sandcastle output
- Vertical guard circuit active via sandcastle output
- Scan composite sync ($\overline{\text{S.C.S.}}$) output as slave input for teletext decoder
- Special "sense" ground pin to ensure correct feedback voltage in the frame deflection circuit
- I^2C bus controlled teletext non-interlaced signal (N.I.L.)
- Line and frame frequencies switched to nominal when noise only is received in standard mode

PACKAGE OUTLINES

28-lead DIL; plastic (SOT117).

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 22)	V_P	10	12	13,2	V
Supply current (pin 22)	I_P	–	125	150	mA
Starting current (pin 23)	I_{23}	5	5,5	10	mA
Video input voltage (positive video)					
pin 1 (peak-to-peak value)	$V_{1\text{-}20(p\text{-}p)}$	–	2,25	3	V
pin 5 (peak-to-peak value)	$V_{5\text{-}20(p\text{-}p)}$	–	1	1,4	V
Horizontal flyback input current (pin 18)	I_{18}	0,3	1	4	mA
Vertical comparator input (pin 14)					
a.c. input voltage (peak-to-peak value)	$V_{14\text{-}20(p\text{-}p)}$	–	3	–	V
d.c. input voltage	$V_{14\text{-}20}$	–	2,5	–	V
I^2C clock input/analogue input (pin 7)					
analogue video switching voltage level	$V_{7\text{-}20}$	6,5	–	7,5	V
I^2C data input/analogue input (pin 8) for selecting peri-television connector input					
analogue switching voltage level for selecting non-standard mode (equal to V.T.R.)	$V_{8\text{-}20}$	6,5	–	7,5	V
Max. horizontal output voltage (pin 17)	$V_{17\text{-}20}$	14	–	16	V
Max. vertical drive output voltage (pin 13)	$V_{13\text{-}20}$	–	–	10	V
Sandcastle 3-level output voltage (pin 9)					
burstkey	$V_{9\text{-}20}$	–	10,8	–	V
horizontal blanking	$V_{9\text{-}20}$	4,1	4,4	4,9	V
vertical blanking	$V_{9\text{-}20}$	2,1	2,6	2,9	V
Scan composite sync output (pin 10)					
high output voltage at $-I_{10} = 5$ mA	$V_{10\text{-}20}$	4,3	4,8	5,3	V
output current	$-I_{10}$	–	1	–	mA
Video output (pin 3)					
a.c. output voltage (peak-to-peak value)	$V_{3\text{-}20(p\text{-}p)}$	2,6	3	3,4	V
d.c. level top sync	$V_{3\text{-}20}$	2,8	3,2	3,7	V
50/60 Hz identification output voltage (pin 4)					
50 Hz at $I_4 = 0,1$ mA	$V_{4\text{-}20}$	–	1,3	1,7	V
60 Hz at $-I_4 = 5$ mA	$V_{4\text{-}20}$	8	10	–	V
output current	$-I_4$	–	–	5	mA
Mute output voltage (pin 28)					
in-sync at $I_{28} = 0,1$ mA	$V_{28\text{-}20}$	–	1,2	1,5	V
out-of-sync/no sync at $-I_{28} = 0,5$ mA	$V_{28\text{-}20}$	–	10,5	–	V

DEVELOPMENT DATA

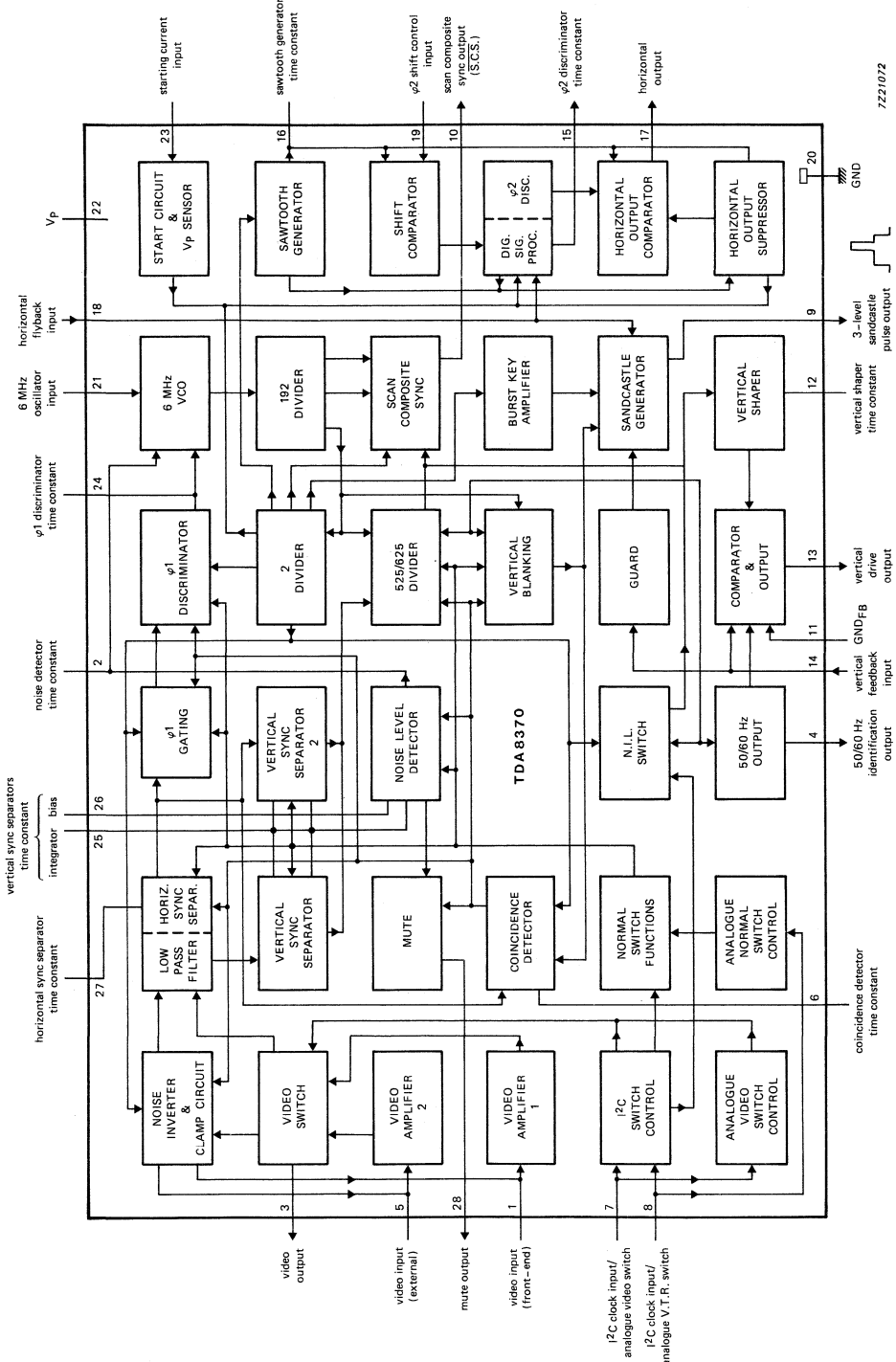


Fig. 1 Block diagram.

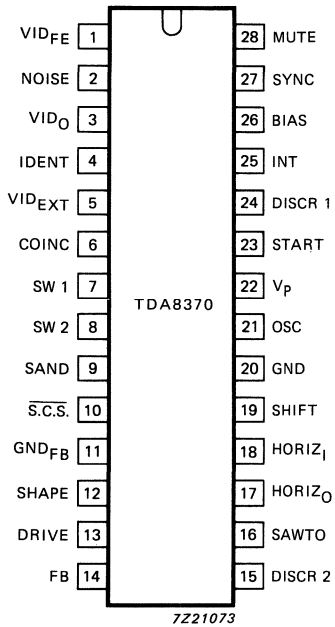


Fig. 2 Pinning diagram.

PINNING

1	VID_{FE}	video input (front-end)
2	NOISE	noise detector time constant
3	VID_O	video output
4	IDENT	50/60 Hz identification output
5	VID_{EXT}	video input (external)
6	COINC	coincidence detector time constant
7	SW 1	I^2C clock input/analogue video switch
8	SW 2	I^2C data input/analogue V.T.R. switch
9	SAND	3-level sandcastle pulse output
10	$\overline{S.C.S.}$	scan composite sync output
11	GND_{FB}	ground feedback input
12	SHAPE	vertical shaper time constant
13	DRIVE	vertical drive output
14	FB	vertical feedback input
15	DISCR 2	φ 2 discriminator time constant
16	SAWTO	sawtooth generator time constant
17	$HORIZ_O$	horizontal output
18	$HORIZ_I$	horizontal flyback input
19	SHIFT	φ 2 shift control input
20	GND	ground
21	OSC	6 MHz oscillator time constant
22	V_P	positive supply voltage
23	START	starting current input
24	DISCR 1	φ 1 discriminator time constant
25	INT	integrator time constant vertical sync separators
26	BIAS	time constant bias vertical sync separators
27	SYNC	horizontal sync separator time constant
28	MUTE	mute output

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 22)	V_P	max.	13,2	V
Starting current (pin 23)	I_{23}	max.	10	mA
Power dissipation	P_{tot}	max.	2	W
Storage temperature range	T_{stg}		−25 to + 150	°C
Operating ambient temperature range	T_{amb}		0 to + 70	°C
Thermal resistance				
From junction to ambient (in free)	$R_{th\ j\ a}$	=	40	K/W
Operating junction temperature	T_j	max.	150	°C

DEVELOPMENT DATA

CHARACTERISTICS

V_P = 12 V; I_{23} = 5,5 mA; 6 MHz clock oscillator operating at nominal frequency; synchronized; T_{amb} = 25 °C; measured in test set-up Fig. 6; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 22)	V_P	10	12	13,2	V
Supply current (pin 22)	I_P	–	125	150	mA
Starting current (pin 23)	I_{23}	5,0	5,5	10	mA
Video input (pin 1)					
A.C. coupled input voltage positive video (peak-to-peak value)	$V_{1\text{-}20(p\text{-}p)}$	–	2,25	3,0	V
D.C. level top sync	$V_{1\text{-}20}$	5,0	5,5	6,5	V
Input impedance	$\lvert Z_{1\text{-}20}\rvert$	–	20	–	kΩ
Generator resistance	R_G	–	75	150	Ω
Allowable sync compression *		20	–	–	dB
Video input (pin 5)					
A.C. coupled input voltage positive video (peak-to-peak value)	$V_{5\text{-}20(p\text{-}p)}$	–	1,0	1,4	V
D.C. level top sync	$V_{5\text{-}20}$	3,5	4,2	4,9	V
Input impedance	$\lvert Z_{5\text{-}20}\rvert$	–	20	–	kΩ
Generator resistance	R_G	–	75	150	Ω
Allowable sync compression		20	–	–	dB
Video output (pin 3)					
Output voltage** positive video (peak-to-peak value)	$V_{3\text{-}20(p\text{-}p)}$	2,7	3,0	3,3	V
D.C. level top sync	$V_{3\text{-}20}$	2,8	3,2	3,7	V
Resistance npn emitter follower	$R_{3\text{-}20}$	–	–	50	Ω
Bandwidth at $-I_3$ = 5 mA	B	10	15	–	MHz
Crosstalk between video signals pin 1 or pin 5 to pin 3		–	–	–54	dB
Noise inversion threshold level	$V_{3\text{-}20}$	1,9	2,1	2,3	V

* When not selected the negative-going input voltage is clamped at 0 V.

** Measured at $V_{1\text{-}20(p\text{-}p)}$ = 2,25 V or $V_{5\text{-}20(p\text{-}p)}$ = 1 V.

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Horizontal sync separator (pin 27)					
D.C. voltage level	$V_{27\text{-}20}$	–	6,2	–	V
Line ripple voltage (peak-to-peak value)					
during standard mode	$V_{27\text{-}20}$	–	2,8	–	mV
during non-standard mode	$V_{27\text{-}20}$	–	0,6	–	mV
φ **1 discriminator** (pin 24)					
Catching range	$\pm \Delta f$	600	1000	1400	Hz
Holding range	$\pm \Delta f$	*	1000	1200	Hz
Phase shift		–	0,5	–	μs/kHz
Input resistance during sync pulse					
with slow time constant	$R_{24\text{-}20}$	–	12,6	–	kΩ
with fast time constant	$R_{24\text{-}20}$	–	2,2	–	kΩ
6 MHz VCO (pin 21)					
Output frequency free running at $V_{2\text{-}20} > 7$ V	f_o	–	6	–	MHz
Frequency variation without tolerance of external components	Δf_o	–	–	± 4	%
Frequency variation as a function of supply voltage	$\Delta f_o/\Delta V_p$	–	–	0,01	
Temperature coefficient of oscillator frequency	TC_{osc}	–	1400	–	Hz/K
A.C. input voltage (peak-to-peak value)	$V_{21\text{-}20(p\text{-}p)}$	–	0,3	–	V
D.C. input voltage	$V_{21\text{-}20}$	–	1,6	–	V
Sawtooth generator (pin 16)					
Start of negative slope of sawtooth	$V_{16\text{-}20}$	–	7,2	–	V
Start flyback of sawtooth	$V_{16\text{-}20}$	–	3,7	–	V
φ 2 trigger pulse width (see Fig. 3)	t_W	–	6,8	–	μs
φ 2 loop not synchronized by φ 1 loop					
Start of negative slope of sawtooth	$V_{16\text{-}20}$	–	7,2	–	V
Start flyback of sawtooth	$V_{16\text{-}20}$	–	3,4	–	V
Flyback time (see Fig. 3)	t_{fb}	0,9	1,3	1,7	μs
Output frequency free running at $V_p = 8{,}5$ V	f_o	–	15,4	–	kHz
Frequency variation without tolerance of external components	Δf_o	–	–	± 4	%

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Horizontal output (pin 17)					
Output current open collector npn; V_{17-20} = 0,5 V	I_{17}	–	–	10	mA
Output voltage protection (2 internal zener diodes)	V_{17-20}	14	–	16	V
Maximum output current during voltage protection	I_{17}	–	0	1	mA
Delay between start of sawtooth output pulse at pin 16 and:					
negative-going edge of horizontal output voltage (see Fig. 3)	t_{d1}	14,5	16	17,5	μs
positive-going control edge of horizontal output voltage (see Fig. 3)	$t_{d2(min.)}$	25	28	31	μs
	$t_{d2(max.)}$	–	T_H	–	μs
	t_{d2}*	–	T_H	–	μs
Condition: I_{23} = 5 to 10 mA					
Horizontal output pulse present if:	V_{23-20}	–	–	6	V
Horizontal output pulse not present if:	V_{23-20}	4	–	–	V
and	I_{23}	3	–	–	mA
δ Horizontal output is a function of the input voltage at pin 23					
δ = 0	V_{23-20}	–	–	4	V
δ = maximum	V_{23-20}	8,5	–	–	V
Horizontal output suppression time	t_s	20	22	24	μs
φ 2 discriminator (pin 15)					
Control current	$\pm I_{15}$	600	800	1000	μA
Control sensitivity	$\Delta\varphi_i/\Delta\varphi_o$	–	400	–	
Input current at V_{15-20} = 4 V; V_P = 0 V	I_{15}	–	–	0,6	μA
Condition:					
No flyback pulse and $V_{23-20} > 5$ V					
Output voltage at pin 15	V_{15-20}	2,7	3	3,3	V
Condition: $V_P < 8,9$ V					
Output voltage at pin 15	V_{15-20}	2,7	3	3,3	V

* Delay with no horizontal flyback pulse present at pin 18.

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
φ 2 shift control input (pin 19)					
Shift control range		–	$1/16T_H+\Delta$	–	μs
Δ		0,2	–	1	μs
Delay between rising edge of horizontal flyback at the slicing level and rising edge of burst key pulse (see Fig. 2)	$t_{d3(min.)}$	–	3	–	μs
	$t_{d3(max.)}$	–	$7+\Delta$	–	μs
t_{d3} = min. when:	V_{19-20}	–	–	4,5	V
t_{d3} = max. when:	V_{19-20}	0	–	–	V
Shift control is active when:	V_{22-20}	$>8,9$	$>9,5$	>10	V
Starting control input (pin 23)					
Starting by current to pin 23: minimum	I_{23}	3	–	5	mA
maximum allowed	I_{23}	–	–	10	mA
Starting by a voltage on pin 22: required input current	I_{23}	0	–	10	mA
Stabilized voltage	V_{23-20}	8,2	8,7	9,2	V
Supply current is added to starting current if: $V_P > V_{23-20}$ and $V_{23-20} < 8,5$ V	V_{23-20}	–	V_P-V_{BE}	–	V
Horizontal flyback input (pin 18)					
Slicing level input voltage	V_{18-20}	0,7	0,9	1,1	V
Input current	I_{18}	0,3	1	4	mA
Maximum input current	$-I_{18}$	–	–	1	mA
Maximum input voltage	V_{18-20}	–	–	V_P	V
Vertical sync separator integrator time constant (pin 25)					
Condition: Standard mode					
D.C. voltage level of vertical sync top of integrated video	V_{25-20}	8,5	9,0	9,5	V
black level of integrated video during vertical blanking	V_{25-20}	4,0	4,5	5,0	V
Input resistance	R_{25-20}	–	5,1	–	kΩ
Condition: Non-standard mode					
Input voltage level of integrated vertical sync top level	V_{25-20}	9,5	10,7	11,0	V
integrated vertical sync amplitude (peak-to-peak value)	$V_{25-20(p-p)}$	–	8,9	–	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Vertical sync separator biasing (pin 26)					
Input voltage in standard mode	V_{26-20}	–	5,9	–	V
Input voltage in non-standard mode	V_{26-20}	–	8,4	–	V
Vertical shaper (pin 12)					
Condition: 50 Hz					
Ramp voltage starting level	V_{12-20}	–	2	–	V
Flyback voltage starting level	V_{12-20}	6,0	6,25	6,5	V
Condition: 60 Hz					
Ramp voltage starting level	V_{12-20}	–	2	–	V
Flyback voltage starting level	V_{12-20}	5,35	5,6	5,85	V
Flyback time (normal)	t_{fb}	170	220	270	μs
Flyback time controlled by second half of N.I.L. signal		–	$t_{fb}-32$	–	μs
Vertical drive output (pin 13)					
Open collector pnp					
Maximum output current at V_{13-20} = 8 V	$-I_{13}$	3	–	–	mA
Output voltage LOW with 100 kΩ resistor to ground	V_{13-20}	–	–	300	mV
Vertical feedback input (pin 14)					
A.C. input voltage not synchronized					
50 and 60 Hz condition: non-standard mode input voltage (peak-to-peak value)	$V_{14-11(p-p)}$	–	3	–	V
d.c. average input voltage	V_{14-11}	–	2,8	–	V
Parabolic pre-correction convex (50 Hz)		–	4	–	%
Parabolic pre-correction convex (60 Hz)		–	3,3	–	%
Guard circuit input					
input voltage HIGH	V_{14-11}	5,3	5,7	6,1	V
input voltage LOW	V_{14-11}	–	–	0	V
input voltage at V_{14-20} = 2,5 V	$-I_{14}$	–	1,5	6,1	μA
Ground feedback input (pin 11)					
A.C. feedback voltage	V_{11-20}	–	0	–	V

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
50/60 Hz identification output (pin 4)					
50 Hz output voltage at I_4 = 0,1 mA	V_{4-20}	–	1,3	1,7	V
60 Hz output voltage at $-I_4$ = 5 mA	V_{4-20}	8	10	–	V
3-level sandcastle output (pin 9)					
Output voltage during burst key at $-I_9$ = 0,5 mA	V_{9-20}	–	10,8	–	V
at $-I_9$ = 5 mA	V_{9-20}	8,0	9,7	–	V
Output voltage during horizontal blanking at $-I_9$ = 0,5 mA	V_{9-20}	4,1	4,4	4,9	V
Output voltage during vertical blanking at $-I_9$ = 0,5 mA	V_{9-20}	2,1	2,6	2,9	V
Zero level output voltage at I_9 = 0,5 mA	V_{9-20}	–	0,25	0,5	V
Pulse width: burst key at V_{9-20} = 7 V	t_W	3,7	4,0	4,3	μs
horizontal blanking at V_{9-20} = 3,5 V	t_W	–	*	–	
Vertical blanking (see Fig. 4)					
Condition: 50 Hz direct synchronization					
Start of vertical blanking with respect to start of vertical sync, dependent on integration at pin 25	t_{bk}	–	16	–	μs
Duration of vertical blanking	t_d	–	$22{,}5T_H - t_{bk}$	–	μs
Condition: 50 Hz indirect synchronization					
Start of vertical blanking with respect to start of vertical sync	t_{bk}	–	$-(2{,}5T_H + 20\ \mu s)$	–	
Duration of vertical blanking	t_d	–	$25T_H + 2\ \mu s$	–	
Condition: 60 Hz direct synchronization					
Start of vertical blanking with respect to start of vertical sync, dependent on integration at pin 25	t_{bk}	–	16	–	μs
Duration of vertical blanking	t_d	–	$18{,}5T_H - t_{bk}$	–	μs
Condition: 60 Hz indirect synchronization					
Start of vertical blanking with respect to start of vertical sync	t_{bk}	–	0	–	μs
Duration of vertical blanking	t_d	–	$18{,}5T_H$	–	μs
Phase position of burst key delay between the middle of the sync pulse on the video input and the rising edge of the burst key pulse at a slicing level of 7 V		2,5	2,9	3,3	μs

* Width of horizontal flyback on pin 18 pulse at the slicing level.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
$\overline{\text{S.C.S.}}$ output (pin 10)					
Output voltage HIGH at $-I_{10}$ = 5 mA	$V_{10\text{-}20}$	4,3	4,8	5,3	V
Output voltage LOW at I_{10} = 0,5 mA	$V_{10\text{-}20}$	–	0,2	0,5	V
Conditions:*					
Noise only on video input pin 1 or 5 or indirect sync 50 Hz with a 4,7 μs horizontal sync pulse width on pin 1 or 5					
Delay between the starting edge of the horizontal sync pulse of the video input signal and the starting edge of the horizontal sync pulse in the $\overline{\text{S.C.S.}}$ signal		–0,25	0	0,25	μs
Noise detector time constant (pin 2)					
Condition: Standard mode					
Output voltage					
strong signal	$V_{2\text{-}20}$	–	4,6	5,3	V
noise only**	$V_{2\text{-}20}$	–	7,2	–	V
Switching voltage level					
strong signal → noise only	$V_{2\text{-}20}$	5,7	6,2	6,7	V
noise only → strong signal	$V_{2\text{-}20}$	–	5,6	–	V
Coincidence detector (pin 6)					
Average voltage level					
in-sync	$V_{6\text{-}20}$	6,8	8	–	V
out-of-sync	$V_{6\text{-}20}$	–	–	2,1	V
noise only	$V_{6\text{-}20}$	–	–	2,4	V
Switching voltage level (see also Fig. 5)					
fast → normal$^{\Delta}$	$V_{6\text{-}20}$	–	4,4	–	V
normal → fast$^{\Delta}$	$V_{6\text{-}20}$	–	2,4	–	V

* All other conditions will cause distorted vertical sync pulses and/or equalizing pulses in the $\overline{\text{S.C.S.}}$ signal.

** When noise only is received the 6 MHz oscillator is switched to nominal frequency and the frame divider to the 625 standard.

Δ This switching level is also valid for clamp gating, φ 1 gating, muting, frame divider indirect/direct sync, horizontal sync separator gated/self-aligned and noise detector inhibit/inhibit off.

parameter	symbol	min.	typ.	max.	unit
Mute output (pin 28)					
Output voltage					
not synchronized					
at $-I_{28}$ = 0,5 mA	V_{28-20}	–	10,5	–	V
at $-I_{28}$ = 5 mA	V_{28-20}	7,0	8,5	–	V
synchronized					
at I_{28} = 0,1 mA	V_{28-20}	–	1,2	1,5	V
I^2C clock input/ analogue input video switch (pin 7)					
Input voltage					
analogue input inactive	V_{7-20}	5	–	–	V
analogue input switching level (external video selected)	V_{7-20}	6,5	–	7,5	V
Input current					
at V_P = 0 V	$\|I_7\|$	–	–	10	μA
at V_P = 12 V	$-I_7$	–	–	10	μA
I^2C clock input switching voltage level	V_{7-20}	1,5	2,6	3,0	V
I^2C data input/ * analogue V.T.R. switch (pin 8)					
Input voltage					
analogue input inactive	V_{8-20}	5	–	–	V
analogue input switching level (non-standard mode)	V_{8-20}	6,5	–	7,5	V
Input current					
at V_P = 0 V	$\|I_8\|$	–	–	10	μA
at V_P = 12 V	$-I_8$	–	–	10	μA
I^2C data input switching voltage level	V_{8-20}	1,5	2,6	3,0	V
During acknowledge					
pull-down current	$-I_8$	–	–	5	mA
saturation voltage	V_{8-20}	–	–	1,5	V

DEVELOPMENT DATA

* For address and data byte definition see Fig. 6 and Table 1 respectively.

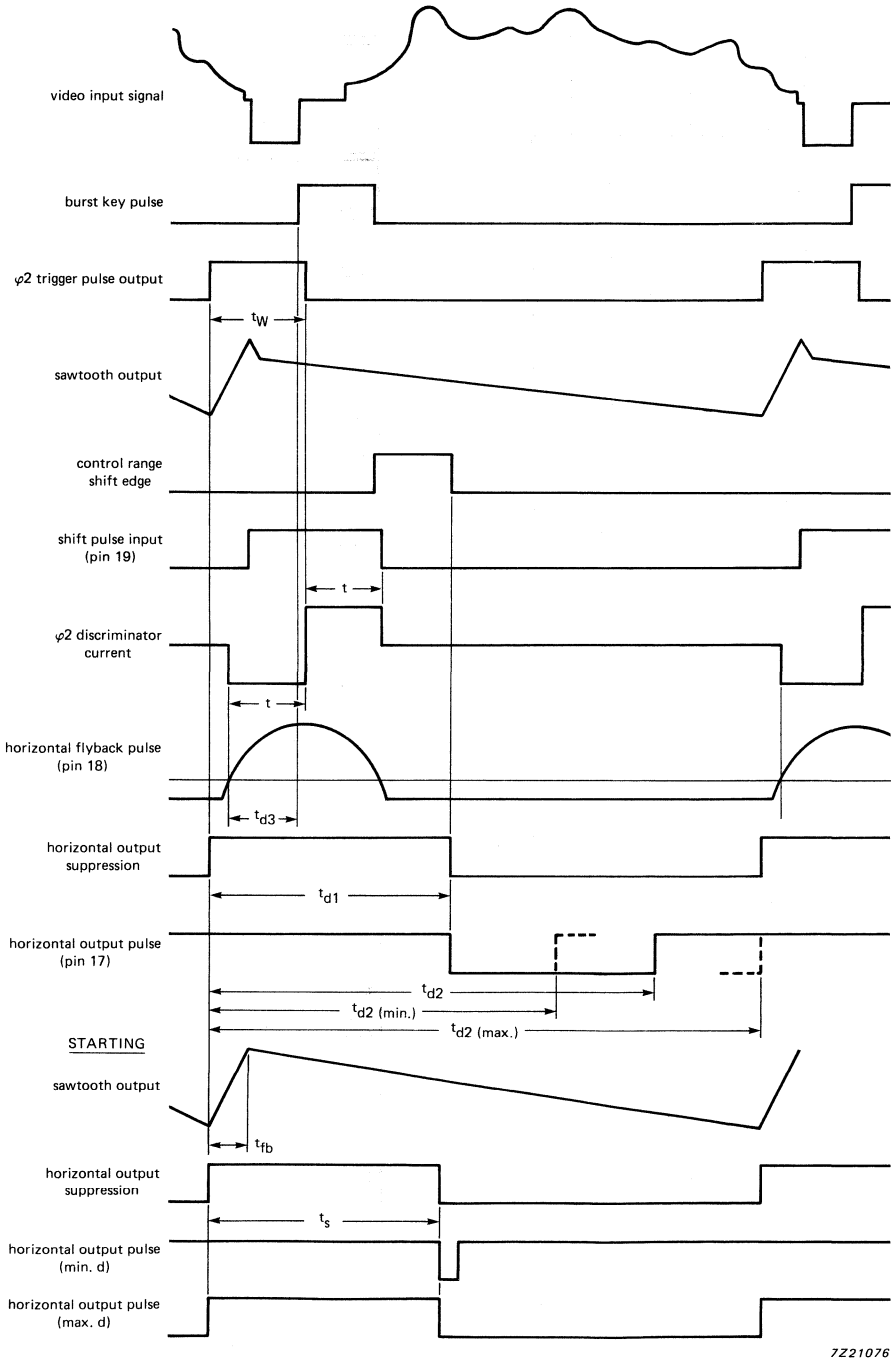


Fig. 3 Timing diagram; video input and starting time.

DEVELOPMENT DATA

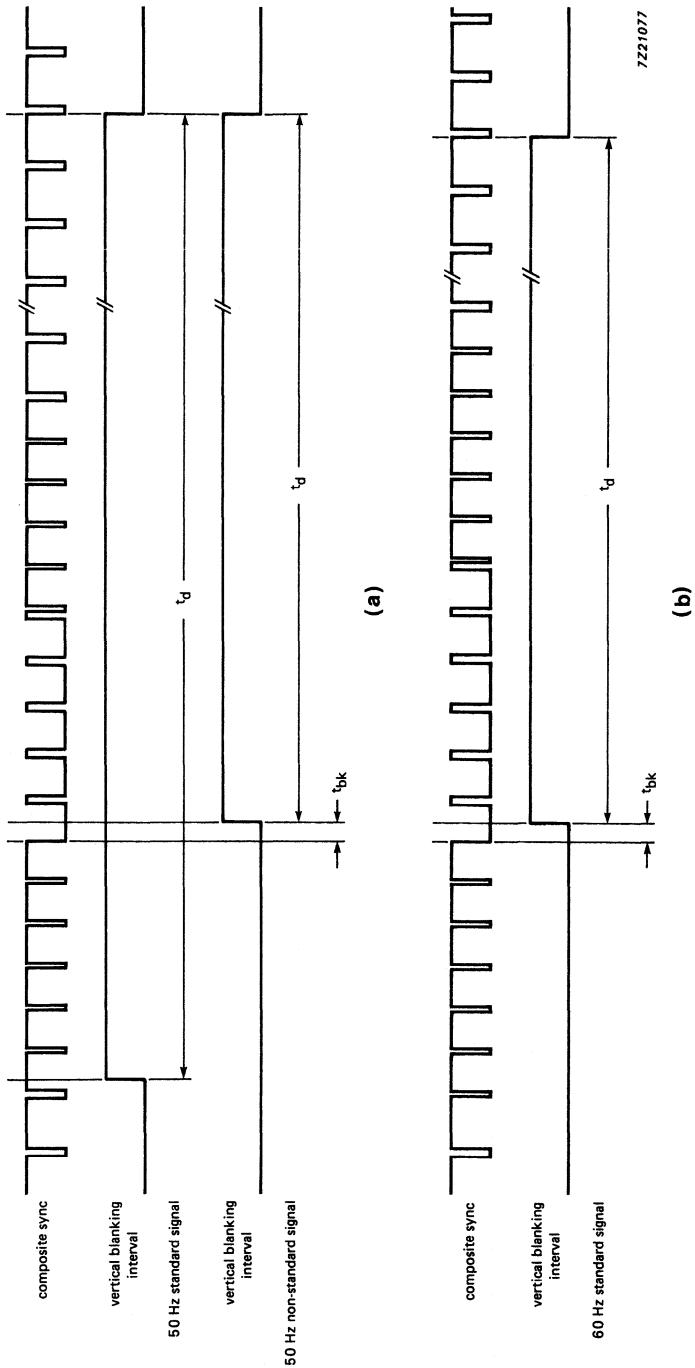
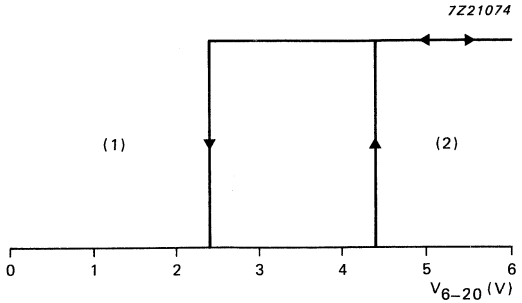


Fig. 4 Timing diagram; vertical blanking synchronization
(a) 50 Hz standard (b) 60 Hz standard.



(1) φ 1 gating circuit off
φ 1 discriminator to fast mode
clamping gate off
mute output HIGH
frame divider direct sync
horizontal sync separator self-aligned
noise detector not inhibited

(2) φ 1 gating circuit on
φ 1 discriminator to slow mode
clamping gate on
mute output LOW
frame divider indirect sync
horizontal sync separator gated
noise detector inhibited

Fig. 5 Coincidence detector time constant switching levels.

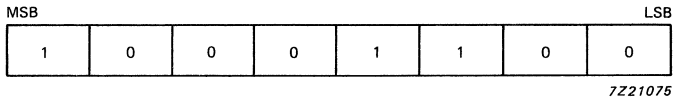


Fig. 6 Address byte.

Table 1 Data byte

	bit no.	logic level	description
MSB	D7	1	*
	D6	1	*
	D5	1	*
	D4	1	*
	D3	1	bit number D5 = don't care
	D3	0	bit numbers D6 and D7 = don't care
	D2	1	$\overline{\text{N.I.L.}}$ (inactive)
	D2	0	N.I.L. (active)
	D1	1	$\overline{\text{VID}_{\text{EXT}}}$ (inactive)
	D1	0	VID_{EXT} (active)
	D0	1	standard mode
LSB	D0	0	non-standard mode

* Bits D7 to D4 are used for measuring procedure in the IC factory.
For application use they must be inactive (logic 1).

DEVELOPMENT DATA

APPLICATION INFORMATION

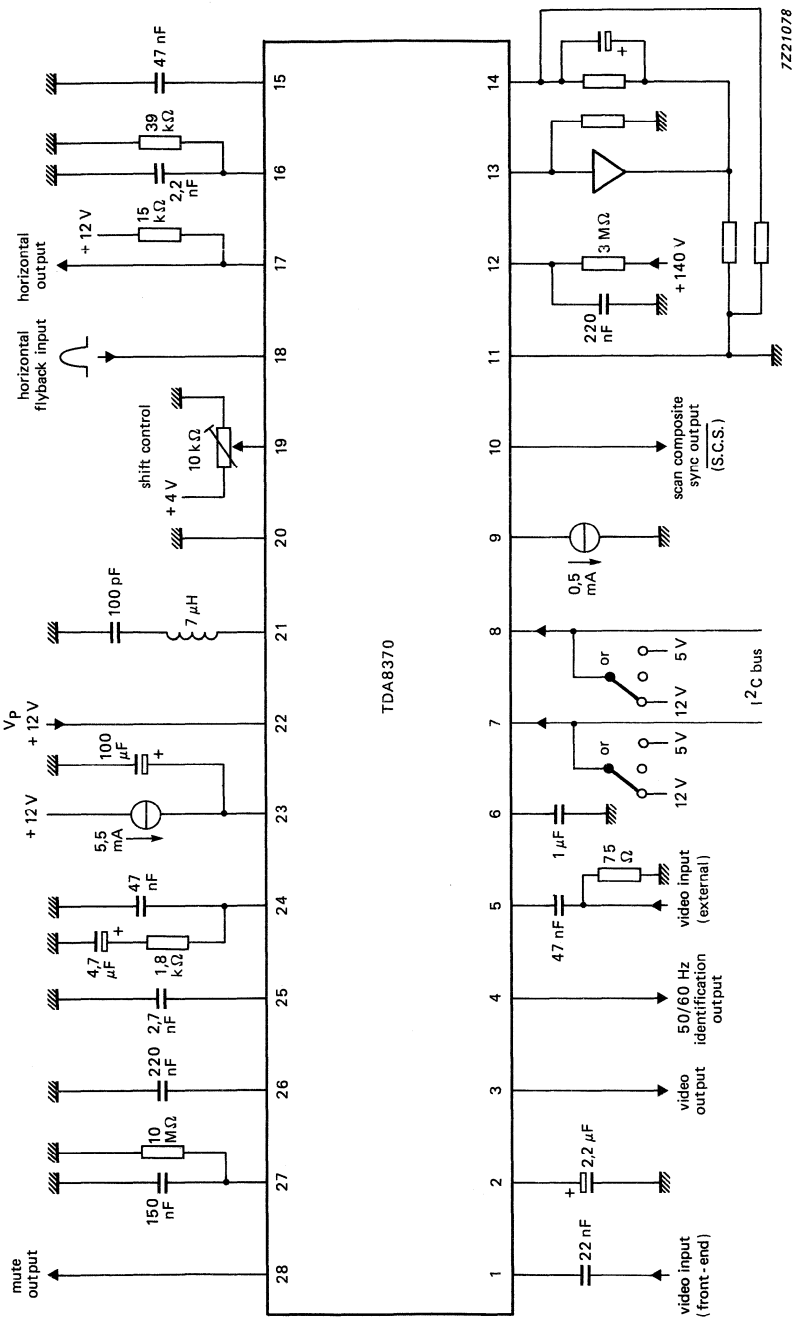


Fig. 7 Application diagram and test circuit.

CONTROL CIRCUIT FOR SWITCHED MODE POWER SUPPLIES

GENERAL DESCRIPTION

The TDA8380 is an integrated circuit intended for use as a control circuit in low-cost switched mode power supplies for television, monitors and small industrial equipment. The TDA8380 operates using duty factor regulation in the fixed frequency mode.

Features

- A low-current initialization circuit (maximum 150 μA) which can be switched off
- A bandgap reference generator
- Circuitry for slow-start combined with an accurate setting of the maximum duty factor (D_{max})
- Programmable low supply voltage protection with two default values
- High supply protection circuitry
- Error amplifier with a transfer characteristic generator (TCG)
- Protection against open- and short-circuited feedback loop
- An overload voltage foldback
- Primary current protection circuitry for both cycle-by-cycle and trip mode
- Protection against transformer saturation
- A direct drive output stage (sink current 2.5 A, source current 0.75 A)
- Anti-double pulse logic
- Protected against damage as a result of a short-circuited high-voltage transistor
- RC oscillator with synchronization input

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	–	14	–	V
Supply current	I_{CC}	–	–	15	mA
Output pulse repetition frequency range	f_o	10	–	100	kHz
Operating ambient temperature range	T_{amb}	–25	–	+ 70	°C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

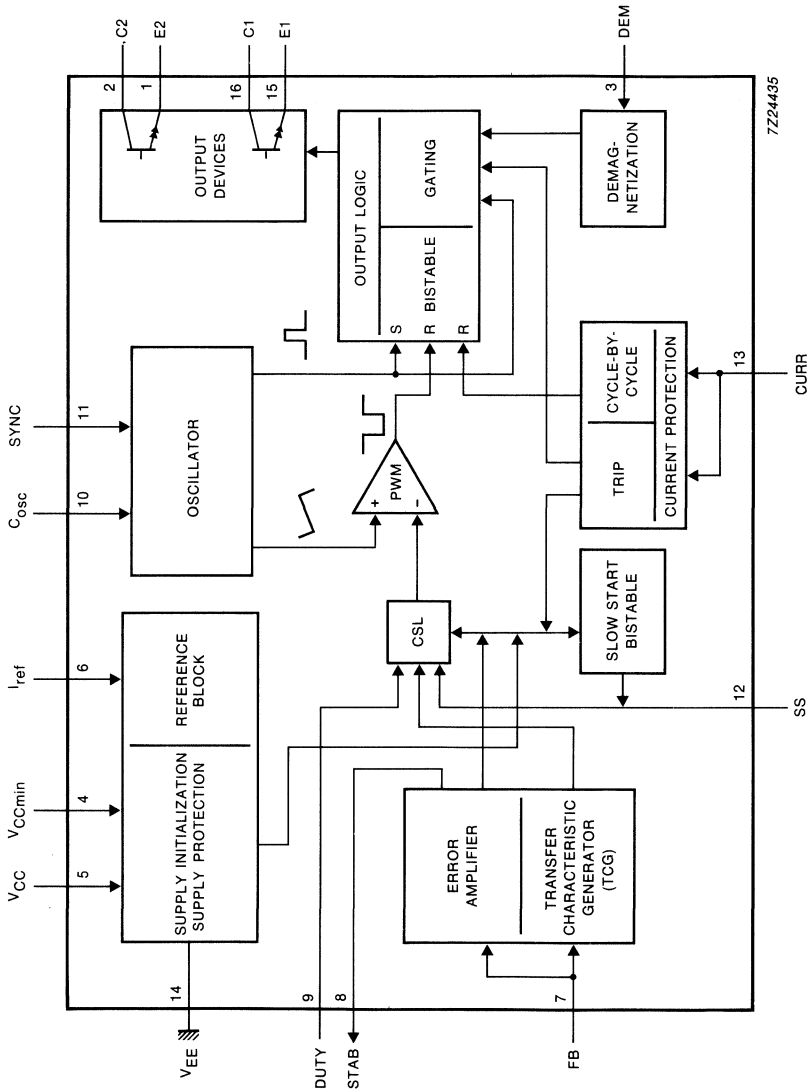


Fig.1 Block diagram.

PINNING

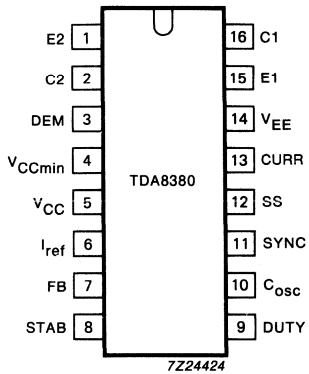


Fig.2 Pinning diagram.

DEVELOPMENT DATA

1	E2	Emitter of output source transistor
2	C2	Collector of output source transistor
3	DEM	Demagnetization sense input
4	V_{CCmin}	Minimum V_{CC} threshold setting
5	V_{CC}	Supply voltage
6	I_{ref}	Reference current setting
7	FB	Feedback input
8	STAB	Output error amplifier
9	DUTY	Pulse width modulator input
10	C_{OSC}	Oscillator capacitor
11	SYNC	Synchronization input
12	SS	Maximum duty factor (D_{max}) setting plus slow-start
13	CURR	Input current protection
14	V_{EE}	Ground
15	E1	Emitter of output sink transistor
16	C1	Collector of output sink transistor

FUNCTIONAL DESCRIPTION

The TDA8380 is a control circuit which generates the pulses required to drive the switching transistor in a switched mode power supply (SMPS).

Supply

This device is intended to be used on the primary side of the power supply and can be supplied via a take-over (auxiliary) winding on the transformer.

The device is initialized via a high value resistor connected between the rectified mains voltage and the device's supply pin (pin 5), which causes the capacitor connected to this pin to charge slowly. When the voltage exceeds the initialization level (typically 17 V) the device will start up and the duty cycle will be slowly increased by the slow-start circuit. After a short period the take-over winding will supply the device. The value of the resistor is normally defined by the time taken to charge the capacitor. A one second delay between switching on and operation of the power supply is acceptable in most cases.

The operating voltage range is from 9 to 20 V. The supply pin is protected by a 23 V Zener diode. The supply protection circuit is activated once the Zener diode is conducting. The slow-start procedure begins after initialization, until then the output is off. The current drawn by the device during the initialization period is less than 150 μA.

When the supply voltage falls below the minimum trip level, the device switches off and the start-up procedure is repeated. The minimum voltage supply threshold setting (V_{CCmin}) can be set externally with a resistor connected between the V_{CCmin} pin (pin 4) and ground (pin 14) (see Fig.3).

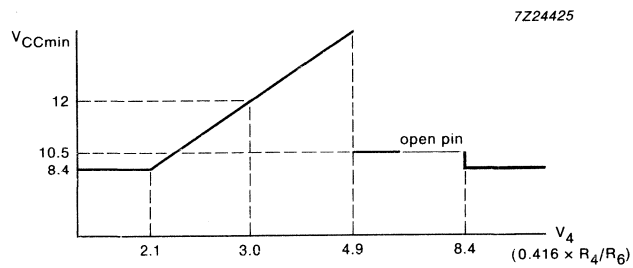


Fig.3 Trip level setting of minimum V_{CC} protection level.

V_{CCmin} can be set between 8.4 V (an internally fixed overriding protection level) and 17 V by means of an external resistor connected to pin 4. With pin 4 left open, the device takes a default value of 10.5 V. If the default value is chosen, care must be taken that no parasitic capacitance (due to wiring) is present at this pin as it will affect the correct operation of the device.

When choosing the initialization and minimum supply voltages the following should be taken into account:

- The difference between the two voltages should be large enough to enable a supply voltage dip during start-up.
- The value of the minimum supply voltage should be high enough to ensure that the high-voltage transistor is correctly driven. A high protection level makes it possible to have a large resistor value in series with the base drive.

For battery line input operation, the V_{CCmin} pin is connected to V_{CC}, the start-up circuit is then inhibited and the device starts operating when V_{CC} exceeds the 8.4 V protection level (this level has a hysteresis of approximately 70 mV). The device draws current continuously under these conditions.

Reference block

A bandgap based reference generates a stabilized voltage of 7 V to supply most of the device's internal circuits, this decreases chip size and increases reliability. The only circuits connected to V_{CC} are:

- The initialization circuit
- The output circuitry
- The series transistor of the stabilized voltage

By means of a resistor (R_6) connected to the I_{ref} input a reference current is defined which determines six other device settings.

Part of the reference current is used to charge the oscillator capacitor (C_{10}), therefore, the charging time is proportional to $R_6 \times C_{10}$. The maximum duty factor (D_{max}) is set by the resistor connected to pin 12 (R_{12}) and is defined by the ratio R_6/R_{12}. The minimum supply voltage (pin 5) set by the resistor (R_4) at input V_{CCmin} is defined by: $4/6 \times V_6 \times R_4/R_6$.

Oscillator

The oscillator capacitor is charged and discharged between the high and low voltage levels as defined by the bandgap reference (high voltage typically 5 V and low voltage typically 1.4 V). The charge current is 1/6 of the reference current, the discharge current having the same value as the reference current. The period is therefore defined by $10 \times R_6 \times C_{10}$.

The oscillator flyback pulse is used to set the bistable in the output logic, however the output remains low until the positive ramp starts (see Fig.4). The oscillator can be synchronized by means of the SYNC pin. When this pin is connected to V_{CC}, the oscillator is free running. When it is between 0.85 and 5.6 V, the oscillator stops at the low voltage level prior to the next positive ramp.

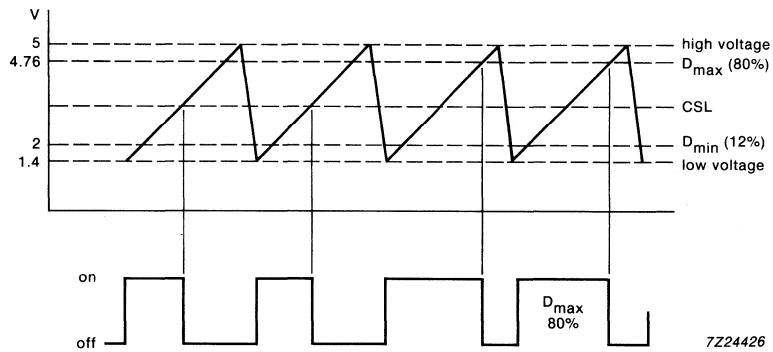


Fig.4 Oscillator levels.

FUNCTIONAL DESCRIPTION (continued)

Synchronization

The synchronization input (pin 11) can be driven by either an optocoupler or a loosely coupled pulse transformer.

Figure 5(a) illustrates synchronization using the 0.85 V threshold and a digital signal connected to the SYNC input (for example, an optocoupler between pin 11 and V_{CC}); the duty factor of the pulse is not very important. The oscillator starts at the first negative going edge of the sync. signal after the low voltage level has been reached. The synchronization frequency must be lower than the free running frequency. Synchronization must never affect the period time as this will corrupt the setting of the maximum duty factor.

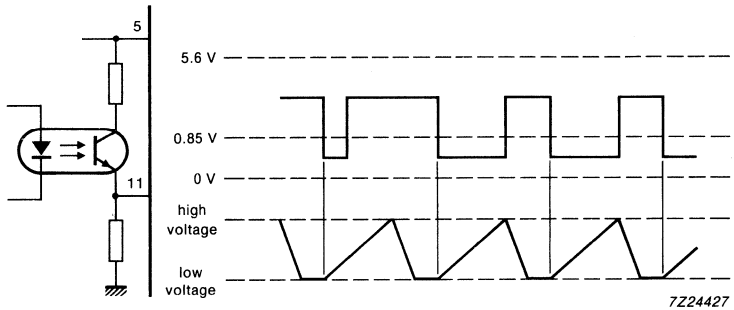


Fig. 5(a) DC coupled synchronization using the 0.85 V level.

In Fig.5(b) the disabling threshold (5.6 V) is used for synchronization. In this case the oscillator starts at the positive going edge of the sync. signal.

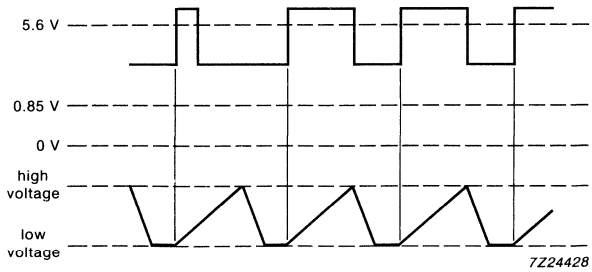
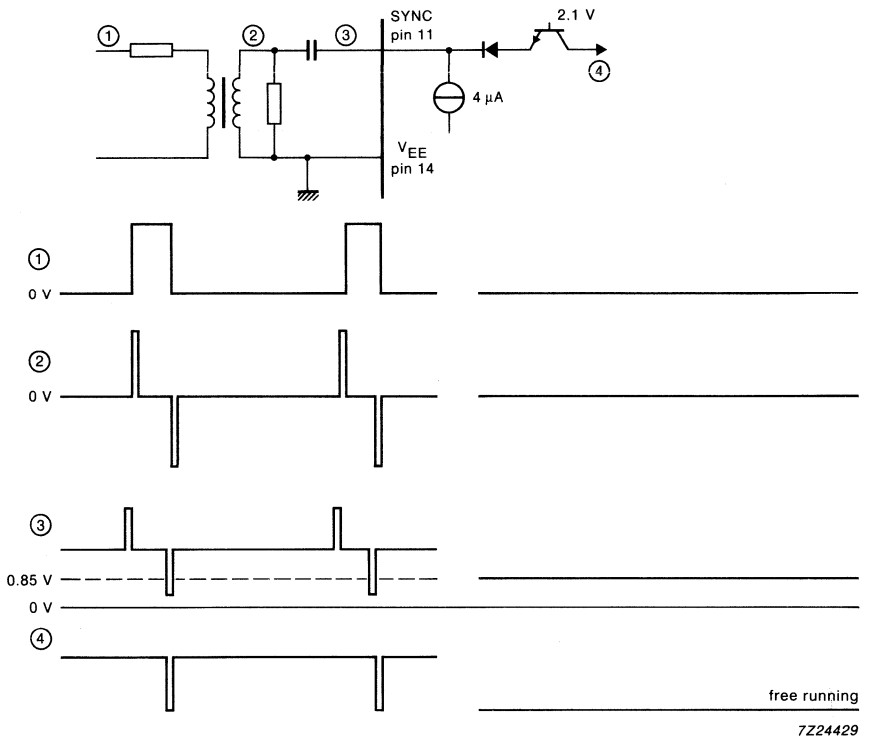


Fig.5(b) DC coupled synchronization using the 5.6 V level.

Figure 6 illustrates synchronization using a pulse transformer. Internal circuitry causes a DC shift which informs the device that synchronization pulses are present (spikes around 0 V at the output of the pulse transformer) or not present (DC 0 V at the output of the pulse transformer). When synchronization is not used the SYNC pin must be connected to V_{CC}, it must not be connected directly to ground or left open.



Synchronization pulses present. Synchronization pulses not present.

Fig.6 Synchronization using a pulse transformer.

FUNCTIONAL DESCRIPTION (continued)

Error amplifier

The error amplifier compares the feedback voltage of the SMPS with a reference voltage (nominally 2.5 V). The amplifier output at pin 8 enables gain setting. The amplifier is internally compensated for 0 dB feedback stability.

The output of the error amplifier is not internally connected to the Pulse Width Modulator (PWM). One input to the PWM is available at the DUTY input (pin 9) via the Control Slicing Level (CSL) circuit. Normally the STAB and DUTY pins are connected together, but direct driving of pin 9 via an optocoupler from the secondary side is also possible. A type of current mode control can be achieved by mixing the STAB signal with the primary current signal before applying it to the DUTY input.

The feedback (FB) input (pin 7) is used as the input to the Transfer Characteristic Generator (TCG) circuit which ensures well defined duty factors at low FB voltages; a voltage foldback is an inherent characteristic. In Fig.7, the duty factor is shown as a function of the voltages at the FB, DUTY and SS inputs. The input which gives the lowest duty factor overrides the others.

The left hand curve is passed through during a slow-start (via the slow-start input pin 12) when the duty cycle slowly increases linearly with respect to V_{12}. The right-hand curve is passed through at start-up. The FB voltage slowly increases from zero and the duty factor, starting at 12%, increases until the maximum duty factor (D_{max}) is reached. A few hundred millivolts later, the FB voltage reaches the start of the regulation curve which is at approximately 2.5 V. The plateau area between reaching D_{max} and starting the regulation curve is kept as small as possible (typically 200 mV).

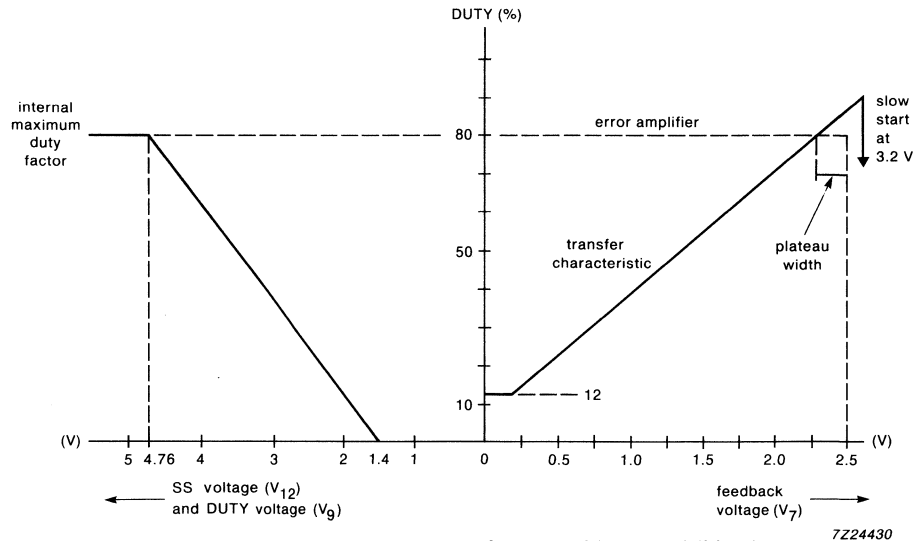


Fig.7 The duty factor as a function of the FB, SS and DUTY voltages.

Due to the characteristics of the TCG, and the fact that an open FB input results in a low voltage at the FB input, open- and short-circuit feedback loops will result in low duty factors. When DC feedback is used across the error amplifier, the current capability of the error amplifier must be considered when determining the feedback resistor value.

When the input to the PWM (pin 9) is driven by an optocoupler, the TCG can be used when a rough primary voltage is applied to the FB input. In this situation an open feedback loop will cause an increase in the FB voltage as the duty factor rises to its maximum. As soon as the FB voltage exceeds the reference by 0.7 V, the slow-start is triggered.

Demagnetization sense circuit

To enable the SMPS to be kept in the non-continuous mode, an input is available which delays switch-on of the high-voltage transistor until the transformer currents have decayed to zero. This is an effective way of avoiding transformer saturation. The waveforms illustrated by Fig.8 show demagnetization with respect to the application diagram of Fig.12.

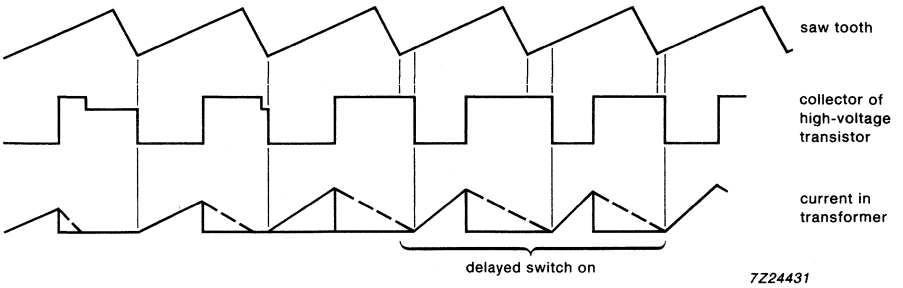


Fig.8 Demagnetization function.

As long as the voltage of the take-over (auxiliary) winding (also used for supplying the device) is above 0.6 V (V_3) the output will be prevented from switching on.

Over-current protection

The over-current protection circuit (pin 13) senses the voltage across resistor R_s (see Fig.12), which reflects the primary current. This generated voltage is negative-going as the emitter of the high-voltage power transistor is grounded (this circuit arrangement provides the IC with the best safeguard against a possible collector-emitter short-circuit in the power transistor). At pin 13, the negative voltage signal is shifted to a positive level by a voltage across resistor R_{13}. This voltage is set by the reference current at pin 13 and is defined by resistor R_6 at the I_{ref} input (pin 6) and = $1/6 \times V_{ref}/R_6$.
Therefore $V_{shift}(V_{R13}) = V_{ref}/6 \times R_{13}/R_6$ or nominal $0.416 \times R_{13}/R_6$ (V).

The positive current monitor voltage at pin 13 is compared with two voltage levels: the first level = 0.2 V and the second level = 0 V (see Fig.9).

The first trip level only switches off the high-voltage transistor for a cycle and puts the SMPS in a continuous cycle-by-cycle current protection mode.

The second trip level is only activated when the primary current rise is very fast which can occur during a short-circuited output. In this mode the high-voltage transistor is quickly switched off and the slow-start procedure is activated.

The difference between the first and second primary current peak levels is set by R_s:

$I_2 - I_1 = 0.2/R_s$.

The absolute peak values are set by R_6 and R_{13}:

$I_2 \times R_s = 0.416 \times R_{13}/R_6$ or

$I_1 \times R_s = (0.416 \times R_{13}/R_6) - 0.2$

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Over-current protection (continued)

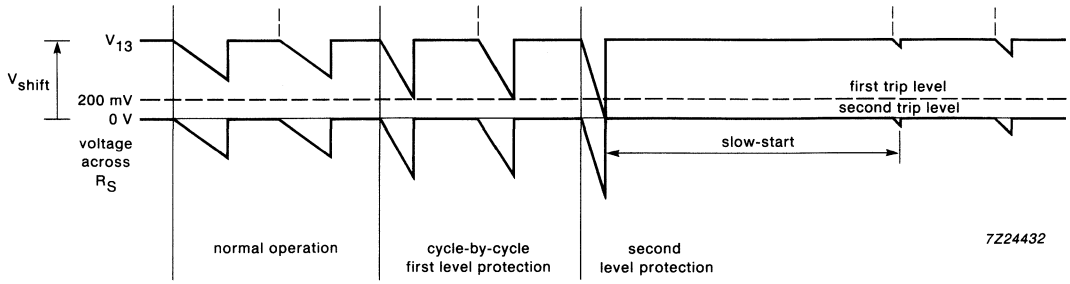


Fig.9 Current protection.

Slow-start circuit

A slow-start occurs:

- At Switch-on of the SMPS
- After a current trip as described in the section **Over-current protection**
- After a low or high V_{CC} trip.

The capacitor at the SS input is discharged and the slow-start bistable is reset when the voltage at the SS input falls below 0.5 V after which the circuit is ready for a slow-start. The dead time (during which the capacitor at the SS input is being charged to the 1.4 V lower level of the sawtooth) before duty cycle regulation starts is minimal. The SS input can also be used for D_{max} setting by connecting a resistor to ground. The voltage across this resistor is then limited to $1/6 \times V_{ref} \times R_{12}/R_C$.

Output stages

The output stage consists of two NPN darlington transistors, their collector and emitter connected to separate pins (see Fig.12). The top transistor is capable of sourcing a maximum of 0.75 A to the high-voltage transistor while the bottom transistor can sink peak currents up to 2.5 A.

For low currents up to 10 mA, the saturation voltage of the sink darlington transistor is similar to that of a single transistor (see Fig.10). During switching of this transistor dV/dt is internally limited to reduce interference.

Care should be taken with the external wiring of the output pins to avoid oscillation or interference due to parasitic inductance and wire resistance.

During start-up a small current flows from V_{CC} to E2 to precharge the series capacitor at the output (see Fig.12).

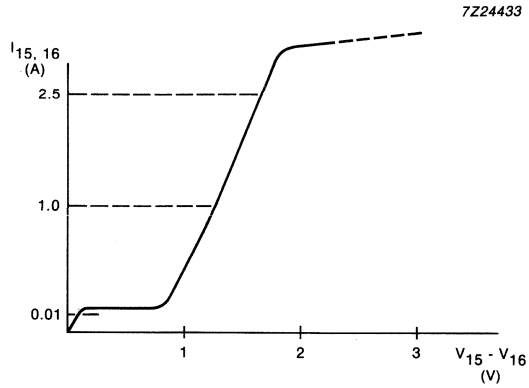


Fig.10 Saturation curve.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	typ.	max.	unit
Voltage					
pin 5 (V_{CC})		−0.5	–	20	V
pins 1, 2, 4 and 16		−0.5	–	V_{CC}	V
pins 3 and 13		−0.5	–	0.5	V
pins 7 and 9		−0.5	–	6.5	V
pin 11		0.6	–	V_{CC}	V
Currents					
pin 5 (V_{CC})		0	–	20	mA
pin 1		−0.75	–	0	A
pin 2		0	–	0.75	A
pins 3, 4, 6 to 8 and 10 to 12		−10	–	10	mA
pin 13		−200	–	10	mA
pin 15		−2.5	–	0	A
pin 16		0	–	2.5	A
Total power dissipation	P_{tot}	see Fig.11			
Operating ambient temperature range (for dissipation $\leqslant$ 1 W)	T_{amb}	−25	–	+ 70	°C
Storage temperature range	T_{stg}	−65	–	+ 150	°C

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j\text{-}a(max)} = 55$ K/W

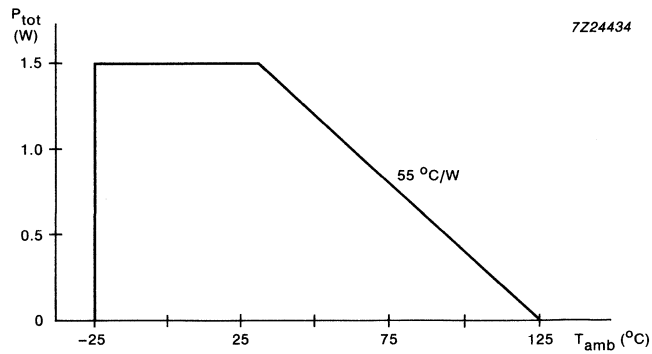


Fig.11 Power derating curve.

DEVELOPMENT DATA

CHARACTERISTICS

V_{CC} = 14 V; T_{amb} = 25 °C; reference resistor = 5 kΩ unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{CC}	9	–	20	V
Supply initialization level		V_5	15	17	18	V
High voltage protection		V_5	21	23	25	V
Internal fixed minimum protection level		V_5	7.9	8.4	8.9	V
Hysteresis		dV_{CC}	*	30	*	mV
Internal default minimum protection level			9.8	10.5	11.2	V
Supply current operational		I_{CC}	–	–	15	mA
before initialization		I_{CC}	–	100	150	μA
Reference current (pin 4)	note 1	I_4	I_6/5.7	I_6/6	I_6/6.3	mA
Trigger level V_{CCmin} setting		V_5	$3.8V_4$	$4V_4$	$4.2V_4$	V
Clamp voltage	at 20 mA		*	23.5	*	V
Reference (pin 6)						
Reference voltage		V_{ref}	2.4	2.5	2.6	V
Current range		I_{ref}	200	–	800	μA
Reference voltage over I_6 range		dV_{ref}	–20	–	+ 20	mV
Error amplifier						
Error amplifier threshold	V_{CC} = 8.5 to 20 V	V_7	2.4	2.5	2.6	V
Input current		I_7	0	–	5	μA
Sink current output	at 1.2 V	I_8	1	–	–	mA
Source current output	at 5.5 V	I_8	*	100	*	μA
Open loop gain		A0	–	100	–	dB
Unity gain bandwidth		BW	–	200	–	kHz
Input DUTY current	note 1	I_9	I_6/5.7	I_6/6	I_6/6.3	mA
High FB protection level		V_7	3	3.2	3.3	V
Temperature coefficient of error amplifier threshold		dV_7/dT	–	100	–	10^{-6}/K
TCG function (see Fig.7)						
Transfer characteristic		dD/dV_7	–	32	–	%/V
Minimum duty factor		D_{min}	–	12	–	%
Plateau width		V_7	*	200	*	mV

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Slow-start function						
Transfer characteristic		dD/dV_{12}	–	23.8	–	%/V
Input current	note 1	I_{12}	$I_6/5.7$	$I_6/6$	$I_6/6.3$	mA
Sink current during faults	at 0.5 V	I_{12}	8	–	–	mA
Internally fixed maximum duty factor		D_{max}	75	80	85	%
Clamp current	at V_{12} = 0.5 V	I_{12}	–	2	–	mA
Output stage						
Source transistor						
Voltage drop with respect to V_{CC}	at 0.75 A	$V_{CC}-V_1$	–	2	*	V
Pull-up current	$V_{CC} - V_1$ = 15 V	$-I_1$	25	–	100	μA
Operating current range		$-I_1$	0	–	0.75	A
Sink transistor (see Fig.10)						
Saturation voltage						
at 2.5 A		$V_{16} - V_{15}$	–	2	*	V
at 1 A		$V_{16} - V_{15}$	–	1.5	*	V
at 10 mA		$V_{16} - V_{15}$	–	0.3	*	V
Leakage current	$V_{16} - V_{15}$ = 20 V	I_{16}	–	–	1	μA
Falling edge		$dV_{16\text{-}15}/dt$	–	0.2	–	V/ns
Operating current range						
Peak		I_{16}	0	–	2.5	A
Average		I_{16}	–	–	250	mA
Oscillator						
High level voltage		V_{10}	–	5	–	V
Low level voltage		V_{10}	–	1.4	–	V
Charge current	note 1	I_{10}	$I_6/5.7$	$I_6/6$	$I_6/6.3$	mA
Frequency range		f_o	10	–	100	kHz
Frequency	R_6 = 5 kΩ C_{10} = 680 pF	f_o	28	29.5	31	kHz
Temperature coefficient of the frequency		df/dT	–	100	–	10^{-6}/K

* Value to be fixed.

parameter	conditions	symbol	min.	typ.	max.	unit
Synchronization						
Minimum synchronization pulse width		t_{11}	–	–	0.5	μs
Switching threshold		V_{11}	*	0.85	*	V
Input current		I_{11}	*	4	*	μA
Disabling threshold		V_{11}	–	5.6	–	V
Demagnetization input						
Pin voltage	at 0 A	V_3	–	690	–	mV
Input current	at 0 V	I_3	*	–40	*	μA
Current range of clamp circuits		I_3	–5	–	2	mA
Clamp level positive	at 1 mA	V_3	–	0.85	–	V
Clamp level negative	at –1 mA	V_3	–	–0.8	–	V
Current protection						
Input current	note 1	I_{13}	$I_6/5.7$	$I_6/6$	$I_6/6.3$	mA
First threshold		V_{13}	190	200	210	mV
Second threshold		V_{13}	–10	0	10	mV
Delay to switch output via level 1	pulse at pin 13 from 300 mV to 100 mV; I_O = 500 mA	–	–	350	–	ns
Delay to switch output via level 2	pulse at pin 13 from 300 mV to –200 mV; I_O = 500 mA	–	–	300	–	ns
First threshold including R_{13} (12 kΩ)	R_6 = 5 kΩ	–	*	–800	*	mV
Threshold for open pin detection		V_{13}	–	3.5	–	V

Note to the characteristics

1. Over the current range of I_6; 200 to 800 μA.

* Value to be fixed.

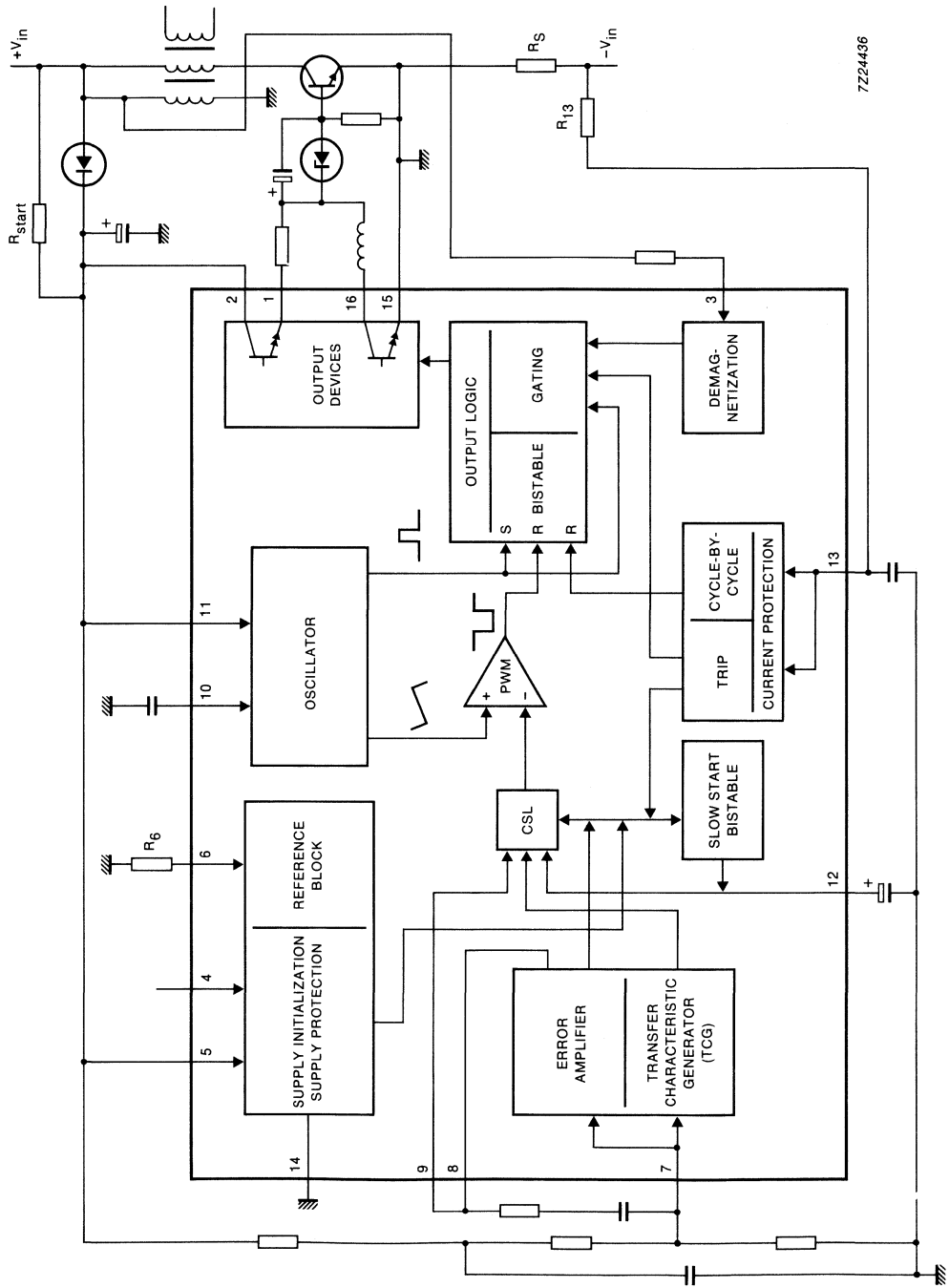


Fig.12 Simplified application diagram.

DEVELOPMENT DATA

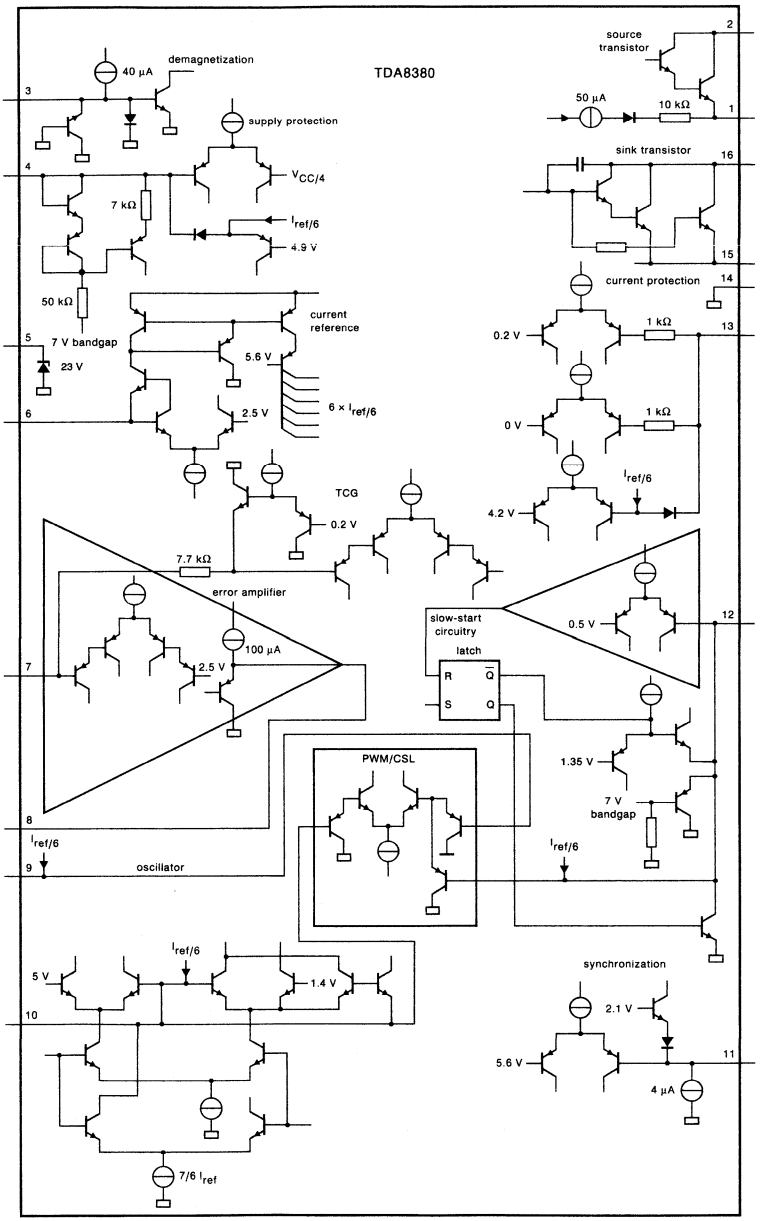


Fig.13 Input and output loading diagram.

PAL DECODER AND RGB MATRIX

GENERAL DESCRIPTION

The TDA8390 is a one-chip PAL colour decoder which is designed to be used in combination with the P^2CCD Delay Line (TDA8451) and the Filter Combination (TDA8452). The IC combines the circuits that are required for the identification and demodulation of PAL signals, RGB matrixing and amplification. SECAM signals can be handled when the IC is used in combination with the SECAM decoder TDA8490.

Inductive components are not required due to the integration of the filters and the delay lines.

The TDA8390 provides a crystal precise reference signal for the clock generator circuits in TDA8451 and TDA8452. Therefore, no adjustments are required to the filters and delay times. The decoder contains separate inputs for RGB signal insertion (analogue or digital) which can, for example, be used for text display systems (e.g. channel number display, Teletext, Antiope etc.).

Features

- A black-current stabilizer which controls the black currents of the three electron guns
- Contrast and brightness control of inserted RGB signals
- Self aligned oscillator
- Capacitive coupling with black level clamping of the luminance, colour difference and RGB inputs
- Equal black levels for internal TV and external signals
- 12 MHz bandwidth
- Emitter follower outputs for driving the RGB output stages

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{23-29}	10.0	12	13.2	V
Supply current		I_{23}	–	90	–	mA
Luminance input voltage (peak-to-peak value)		$V_{25(p-p)}$	–	0.45	–	V
Contrast control range		ΔG	–	20	–	dB
Chrominance input voltage (peak-to-peak value)		$V_{30(p-p)}$	–	465	–	mV
Demodulator output voltages						
R-Y (peak-to-peak value)		$V_{26(p-p)}$	0.50	0.62	0.74	V
B-Y (peak-to-peak value)		$V_{27(p-p)}$	0.64	0.80	0.96	V
Saturation control range		ΔG	50	–	–	dB
Colour difference input signals						
R-Y (peak-to-peak value)		$V_{21(p-p)}$	–	0.62	–	V
B-Y (peak-to-peak value)		$V_{22(p-p)}$	–	0.8	–	V
RGB input signal (peak-to-peak value)		$V_{14, 16, 18(p-p)}$	–	0.7	–	V
Bandwidth of RGB amplifier	–3 dB	B	12	–	–	MHz
Video switching voltage	external RGB	V_9	0.9	–	4.0	V
RGB output voltage (peak-to-peak value)		$V_{13, 15, 17(p-p)}$	–	4.0	–	V
Brigthness control range		V_5	–	2	–	V

PACKAGE OUTLINE

32-lead DIL; plastic with internal heat spreader (SOT201).

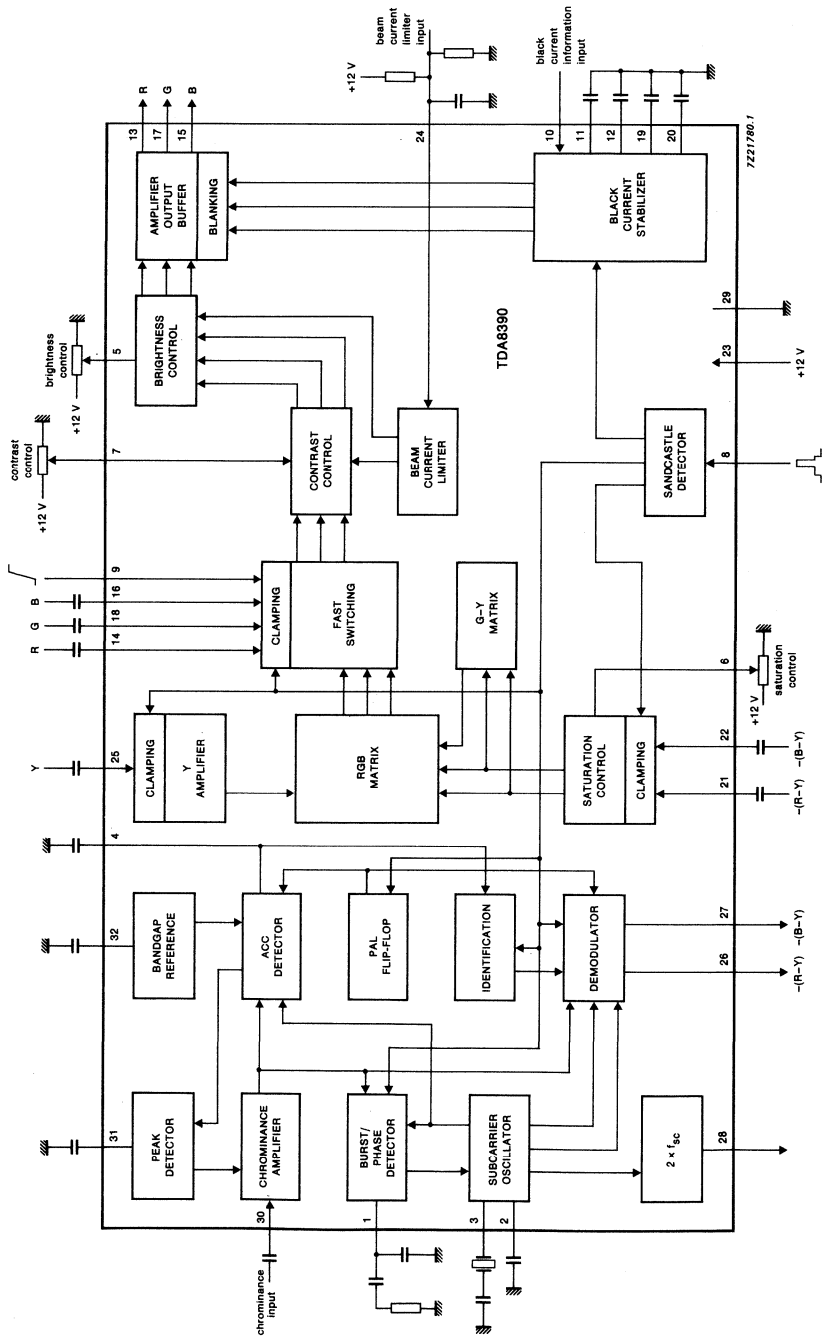


Fig.1 Block diagram.

PINNING

1. Phase detector
2. 90° phase shift DC reference
3. 4.43 MHz PAL reference frequency input
4. Sample and hold (PAL identification)
5. Brightness control
6. Saturation control
7. Contrast control
8. Sandcastle pulse input
9. Video switch input
10. Black current input
11. Black current reference
12. Red clamping circuit
13. Red signal output
14. Red insertion input
15. Blue signal output
16. Blue insertion input
17. Green signal output
18. Green insertion input
19. Blue clamping circuit
20. Green clamping circuit
21. −(R-Y) colour difference input
22. −(B-Y) colour difference input
23. Positive supply voltage
24. Beam current limiter input
25. Luminance input
26. −(R-Y) signal output
27. −(B-Y) signal output
28. Frequency doubler output
29. Ground
30. Chrominance input
31. Automatic colour control
32. ACC reference voltage

FUNCTIONAL DESCRIPTION

Colour decoder

The input chroma signal is amplified and applied to the burst phase detector (reference signal R-Y phase), the ACC and identification detector (reference signal ± R-Y phase) and the two demodulators. The burst phase detector controls the oscillator which operates at a frequency of 4.43 MHz. By connecting pin 6 to 12 V, the free-running frequency of the oscillator can be adjusted (phase detector and colour killer switched off). The gain control stage of the oscillator is biased in such a way that sinewave signals are generated. The output from the oscillator is fed to a Miller integrator in order to obtain the required 90° phase shift. The reference signals obtained from the oscillator and 90° phase shift network are applied to the various demodulators.

The output signal from the ACC and identification detector is peak detected to generate the ACC voltage and detected in a sample and hold circuit to obtain the identification and killer information. Because the P^2CCD delay line (TDA8451) and the P^2CCD filter combination (TDA8452) both require a reference signal ($2 \times f_{sc}$) the oscillator frequency is doubled, internally, and is made available at pin 28. The demodulated signals, with the correct amplitude ratio, are applied to the TDA8451.

The TDA8390 can be combined with the SECAM decoder TDA8490 (Fig.3) by direct connection of their outputs. The output DC levels have been chosen so that the PAL decoder has priority (output level during PAL is higher than output level during SECAM).

Control circuit

The luminance and colour difference signals together with the RGB inputs and fast switching pulse form the inputs to the control circuit. The required luminance input signal (from TDA8452) has a peak-to-peak value of 0.45 V (including sync). The colour difference input signals (from TDA8451) have a negative phase with a 0.62 V (R-Y) and 0.8 V (B-Y) peak-to-peak value. After amplification, the luminance signal is applied to the RGB matrix.

The colour difference signals are fed to the saturation control circuit before being applied to the RGB matrix (the G-Y signal is generated after the saturation control circuit).

The normal matrix for PAL is: (G-Y) = −0.51 (R-Y)−0.19 (B-Y).

The signals from the RGB matrix are applied to a fast switching circuit from where external RGB signals can be selected. The fast switching circuit is controlled by the video switching input. After amplification the RGB signals (internal or external video) are controlled on the contrast and brightness before being fed to the outputs. A typical output signal amplitude is 4 V black-to-white (nominal controls).

The black level of the RGB output signals is determined by the black current stabilization circuit. The information regarding the black current level of the picture tube is obtained in the same manner as the TDA3562A. The beam current limiter input is used to reduce the output signal amplitude via the contrast and brightness control circuits.

A block diagram is given in Fig.1. Figure 2 illustrates the PAL decoder configuration and Figure 3 the PAL-SECAM configuration. Figures 4, 5 and 6 illustrate the Saturation, Contrast and Brightness control curves respectively.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 23)		V_P	–	13.2	V
Total power dissipation		P_{tot}	–	1.5	W
Operating ambient temperature range		T_{amb}	−25	+ 70	°C
Storage temperature range		T_{stg}	−25	+ 150	°C

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j\text{-}a}$ 40 K/W

DEVELOPMENT DATA

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; all voltages are referenced to ground (pin 29) unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 23)		V_P	10.0	12.0	13.2	V
Supply current (pin 23)		I_P	–	90	–	mA
Total power dissipation		P_{tot}	–	1	1.5	W
DEMODULATOR PART						
Chrominance amplifier (pin 30)						
Input signal amplitude (peak-to-peak value)	note 1	$V_{30(p-p)}$	–	465	–	mV
Input signal amplitude before clipping occurs in the input stage (peak-to-peak value)		$V_{30(p-p)}$	–	–	1100	mV
Minimum burst signal amplitude within the ACC control range (−1 dB) (peak-to-peak value)		$V_{30(p-p)}$	30	–	–	mV
Input resistance		R_{30}	–	12	–	kΩ
Input capacitance		C_{30}	–	–	4	pF
ACC control range			30	–	–	dB
Change in amplitude of the output signals (pins 26 and 27) over the ACC range		ΔV_o	–	± 1	–	dB
REFERENCE PART						
Phase locked loop						
Catching range	note 2	Δf	± 500	–	–	Hz
Phase shift for ± 400 Hz deviation of the oscillator frequency	note 2	$\Delta\varphi$	–	–	5	deg
Oscillator						
Temperature coefficient of the oscillator frequency		TC_{osc}	–	−2	–	Hz/K
Frequency deviation for a supply voltage change from 10 V to 13.2 V	note 2	Δf	–	40	–	Hz
Input resistance (pin 3)		R_3	–	650	–	Ω
Input capacitance (pin 3)		C_3	–	–	6	pF

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
ACC and identification detectors (pins 4 and 31)						
Voltage at the PAL identification output (pin 4)						
nominal input signal for PAL		V_4	–	5.0	–	V
without burst input		V_4	–	3.1	–	V
Colour-OFF voltage		V_4	–	3.3	–	V
Colour-ON voltage		V_4	–	3.5	–	V
Voltage at peak detector output (pin 31)						
voltage at nominal input signal		V_{31}	–	5.8	–	V
voltage without input signal		V_{31}	–	2.7	–	V
Demodulators						
Output signal amplitude						
R-Y output (peak-to-peak value) (pin 26)		$V_{26(p-p)}$	0.50	0.62	0.74	V
B-Y output (peak-to-peak value) (pin 27)		$V_{27(p-p)}$	0.64	0.80	0.96	V
Ratio of amplification of both demodulators G(B-Y)/G(R-Y)		V_{26-27}	1.6	1.78	1.96	
Frequency response between 0 and 1 MHz		f	–	–3	–	dB
Output resistance R-Y/B-Y output		R_{26-27}	–	100	–	Ω
Output DC level when a PAL signal is identified		V_{26-27}	–	8.3	–	V
Output level during killing		V_{26-27}	–	1.3	–	V
Unwanted signals at R-Y and B-Y outputs	note 3		–	–	*	dB
4.4 MHz residual carrier at R-Y and B-Y outputs (peak-to-peak value)		$V_{26-27(p-p)}$	–	–	10	mV
8.8 MHz + harmonics residual carrier at R-Y and B-Y outputs (peak-to-peak value)		$V_{26-27(p-p)}$	–	–	20	mV
H/2 ripple at R-Y output without input signal (peak-to-peak value)		$V_{26(p-p)}$	–	–	50	mV
Change in amplitude (R-Y/B-Y) with temperature		$\Delta V/\Delta T$	–	–0.1	–	%/K
Change in amplitude with supply voltage		$\Delta V/\Delta V$	–	–	± 0.1	dB

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Frequency doubler output (pin 28)						
Output signal amplitude (peak-to-peak value)		$V_{28(p-p)}$	–	350	–	mV
Output resistance		R_{28}	–	50	–	Ω
DC output level		V_{28}	–	4.9	–	V
Bandgap reference decoupling (pin 32)						
DC level		V_{32}	–	7.3	–	V
Luminance input (pin 25)						
Input voltage (peak-to-peak value)	note 4	$V_{25(p-p)}$	–	0.45	–	V
Input voltage before clipping occurs (peak-to-peak value)		$V_{25(p-p)}$	–	–	0.9	V
Input current		I_{25}	–	0.1	1.0	μA
Frequency response of total luminance and amplifier circuits; 0 to 12 MHz			–	–3	–	dB
Colour difference input signals						
Input signal amplitude (R-Y) (peak-to-peak value) (pin 21)		$V_{21(p-p)}$	–	0.62	–	V
Input signal amplitude (B-Y) (peak-to-peak value) (pin 22)		$V_{22(p-p)}$	–	0.8	–	V
Input current (pins 21 and 22)		$I_{21, 22}$	–	0.1	1.0	μA
RGB inputs (pins 14, 16 and 18)						
Input signal amplitude (peak-to-peak value)	note 5	$V_{14, 16, 18(p-p)}$	–	0.7	–	V
Δ Black level	note 6	$\Delta V_{13, 15, 17}$	–	–	*	mV
Frequency response of RGB amplifier between 0 and 12 MHz		f	–	–2	–	dB
Delay difference for the three channels		t_d	–	0	–	ns
Input current		$I_{14, 16, 18}$	–	–	10	μA
Video switching (pin 9)						
Input voltage	no signal insertion	V_9	–	–	0.3	V
Input voltage	signal insertion	V_9	0.9	–	4.0	V
Delay of switching		t_d	–	–	50	ns
Input resistance		R_9	–	10	–	kΩ

* Value to be fixed.

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Ratio of unwanted internal RGB signals with reference to 4 V at the RGB outputs (peak-to-peak value)	note 8; $V_9 > 0.9$ V 0 - 5 MHz		−46	–	–	dB
Ratio of unwanted external RGB signals with reference to 4 V at the RGB outputs (peak-to-peak value)	note 8; $V_9 < 0.3$ V 0 - 5 MHz		−35	–	–	dB
Sandcastle input (pin 8)						
Detection level for:						
vertical blanking		V_8	1.0	1.5	2.0	V
horizontal blanking		V_8	3.0	3.5	4.0	V
upper part of pulse		V_8	6.5	7.0	7.5	V
Input current						
V_I = 0 to 1.5 V		I_8	–	–	−0.5	mA
V_I = 1.5 to 3.5 V		I_8	–	–	−15	μA
V_I = 3.5 to 7.0 V		I_8	–	–	−7	μA
V_I = 7.0 to 12 V		I_8	–	–	−1	μA
Internal delay between black level clamping and burst gating pulse (leading edge)		t_d	1.5	2.0	2.5	μs
Saturation control input (pin 6)						
Saturation control range		G	50	–	–	dB
Saturation control curve				see Fig.4		
Input current saturation control for $V_6 < 4.5$ V		I_6	–	–	10	μA
Input resistance for V_6 between 4.5 V and 8 V		R_6	–	2	–	kΩ
Input resistance for V_6 between 8 V and 12 V		R_6	–	1	–	kΩ
Contrast control input (pin 7)						
Contrast control range	note 7	G	–	20	–	dB
Tracking of contrast control between the three channels over a control range of 10 dB			–	–	0.5	dB
Contrast control curve				see Fig.5		
Input current contrast control for $V_7 < 6$ V		I_7	–	–	10	μA
Input resistance for $V_7 > 6$ V		R_7	–	2	–	kΩ

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Brightness control input (pin 5)						
Brightness control voltage range	note 11	V_5	–	2.0	–	V
Brightness control curve				see Fig.6		
Input current brightness control		I_5	–	–	–50	μA
Colour difference matrices						
G-Y/R-Y			–	–0.51	–	
G-Y/B-Y			–	–0.19	–	
RGB amplifiers (pins 13, 15, 17)						
Output signal amplitude (peak-to-peak value)	notes 7 and 8	$V_{13, 15, 17(p-p)}$	3.5	4.0	4.5	V
Output signal amplitude for the blue channel (peak-to-peak value)	note 9	$V_{15(p-p)}$	4.3	5.4	6.5	V
Maximum peak white level		V_{max}	–	10.5	–	V
Available output current		$I_{13, 15, 17}$	10	–	–	mA
Difference in black level between the three outputs at nominal brightness	note 10	$\Delta V_{13, 15, 17}$	–	–	100	mV
Control range of black current stabilization at V black = 3 V and nominal brightness control			–	–	± 2	V
Black level shift with picture content		ΔV	–	–	40	mV
Output voltage during the 4L pulse after switch-ON		$V_{13, 15, 17}$	7.5	–	–	V
Variation of black level with temperature		$\Delta V/\Delta T$	–	0	–	mV/K
Variation of black level over contrast control at nominal satuarion	note 11 +3 to −17 dB	ΔV	–	–	*	mV
Relative spread between the three output signals			–	–	10	%

* Value to be fixed.

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Relative variation in black level between the three channels during variations of the following conditions:						
supply voltage (± 10%) at nominal controls	note 11	ΔV	–	–	*	mV
contrast (20 dB) at nominal saturation		ΔV	–	–	*	mV
saturation (50 dB) at nominal contrast		ΔV	–	–	*	mV
brightness (± 1 V) at nominal controls		ΔV	–	–	*	mV
Differential drift of the black level over a temperature range of 40 K	note 11	$\Delta V/\Delta T$	–	–	70	mV
Blanking level at the RGB outputs		V_{bl}	–	1	–	V
Difference in blanking level of the three channels		ΔV_{bl}	–	0	10	mV
Differential drift of the blanking levels over a temperature range of 40 K		$\Delta V/\Delta T$	–	0	10	mV
Tracking of the output black levels with supply voltage		$\frac{\Delta V_{bl}}{V_{bl}} \times \frac{V_P}{\Delta V_P}$	0.9	1.0	1.1	
Signal-to-noise ratio of output signals	note 3	S/N	–	–	*	dB
Output resistance		$R_{13, 15, 17}$	–	50	–	Ω
Current source at output stage		I_O	–	2.5	–	mA
Black current stabilization (pin 10)						
DC bias voltage		V_{10}	3.5	5.0	7.0	V
Difference between input voltage for black current and leakage current		ΔV	0.35	0.5	0.65	V
Input current during black current		I_{10}	–	–	1	μA
Input current during scan		I_{10}	–	–	10	mA
Internal limiting level		V_{10}	8.5	9.0	9.5	V
Switching threshold for black current control ON		V_{10}	7.6	8.0	8.4	V
Input resistance during scan		R_{10}	1.0	1.5	2.0	kΩ
DC input current during scan at pins 12, 19 and 20		$I_{12, 19, 20}$	–	–	50	nA
Maximum charge/discharge current during measuring time of clamping pulse at pins 12, 19 and 20		$I_{12, 19, 20}$	0.5	–	–	mA

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Beam current limiter (pin 24)						
Voltage when beam current limiter function is not active	note 12	V_{14}	5	–	–	V
Trigger level for beam current limiter function		V_{24}	–	4.2	–	V

Notes to the characteristics

1. Indicated as a signal for a colour bar with 75% saturation (chrominance/burst ratio = 2.2 : 1).
2. All frequency variations are referred to 4.43 MHz carrier frequency.
3. The ratio between wanted and unwanted signals (e.g. crosstalk, phase errors and noise) is specified as the output signal amplitude (peak-to-peak value at nominal conditions) with respect to the RMS value of the unwanted signal.
4. Signal with negative going sync. Amplitude includes sync pulse amplitude.
5. For a resultant black-to-white output signal of 4 V at nominal contrast.
6. Difference in black level between RGB signals and inserted signals.
7. Nominal contrast is specified as maximum contrast –3 dB. Nominal saturation as maximum saturation –6 dB; nominal white point adjustment is maximum –3 dB.
8. Nominal luminance input signal and nominal contrast.
9. Nominal contrast, nominal saturation no (R-Y) and no luminance signal.
10. With respect to the measuring pulse. At nominal brightness the black level of one output is identical to the measuring level.
11. With respect to the measuring pulse.
12. Pin 28 should be connected externally to a high-resistance voltage divider. Pins 14, 16 and 18 when unused, should be connected to ground via a 100 nF capacitor.

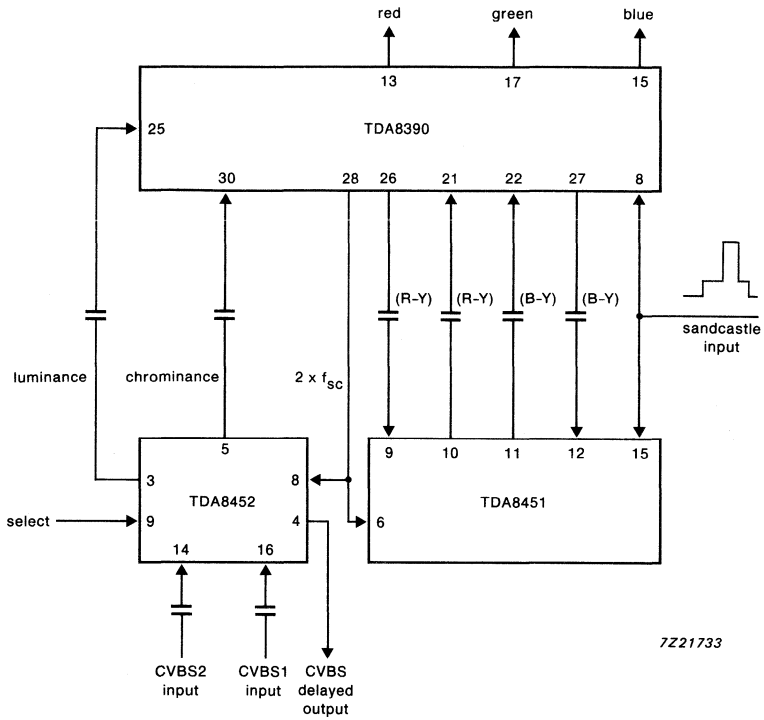


Fig. 2 PAL decoder configuration.

DEVELOPMENT DATA

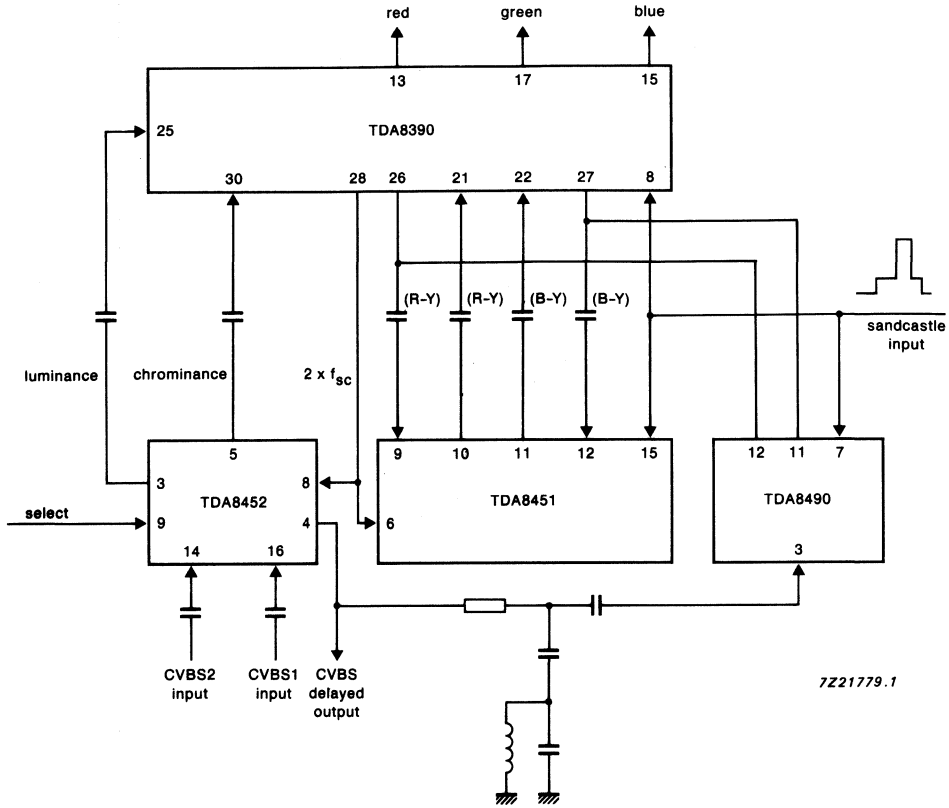


Fig. 3 PAL-SECAM decoder configuration.

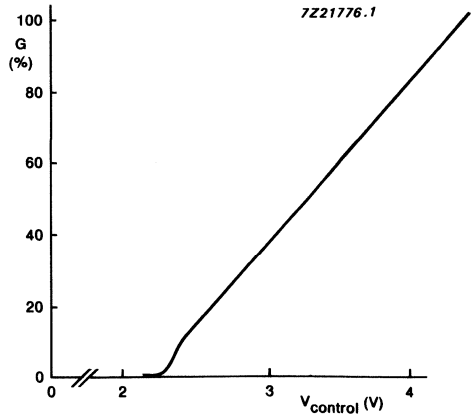


Fig.4 Saturation control curve.

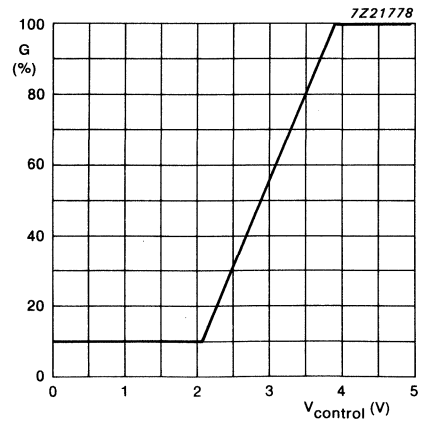
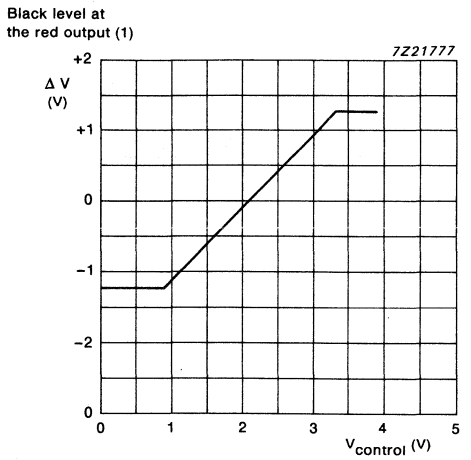


Fig.5 Contrast control curve.



(1) with respect to the measuring pulse

Fig.6 Brightness control curve.

DEVELOPMENT DATA

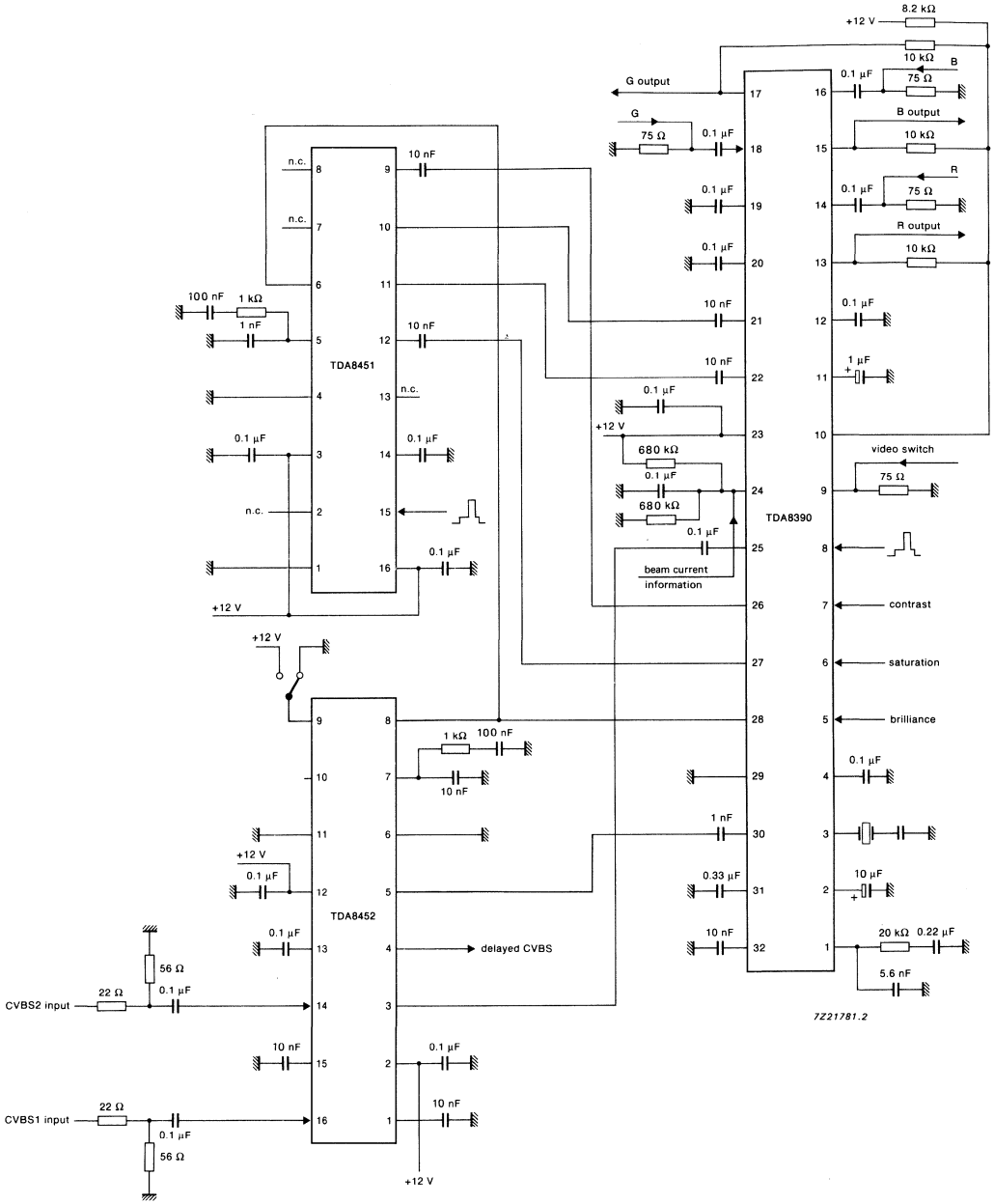


Fig.7 Application diagram.

TV AND VTR STEREO/DUAL SOUND PROCESSOR WITH I²C BUS CONTROL

GENERAL DATA

The TDA8405 integrated circuit is a processor for stereo/dual-language signals for stereo-sound television receivers and VTR. The modulated signals at the TDA8405 inputs need to be "(L+R)/2" or "language A" on one channel and "R" or "language B" on the second channel (where L = left and R = right). The second channel is also modulated with the pilot carrier. The IC is controlled via the two-line, bidirectional I²C bus.

Features

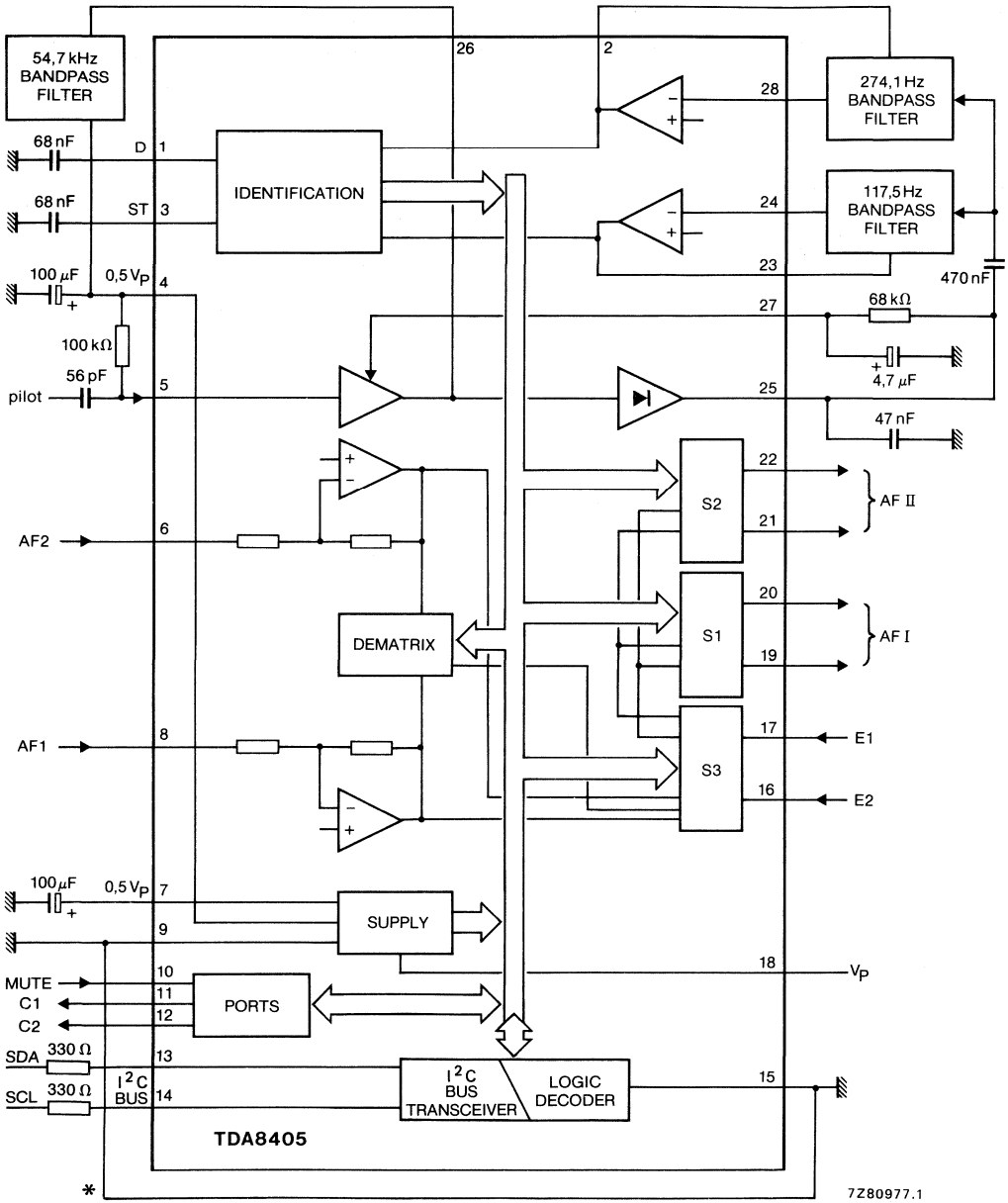
- Amplification of the two a.f. input signals by integrated operational amplifiers.
- Low distortion stereo dematrix
- All operational amplifiers are offset compensated
- I²C bus transceiver for system control (port control, mute, mode select, identification, etc.)
- Input port for fast muting
- Two general purpose output ports (three-state, bus-controlled)

QUICK REFERENCE DATA

Supply voltage	$V_P = V_{18\text{-}9\text{-}15}$	typ.	12 V
Supply current	$I_P = I_{18}$	typ.	25 mA
A.F. input signal	$V_{i(rms)} = V_{6\text{-}9}, V_{8\text{-}9}$	typ.	1 V
Weighted signal-to-noise ratio of the a.f. output-signals (CCIR 468/2)	(S+N)/N	⩾	70 dB
Crosstalk attenuation: stereo mode at f = 1 kHz	α_S	>	40 dB
dual sound mode at f = 40 to 12 500 Hz	α_{DS}	>	70 dB
Pilot signal input sensitivity	$V_i = V_{5\text{-}9(rms)}$	typ.	5 mV
Pilot signal amplifier gain control range	ΔG_V	>	40 dB

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).



* Direct connection between pins 9 and 15 is needed.

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 18)*	$V_P = V_{18-9, 15}$	max.	13,2 V
Output current (pins 19, 20, 21, 22)	I_n	max.	5 mA
Output current (pins 2, 23)	I_n	max.	1 mA
Output current (pins 11, 12)	I_n	max.	3 mA
Voltage range at any pin	V_n		0 to V_P V
Total power dissipation	P_{tot}	max.	1 W
Storage temperature range	T_{stg}		−40 to + 150 °C
Operating ambient temperature range	T_{amb}		0 to + 70 °C

DEVELOPMENT DATA

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

* Supply voltage may be applied only when pins 9 and 15 are connected to ground.

CHARACTERISTICS

T_{amb} = 25 °C; V_P = 12 V; $V_{i(af)rms}$ = 1 V; f = 1 kHz; dematrix aligned; $V_{i\,pilot(rms)}$ = 16 mV; test circuit Fig. 2; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply voltage	$V_P = V_{18\text{-}9,\,15}$	10,8	12	13,2	V
Supply current at V_P = 12 V	$I_P = I_{18}$	–	25	–	mA
Reference voltage	$V_{ref} = V_{4\text{-}9,\,15}$	–	$V_P/2$	–	V
DC levels (pins 5, 6, 7, 8, 16 17, 19, 20, 21, 22, 24, 28)	$V_{n\text{-}9,\,15}$	–	$V_P/2$	–	V
BUS TRANSCEIVER (pins 13, 14) (note 1)					
Clock SCL					
Voltage level LOW	$V_{14\text{-}15}$	−0,3	–	1,5	V
Voltage level HIGH	$V_{14\text{-}15}$	3,0	–	–	V
Timing LOW period	t_{PL}	4,7	–	–	μs
Timing HIGH period	t_{PH}	4,0	–	–	μs
Rise time	t_r	–	–	1	μs
Fall time	t_f	–	–	0,3	μs
Input current HIGH	I_{IH}	–	–	10	μA
Input current LOW	$-I_{IL}$	–	–	10	μA
Data					
Voltage level LOW	$V_{13\text{-}15}$	−0,3	–	1,5	V
Voltage level HIGH	$V_{13\text{-}15}$	3,0	–	–	V
Rise time	t_r	–	–	1,0	μs
Fall time	t_f	–	–	0,3	μs
Set-up time data	t_{SU}	0,25	–	–	μs
Input current HIGH	I_{13}	–	–	10	μA
Input current LOW	$-I_{13}$	–	–	10	μA
Output current LOW	$+I_{13}$	3,0	–	–	mA
MUTE PORT (pin 10) note 2					
Input voltage LOW	$V_{10\text{-}15}$	–	–	1,5	V
Input voltage HIGH	$V_{10\text{-}15}$	8	–	–	V

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
CONTROL PORTS (pins 11, 12)					
3-state HIGH, LOW, high ohmic					
Output resistance in open state	$R_{11, 12-15}$	50	–	–	kΩ
Output voltage LOW	$V_{11, 12-15}$	–	–	0,8	V
Output voltage HIGH	$V_{11, 12-15}$	V_{P-1}	–	–	V
Output current LOW	$I_{11, 12}$	500	–	–	μA
Output current HIGH	$-I_{11, 12}$	80	–	–	μA
IDENTIFICATION (See Fig. 3)					
Input amplifier and demodulator					
Input voltage	$V_{5-9(p-p)}$	–	–	2,0	V
Min. input voltage	$V_{5-9(rms)}$	5,0	–	–	mV
Input resistance	R_{5-9}	500	–	–	kΩ
Gain	G_{25-9}	–	42	–	dB
Gain control range	ΔG	40	–	–	dB
Output voltage (gain-controlled)	$V_{25-9(p-p)}$	–	1,5	–	V
Operational amplifiers					
Input current	$I_{24, 28}$	–	70	–	nA
Gain at f = 200 Hz	G_{23-24}, G_{2-28}	78	–	–	dB
Output current	$I_{2, 23}$	1,5	–	–	mA
Output resistance	$R_{2, 23-9}$	–	2	–	kΩ
Output load capacitance	$C_{2, 23-9}$	–	–	30	pF
Schmitt trigger					
A.C. input signal	$V_{2, 23-9(rms)}$	–	1	–	V
Internal discharge resistors	$R_{1, 3-9}$	–	3	–	kΩ
A.F. STAGES					
Input resistance (pins 6, 8, 16 and 17)	R_{n-9}	10	–	–	kΩ
Gain ($V_{19, 20, 21, 22-9}/V_{6, 8-9}$)	G1	–	6	–	dB
Gain ($V_{19, 20, 21, 22-9}/V_{16, 17-9}$)	G2	–	0	–	dB
Input voltage	$V_{6, 8-9(rms)}$	–	1	–	V
Crosstalk attenuation (notes 3, 4 and 9)					
dual sound	α_{DS}	70	–	–	dB
stereo f = 250 Hz to 6,3 kHz	α_S	40	–	–	dB
stereo f = 40 Hz to 250 Hz; 6,3 kHz to 12,5 kHz	α_S	30	–	–	dB

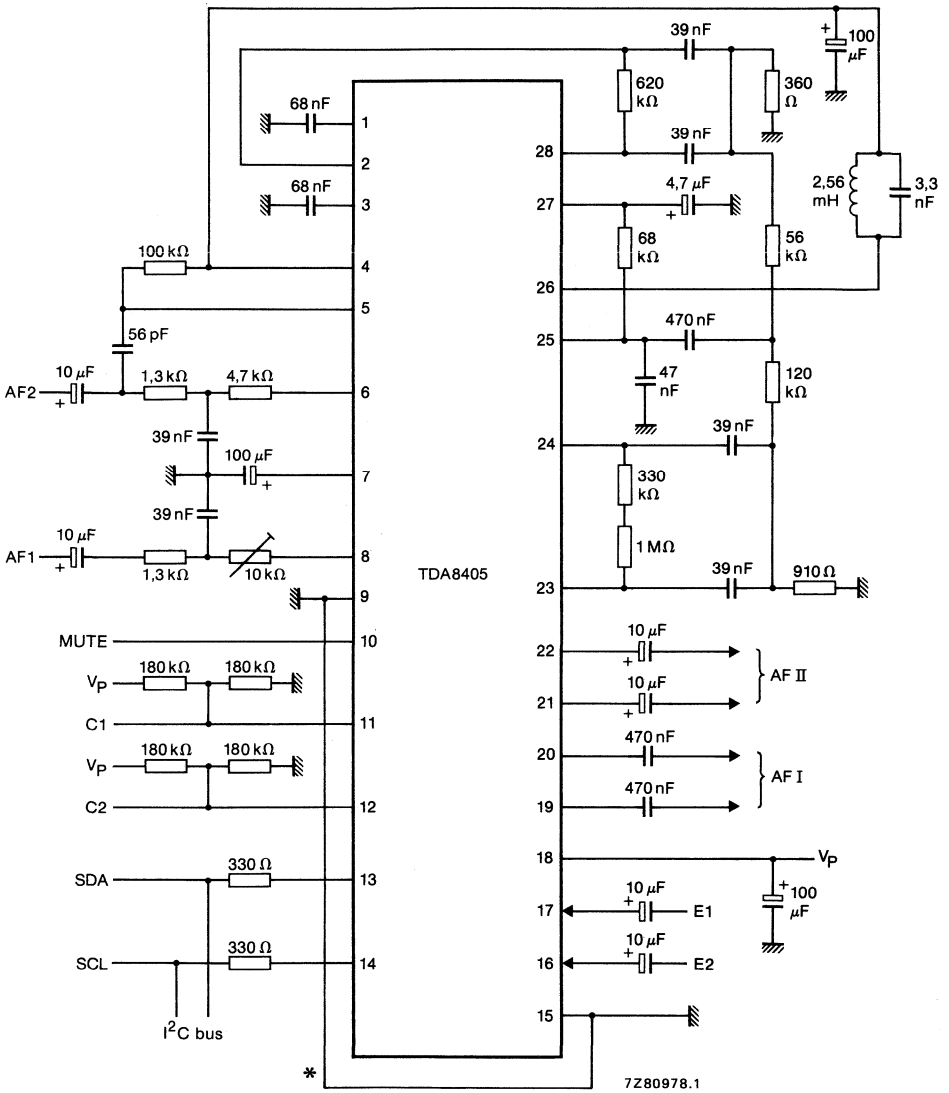
CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
A.F. STAGES (continued)					
Output resistance	$R_{19,20,21,22}$	–	200	300	Ω
Output load capacitance (pins 19, 20, 21 and 22)	$C_{n\text{-}9}$	–	–	1,5	nF
D.C. offsets (note 8) at pins 19,20,21 and 22	Δ_V	–	–	30	mV
Total harmonic distortion (notes 4 and 5)	THD	–	0,1	0,5	%
Output signal (r.m.s. value) (pins 19, 20, 21 and 22)	$V_{n\text{-}9(rms)}$	–	–	2,0	V
Ripple rejection (note 6)	RR	30	35	–	dB
Noise rejection (note 7) (noise from I^2C bus)	NR	80	–	–	dB
Signal-to-noise ratio (note 7)	(S+N)/N	70	–	–	dB
Ident signal suppression		70	–	–	dB
Signal suppression during mute (notes 4 and 7)		70	–	–	dB

Notes to the characteristics

1. Full specification of the I^2C bus will be supplied on request.
2. Programmable mute state. If the SC3 bit in the I^2C bus is LOW then the mute input is active LOW; if the mute bit is set to HIGH then the mute input is active HIGH.
3. Crosstalk attenuation definition: 20 log (unwanted output signal/input signal).
4. Frequency range: 40 Hz $<$ f $<$ 12,5 kHz.
5. In dual sound mode.
6. Test circuit as in Fig. 4: ripple rejection = output modulation due to hum on the supply line.
7. Related to 2 V (r.m.s.) output signal at pin 19, 20, 21 or 22; noise weighted according to CCIR 468/2.
8. Caused by any change of the switch position.
9. α_S measured without de-emphasis network.

DEVELOPMENT DATA



* Direct connection between pins 9 and 15 is needed.

Fig. 2 Test circuit.

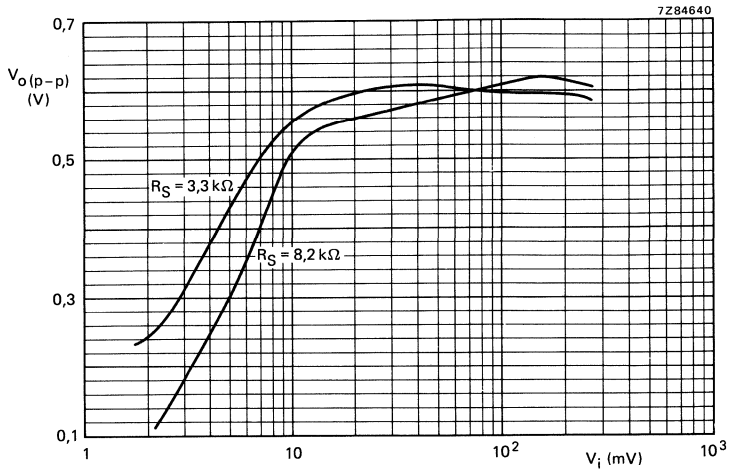


Fig. 3 Controlled output voltage as a function of the input signal (Q = 80); pilot frequency f_o = 54 kHz; R_S = source resistance.

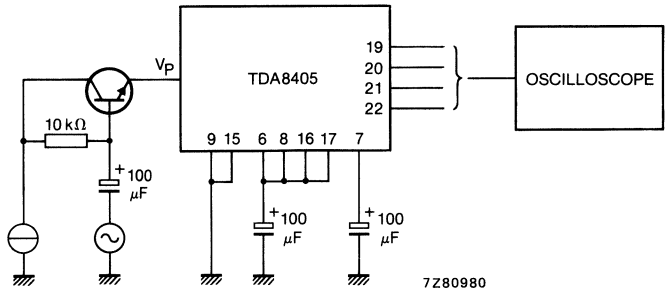
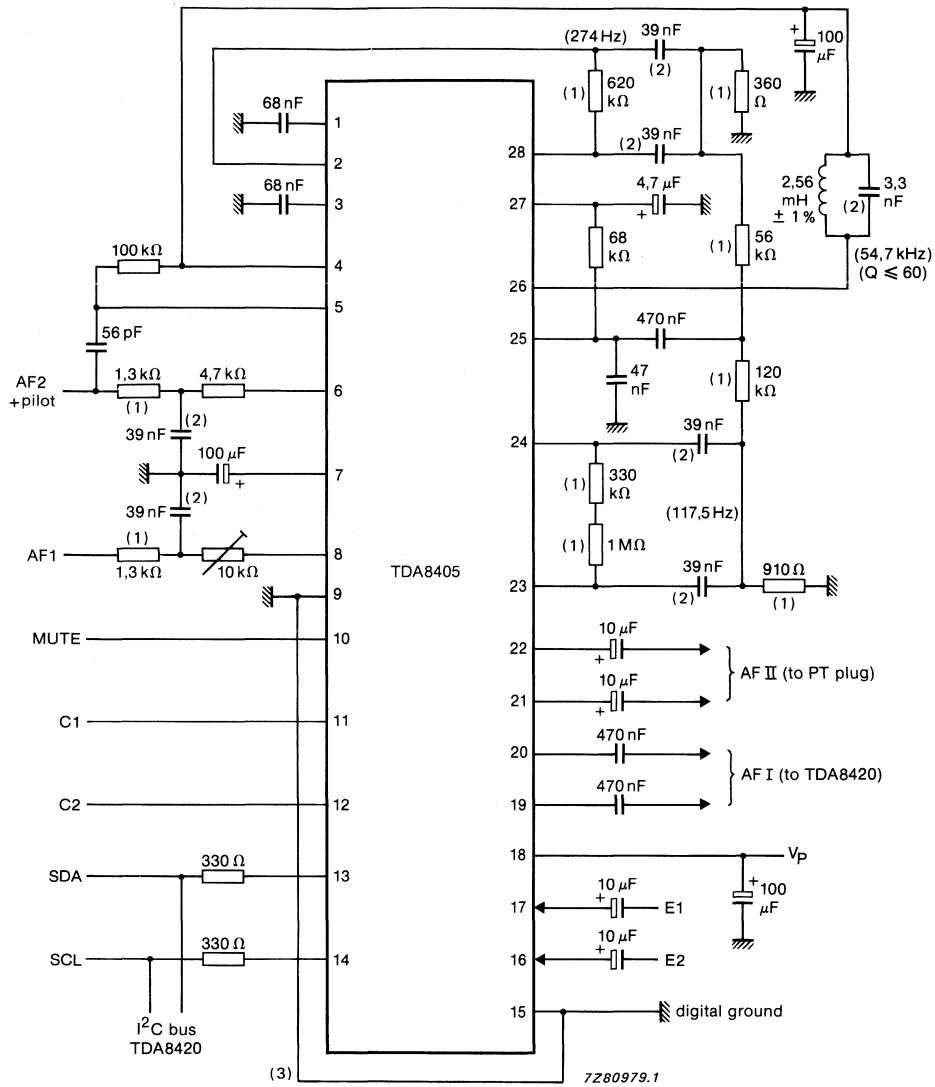


Fig. 4 Test circuit for ripple rejection: supply (d.c.) + pulse (r.m.s.) voltage at 100 Hz = 12 V + 50 mV.

DEVELOPMENT DATA



(1) ± 1 % tolerance

(2) polystyrene film/foil capacitors (KS) : ± 1 % tolerance

metallized polyethylenetherephthalate film capacitors (MKT) : ± 10 % tolerance

(3) Direct connection is needed between pins 9 and 15

Fig. 5 Application diagram.

TV AND VTR STEREO/DUAL SOUND PROCESSOR WITH INTEGRATED FILTERS AND I²C-BUS CONTROL

GENERAL DESCRIPTION

The TDA8415 is a processor of stereo/dual language signals (B/G-standard) for stereo sound television receivers and VTRs, using the switched-capacitor technique. The AF signals at the TDA8415 inputs must be "(L+R)/2" or "language A" on one channel and "R" or "language B" on the second channel (where L = left and R = right). The carrier frequency of the second channel is also modulated by an identification signal (stereo or dual sound). The device is controlled by a microcomputer via the two-line, bidirectional I²C-bus.

Features

- Use of the switched-capacitor technique for signal processing
- Small amount of peripheral components
- Integrated anti-aliasing filters
- Low distortion AF signal handling
- Integrated de-emphasis with a time constant of 50 μs
- Function and software are compatible with the TDA8405
- Two general purpose output ports
- Full ESD protection

QUICK REFERENCE DATA

parameter	condition	symbol	min.	typ.	max.	unit
Supply voltage (pin 15)		V_P	–	12	–	V
Supply current (pin 15)		I_P	–	10	–	mA
AF output signal (RMS value) (pins 11 to 14)		V_o	–	2	–	V
Weighted signal-to-noise ratio of the AF output signals (CCIR 468/3)		(S+W)/W	70	–	–	dB
Crosstalk attenuation						
stereo mode at	f = 1 kHz	α_S	40	–	–	dB
dual sound mode at	f = 40 Hz to 12.5 kHz	α_{DS}	70	–	–	dB
Pilot signal input sensitivity		V_i	–	2.5	–	mV
Total harmonic distortion		THD	–	0.1	–	%

PACKAGE OUTLINE

20-lead DIL; plastic (SOT146).

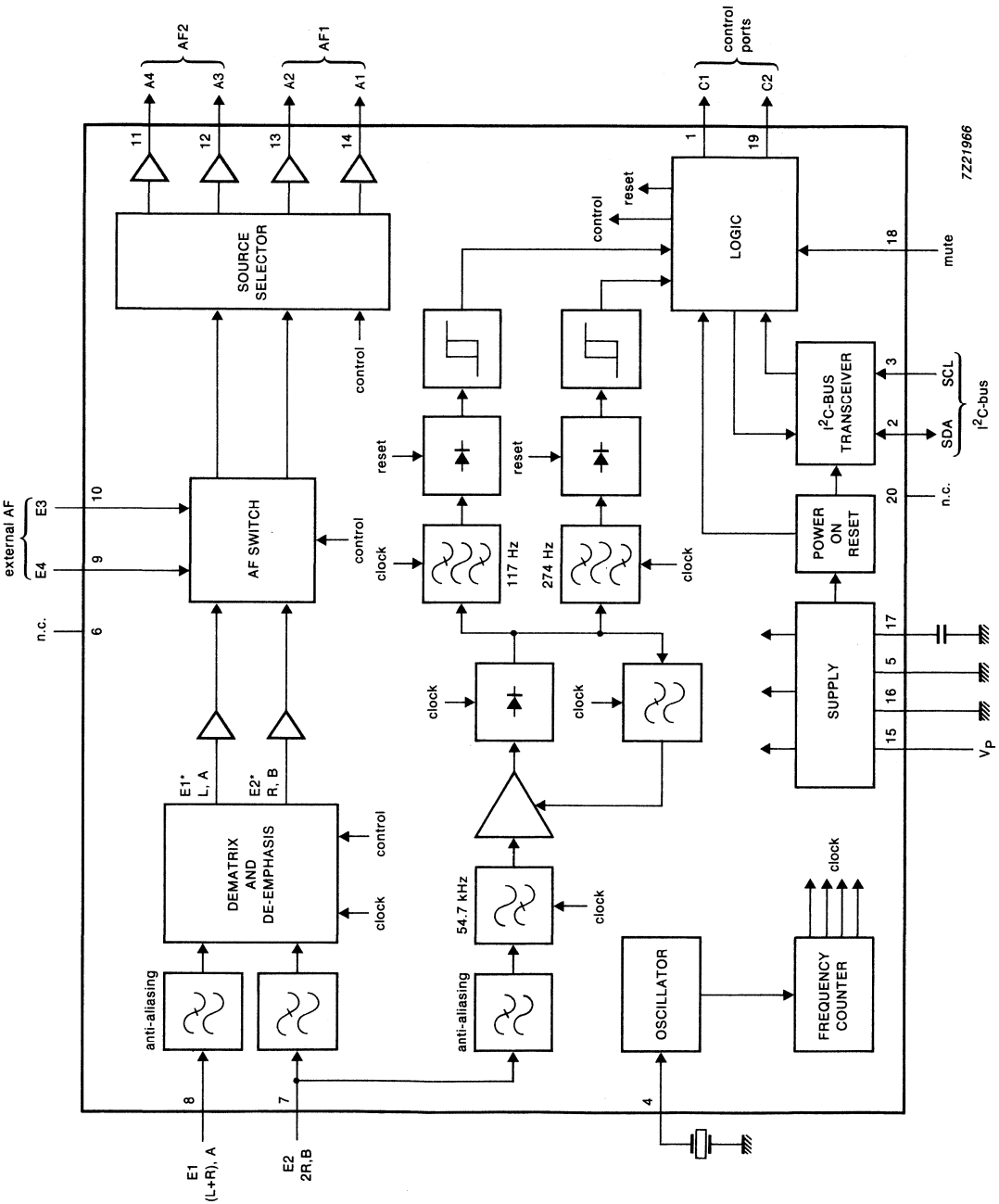


Fig.1 Block diagram.

DEVELOPMENT DATA

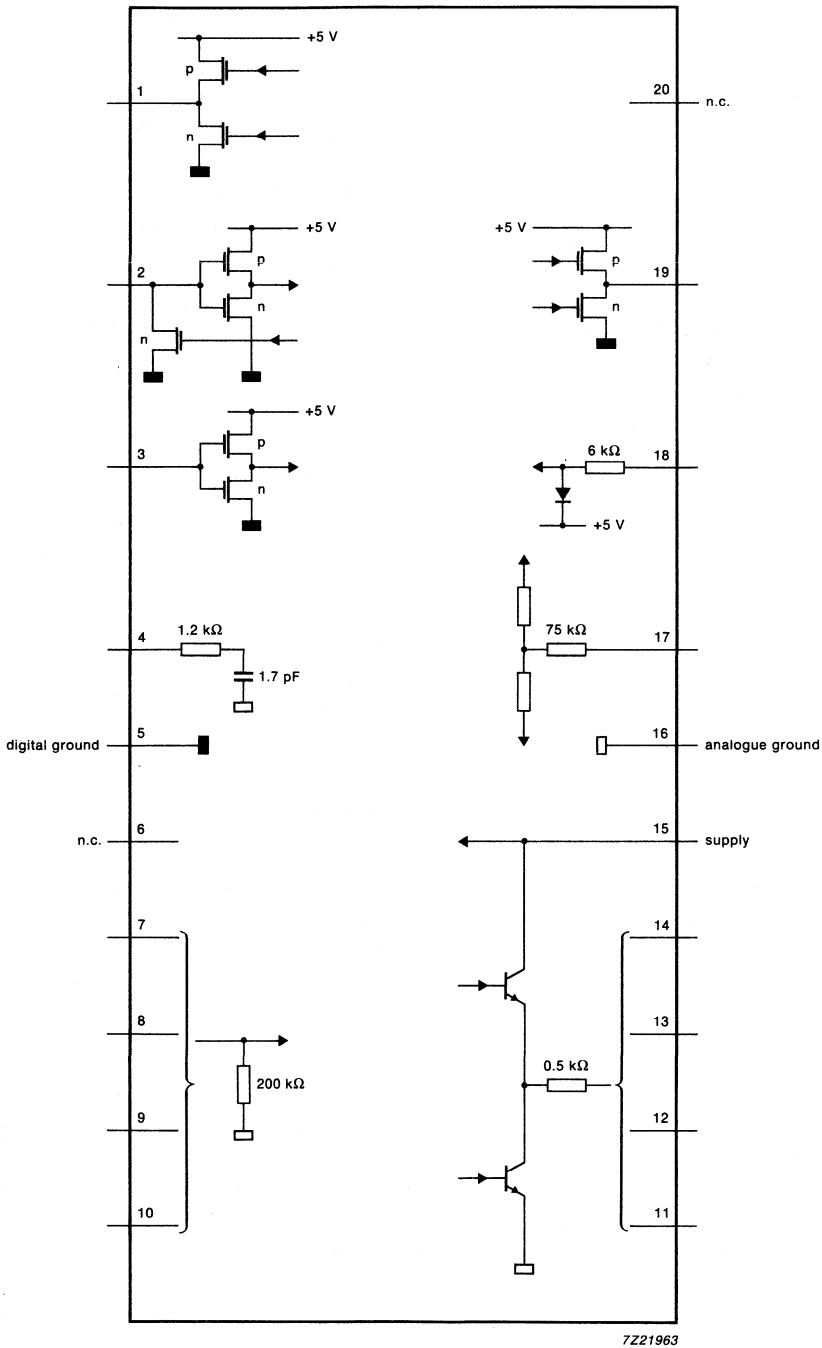


Fig.2 Input and output loading diagram.

PINNING

1 Control port C1
2 SDA, serial data line (I^2C-bus)
3 SCL, serial clock line (I^2C-bus)
4 Oscillator input (or quartz)
5 Digital ground (0 V)
6 Not connected, but reserved
7 Sound channel input AF2 (E2)
8 Sound channel input AF1 (E1)
9 External AF input (E4)
10 External AF input (E3)
11 Output A4 AF 2 output
12 Output A3 AF 2 output
13 Output A2 AF 1 output
13 Output A1 AF 1 output
15 Supply voltage V_P
16 Analogue ground (0 V)
17 Ripple rejection improvement
18 Mute input
19 Control port C2
20 Not connected, but reserved

FUNCTIONAL DESCRIPTION

Anti-aliasing filters

Frequency band limitation is performed by a second order Sallen and Key low-pass filter inserted in the AF signal path and the identification circuit. This limitation is necessary because of the time-discrete signal processing needed to meet the Nyquist criterium.

Identification

To enable the identification of the transmitted AF signal (mono, stereo or dual sound), the carrier frequency of the second channel (E2) is also modulated by an identification signal. The identification signal is a 54.6875 kHz pilot carrier signal which is 50% amplitude modulated by either a 117.4 Hz signal for stereo transmission or by a 274.1 Hz signal for dual sound transmission.

The identification section of the circuit consists of a 54 kHz high-pass filter followed by a gain controlled amplifier with an AM demodulator. The total gain of the high-pass filter and the amplifier is approximately 56 dB. The demodulated identification signal is filtered by the identification band-pass filters, (117.4 Hz for stereo transmission, 274.1 Hz for dual sound transmission). The output from either filter is converted to a DC signal by a peak detector and the necessary hysteresis is performed by a Schmitt-trigger. The resultant DC output signals indicate the status of the transmitter (mono, stereo or dual sound).

De-matrix and de-emphasis

Depending on the results of the identification circuit (mono, stereo or dual sound) the AF signals at the inputs E1 and E2 are converted to the signals at E1* and E2* as listed in Table 1.

Table 1 Transmitter status

transmitter status	E1	E2	E1*	E2*
mono	0.7(L+R)	–	2(L+R)	–
stereo	0.7(L+R)	2R	4L	4R
dual sound	0.7A	B	2A	2B

Where L = left channel signal; R = right channel signal; A = first sound channel signal and B = second sound channel signal.

This section of the circuit also performs the de-emphasis (50 μs time constant) with a high degree of accuracy.

AF switch

The AF switch is used to switch to either the internal sound sources (E1* or E1* and E2*) or, to the external sound source (E3 and E4) and is controlled via the I²C-bus.

Source selector

The source selector is used to connect the outputs from the AF switch to the outputs A1 to A4 as illustrated by Table 5. The selector is controlled via the I²C-bus.

Muting

In this mode the AF outputs A1 to A4 are muted, and the identification circuit is deactivated (mono). The muting is active after power-on reset or as a result of user control (via the mute input and bit CR3 of the control byte of the mute and port control register; see Table 4).

Sound mute

If the switch register is set to (00) hex, (sound mute) only the AF outputs are muted, the identification circuit is still active and can be read (status register) via the I²C-bus.

Power-on reset

The following actions are carried out by the internal power-on reset when it is active:

- The AF outputs are muted
- The identification circuit is deactivated (mono)
- The control ports (C1 and C2) are set LOW
- The I²C-bus transceiver is initialized

When the power-on reset becomes passive the following occurs:

- The AF outputs are kept in the mute state until the contents of the switch register are changed from (00) hex via the I²C-bus
- The identification circuit is activated
- The control ports are LOW until the mute and control port register is changed (CR bits 10, 11, 20 and 21)
- The I²C-bus transceiver is activated

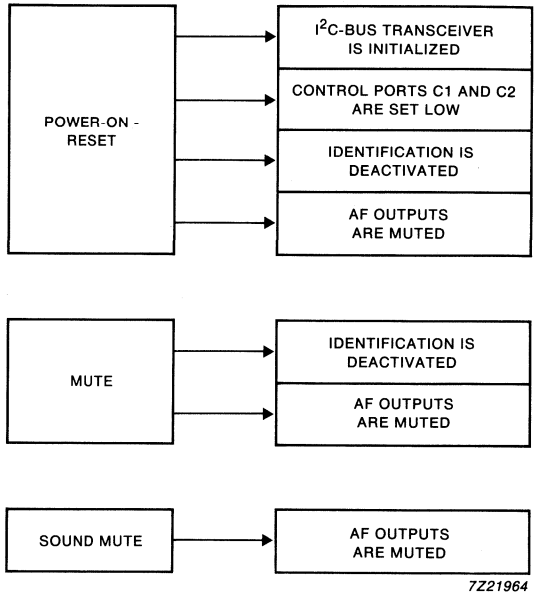


Fig.3 Mute modes.

Control ports

The general purpose control ports C1 and C2 can be set to LOW, HIGH or high impedance via the I²C-bus.

I²C-bus receiver and data handling

Bus specification

The TDA8415 is controlled, via the bidirectional 2-line I²C-bus, by a microcomputer. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

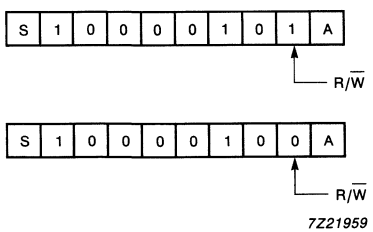
When the bus is free both lines are HIGH. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The set up and hold times are specified in the CHARACTERISTICS.

A HIGH-to-LOW transition of the SDA line while SCL is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the SDA line while SCL is HIGH is defined as the stop condition (P). The bus receiver will be reset on the reception of a start condition. The bus is considered to be busy after the start condition. The bus is considered to be free again after a stop condition.

The I²C-BUS PROTOCOL OF THE TDA8415

The TDA8415 is controlled by a microcomputer and can be written to or read from via the I²C-bus.

The first byte is the address and determines whether the TDA8415 is to be read from (status register) or written to (switch register or mute and port control register).



Read from (TDA8415 is a slave transmitter)

Write to (TDA8415 is a slave receiver)

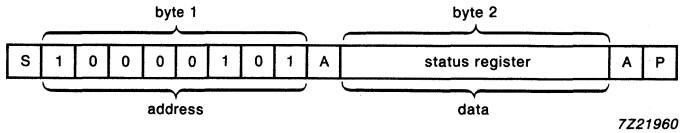
Where S = start bit and A = acknowledge bit

Fig.4 Address byte.

DEVELOPMENT DATA

Reading the TDA8415

Reading the TDA8415 means reading the status register and the data stream will have the format as illustrated in Fig.5 below.



Where S = start bit; A = acknowledge bit and P = stop bit

Fig.5 Read format.

The second byte, the contents of the status register, is defined by Table 2.

Table 2 Status register

D7	D6	D7	D5	D4	D3	D2	D1	D0
PONRES	ST	DS	0	0	0	0	0	0

PONRES = power on reset
1 = power on reset active after switching on or power breakdown
0 = after reading the status register
ST = stereo transmission
DS = dual sound transmission

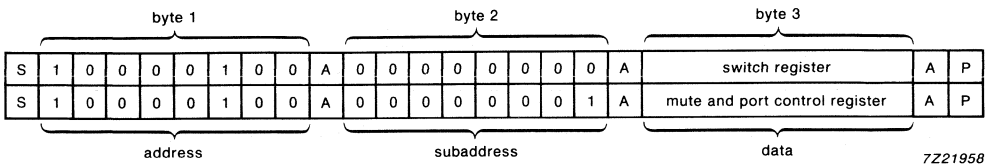
The truth table for the ST and DS bits is provided by Table 3.

Table 3 Truth table for ST and DS bits

ST	DS	definition
0	0	mono transmission
0	1	dual sound transmission
1	0	stereo transmission
1	1	not possible

Writing to the TDA8415

Writing to the TDA8415 means, writing to either the switch register or the mute and port control register. Which one is to be addressed is defined by the subaddress (the second byte) as illustrated by Fig.6 below. The third byte contains the information to be stored in the specified register.



Where S = start bit; A = acknowledge bit and P = stop bit

Fig.6 Write format.

Table 4 defines the contents of the mute and port control register.

Table 4 Mute and port control register

D7	D6	D5	D4 CR3	D3 CR21	D2 CR20	D1 CR11	D0 CR10	definition
X	X	X				0	0	control port C1 = LOW
X	X	X				0	1	control port C1 = HIGH
X	X	X				1	X	control port C1 = high impedance
X	X	X		0	0			control port C2 = LOW
X	X	X		0	1			control port C2 = HIGH
X	X	X		1	X			control port C2 = high impedance
X	X	X	0					mute is active when pin 18 is LOW (default)
X	X	X	1					mute is active when pin 18 is HIGH

Where: X = don't care.

DEVELOPMENT DATA

Table 5 defines the contents of the switch register.

Table 5 Switch register

switch register		input E1	E2	E3	E4	output A1	A2	A3	A4	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)
sound mute	–	–	–	–	–	no signal				0	0	0	0	0	0	0	0	(00)
mono	M	M	M	–	–	M	M	M	M	0	0	0	1	0	0	0	0	(10)
	St	L*	R	–	–	L*	L*	L*	L*	0	0	0	1	0	0	0	0	(10)
stereo	St	L*	R	–	–	L	R	L	R	0	0	1	0	1	0	1	0	(2A)
sound A	DS	A	B	–	–	A	A	A	A	0	0	0	1	0	0	0	0	(10)
sound B	DS	A	B	–	–	B	B	B	B	0	0	0	1	1	1	1	1	(1F)
dual sound	DS	A	B	–	–	A	A	B	B	0	0	0	1	1	1	0	0	(1C)
	DS	A	B	–	–	B	B	A	A	0	0	0	1	0	0	1	1	(13)
dual sound	DS	A	B	–	–	A	B	A	A	0	0	0	1	0	0	1	0	(12)
mix	DS	A	B	–	–	A	A	A	B	0	0	0	1	1	0	0	0	(18)
	DS	A	B	–	–	A	B	A	B	0	0	0	1	1	0	1	0	(1A)
	DS	A	B	–	–	B	B	A	B	0	0	0	1	1	0	1	1	(1B)
	DS	A	B	–	–	A	B	B	B	0	0	0	1	1	1	1	0	(1E)
external	–	–	–	E3	E4	E3	E3	E3	E3	0	1	1	1	0	0	0	0	(70)
	–	–	–	E3	E4	E4	E4	E4	E4	0	1	1	1	1	1	1	1	(7F)
	–	–	–	E3	E4	E3	E4	E3	E4	0	1	1	1	1	0	1	0	(7A)
	–	–	–	E3	E4	E4	E4	E3	E3	0	1	1	1	0	0	1	1	(73)
	–	–	–	E3	E4	E3	E3	E4	E4	0	1	1	1	1	1	0	0	(7C)
	–	–	–	E3	E4	E3	E4	E3	E3	0	1	1	1	0	0	1	0	(72)
	–	–	–	E3	E4	E3	E3	E3	E4	0	1	1	1	1	0	0	0	(78)
	–	–	–	E3	E4	E4	E4	E3	E4	0	1	1	1	1	0	1	1	(7B)
	–	–	–	E3	E4	E3	E4	E4	E4	0	1	1	1	1	1	1	0	(7E)

Where: M = mono; St = stereo. DS = dual sound; R = right; L = left; L* = (L+R)/2; A = sound A; B = sound B.

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

parameter	symbol	min.	typ.	max.	unit
Supply voltage*	$V_P = V_{15-16}$	–	–	13.2	V
Output current					
pins 11, 12, 13, 14	I_O	–	–	10	mA
pins 1 and 19 (sink)	I_O	–	–	7	mA
(source)	$-I_O$	–	–	3	mA
Input voltage (not pin 18)	V_I	0	–	V_P	V
Input voltage pin 18	$V_I = V_{18-16}$	–	–	7	V
Output voltage	V_O	0	–	V_P	V
Total power dissipation	P_{tot}	–	–	1	W
ESD protection (each pin) (0 Ω/200 pF)		500	–	–	V
Operating ambient temperature range	T_{amb}	0	–	+ 70	°C
Storage temperature range	T_{stg}	–40	–	+ 150	°C

DEVELOPMENT DATA

* Supply voltage may be applied only when both pins 5 and 15 are connected to ground.

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C. Measurement conditions (see Fig.7): reference level is 1 V (RMS); test frequency = 3.183 kHz; noise measurement in accordance with DIN 45405, CCIR 468-3; oscillator frequency = 10 MHz; pre-emphasis time constant = 50 μs.

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage		$V_P = V_{15-16}$	10.8	12	13.2	V
Supply current		$I_P = I_{15}$	–	10	–	mA
DC levels						
pins 7 - 14 and 17		V_{n-16}	–	3.25	–	V
pin 4		V_{4-5}	–	2	–	V
Bus transceiver						
Clock frequency (I^2C-bus)	note 1	f_{CLK}	0.7	–	100	kHz
Clock SCL (pin 3)						
Input voltage LOW		V_{IL}	−0.3	–	1.5	V
Input voltage HIGH		V_{IH}	3	–	5	V
Timing LOW period		t_{LOW}	4.7	–	–	μs
Timing HIGH period		t_{HIGH}	4	–	–	μs
Rise time		t_r	–	–	1	μs
Fall time		t_f	–	–	0.3	μs
Input current LOW		$-I_{IL}$	–	–	10	μA
Input current HIGH		I_{IH}	–	–	10	μA
Data SDA (pin 2)						
Input voltage LOW		V_{IL}	−0.3	–	1.5	V
Input voltage HIGH		V_{IH}	3	–	5	V
Rise time		t_r	–	–	1	μs
Fall time		t_f	–	–	0.3	μs
Data set-up time		$t_{SU;DAT}$	0.25	–	–	μs
Input current LOW		$-I_{IL}$	–	–	10	μA
Input current HIGH		I_{IH}	–	–	10	μA
Output current LOW		I_{OL}	3	–	–	mA

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Mute port (pin 18)						
Input voltage LOW	note 2	V_{IL}	−0.3	–	1.5	V
Input voltage HIGH	note 2	V_{IH}	3	–	5	V
Control ports (pins 1 and 19)						
Output voltage LOW	note 3	V_{OL}	–	–	0.5	V
Output voltage HIGH	note 3	V_{OH}	4.5	–	5	V
Output impedance	3-state	Z_o	1	–	–	MΩ
Output current LOW		I_{OL}	1	–	–	mA
Output current HIGH		$-I_{OH}$	1	–	–	mA
AF stages and identification (pins 7 to 14)						
Input impedance (pins 7 to 10)		Z_i	150	200	–	kΩ
Input voltage E1		V_I	–	–	0.7	V
Input voltage E2		V_I	–	–	1	V
Input voltage E2 for identification active (RMS value)	note 4	V_i	2.5	–	–	mV
Voltage gain 7-15/output	note 5	G_v	5.9	6	6.1	dB
Voltage gain 8-15/output	note 5	G_v	8.9	9	9.1	dB
Voltage gain 9, 10-15/output		G_v	−0.1	0	0.1	dB
Crosstalk attenuation	notes 6 to 8					
dual mode		α_{ds}	70	75	–	dB
stereo mode		α_s	30	50	–	dB

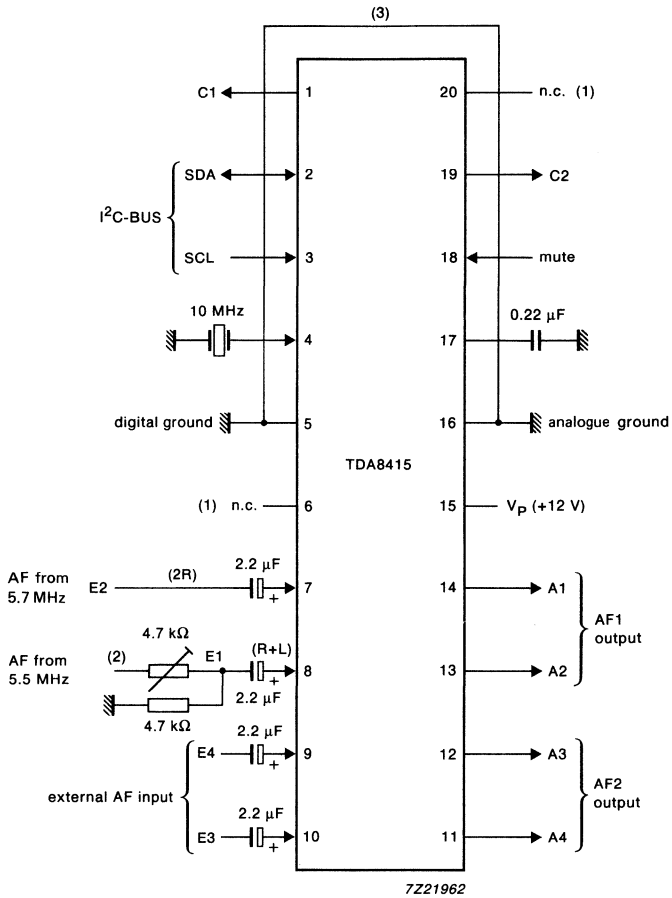
CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
AF stages and identification (continued)						
Output impedance (pins 11 to 14)		Z_o	400	500	600	Ω
De-emphasis time constant	note 9		49.5	50	50.5	μs
Frequency response	note 6	Δf	−1	–	1	dB
Total harmonic distortion	note 10	THD	–	–	0.2	%
Capacitive load (pins 11 to 14)		C_L	–	–	1.5	nF
Output signal (RMS value) (pins 11 to 14)	THD ⩽ 0.2%	V_o	–	–	2	V
Ripple rejection	note 11	RR	50	66	–	dB
Noise from I²C-bus		NR	–	–	−80	dB
Signal-to-noise ratio		(S+W)/W	70	–	–	dBV CCIR
Signal suppression during mute	note 6	SS	70	75	–	dB
Change of output DC voltage level between any two modes			–	–	30	mV
Oscillator						
Oscillator frequency		f_{OSC}	–	10	–	MHz
External oscillator signal (RMS value)		V_{4-5}	1.7	–	–	V
Quartz series resistor		R1	–	–	100	Ω
Impedance		Z_i	–	−1.2 + j9.3	–	kΩ
Capacitance		C_{OSC}	–	1.7	–	pF

Notes to the characteristics

1. Full specification of I²C-bus will be supplied on request.
2. Programmable mute state. If the CR3 bit of the mute and port control register is LOW, the mute is active LOW; if it is HIGH, the mute input is active HIGH.
3. Output current $I_O \approx 1$ mA.
4. Unmodulated.
5. f = 400 Hz; R_L = 1 MΩ.
6. 40 Hz $\leqslant$ f $\leqslant$ 15 kHz.
7. In dual mode: A(B)-signal into B(A)-channel.
   In stereo mode: R-signal into left, L-signal = 0, reference is 1 V RMS.
8. Source impedance $|Z_S| < 1$ kΩ.
9. Equivalent to an output level of −3 dB at f = 3.183 kHz.
10. V_O = 1 V RMS; f = 1 kHz.
11. Test circuit see Fig.7.

DEVELOPMENT DATA

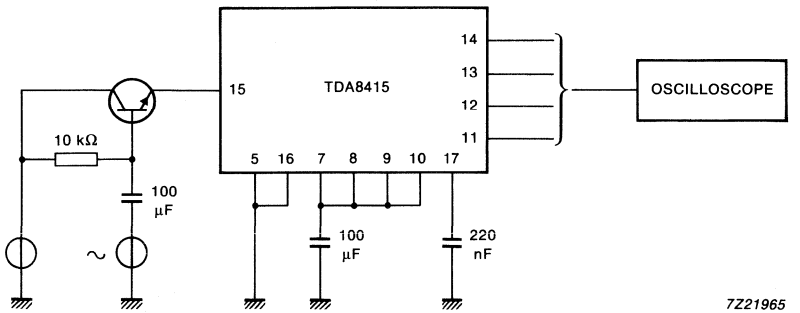


(1) These pins are not connected internally and should not be connected on the printed circuit board in order to maintain compatibility with future devices.

(2) This potentiometer has to be adjusted to achieve the best stereo separation.

(3) Direct connection between pins 5 and 16 is needed.

Fig.7 Application and test circuit.



Voltage input = supply voltage + pulse voltage at 70 Hz = 12 V ± 50 mV (p-p).

Fig.8 Ripple rejection test circuit.

DEVELOPMENT DATA

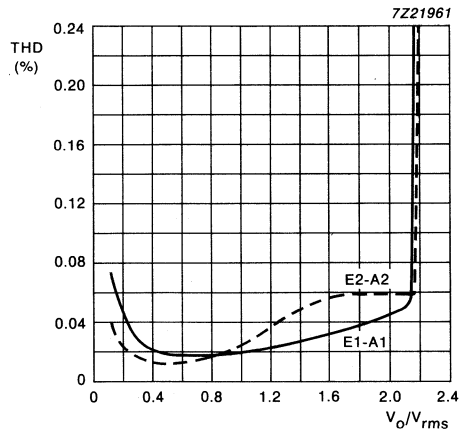


Fig.9 Total harmonic distortion diagram (stereo mode).

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

HI-FI STEREO AUDIO PROCESSOR; I²C BUS

GENERAL DESCRIPTION

The TDA8420 is a monolithic bipolar integrated stereo sound circuit with a loudspeaker channel (CH1) and a headphone channel (CH2), digital controlled via the I²C bus, for application in hi-fi audio and television sound.

Features

- Input selector
- Mode selector
- Loudspeaker channel (CH1) } with volume control, balance control and mute
- Headphone channel (CH2) }
- Pseudo stereo and spatial function
- Bass and treble control

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_{CC}	7,5	12	14	V
Input signal handling	V_I	2	–	–	V
Input sensitivity full power at the output stage	V_i	–	200	–	mV
Signal plus noise-to-noise ratio	(S+N)/N	–	90	–	dB
Total harmonic distortion	THD	–	0,05	–	%
Channel separation	α	–	75	–	dB
Volume control range CH1	G	–46	–	16	dB
Treble control range	G	–12	–	12	dB
Bass control range	G	–12	–	15	dB
Volume control range CH2	G	–62	–	0	dB

PACKAGE OUTLINE

28-lead dual in-line; plastic (SOT117).

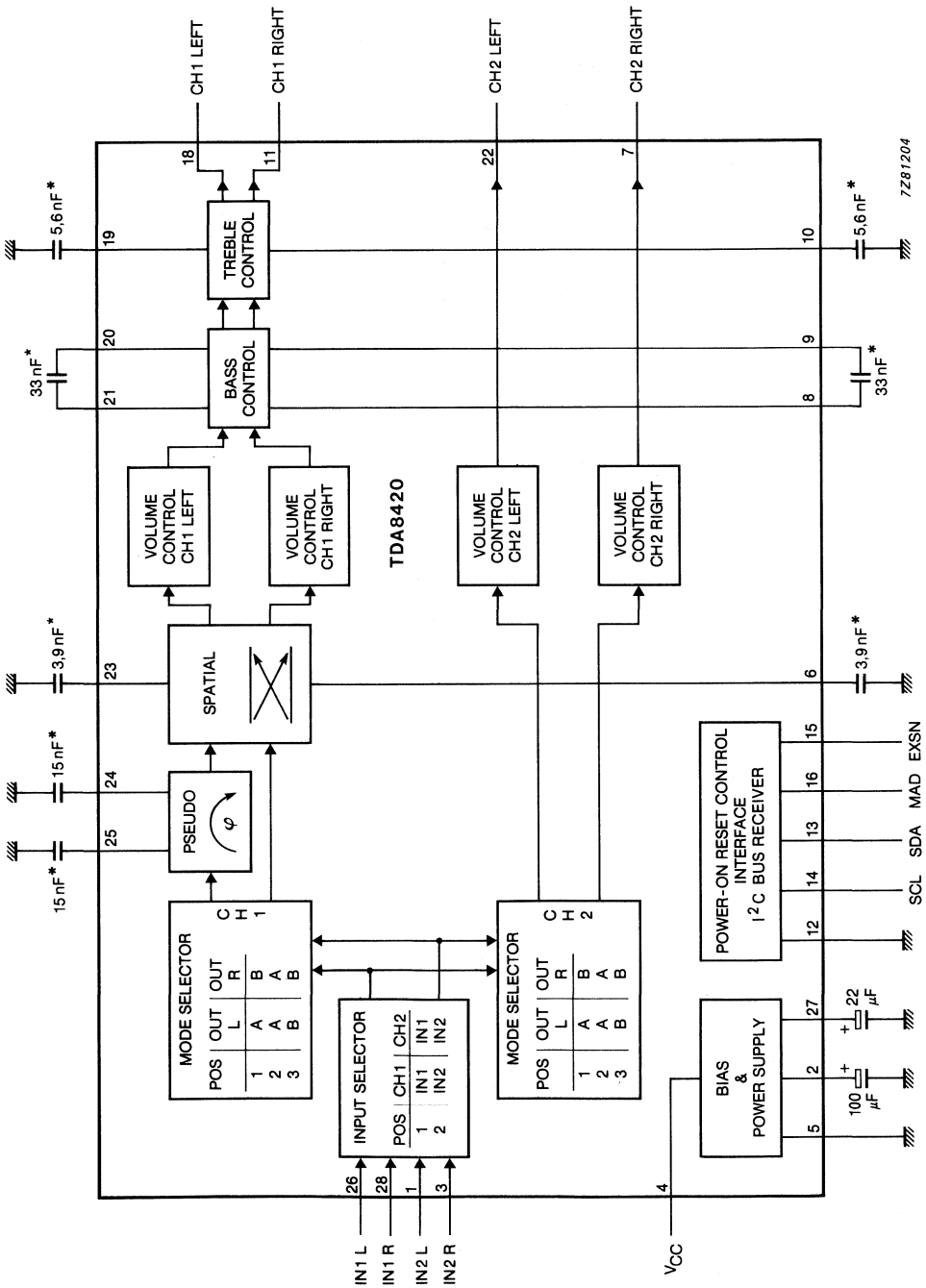


Fig. 1 Block diagram.

* These values are dependent on the required frequency response and effect.

PINNING

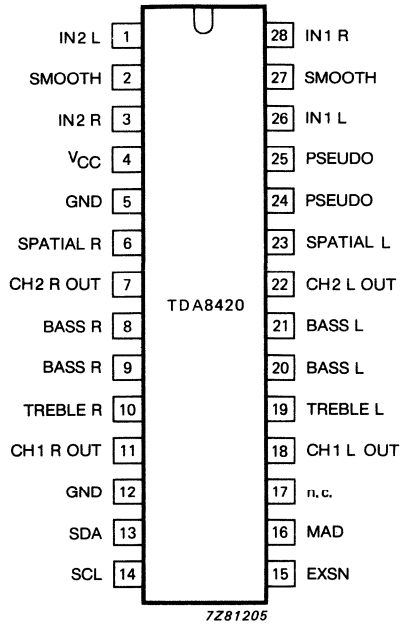


Fig. 2 Pinning diagram.

FUNCTIONAL DESCRIPTION

Input selector

The input to channel 1 (CH1) and channel 2 (CH2) is determined by the input selector. The selection is made from the following AF input signals:

- IN1 L (pin 26); IN1 R (pin 28)
  or
- IN2 L (pin 1); IN2 R (pin 3)

Where IN1 is an internal input signal and IN2 an external input signal.

Mode selector

For each channel (CH1 and CH2) there is a mode selector which selects between stereo, sound A and sound B in the event of bilingual transmission. Both mode selectors can be controlled independently.

Headphone channel (CH2)

Volume control and balance

The stages for volume control for CH2 consist of two parts for left and right. In each part the gain can be adjusted between 0 and −62 dB in steps of 2 dB. An additional step allows an attenuation of $\geqslant$ 90 dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right.

Loudspeaker channel (CH1)

Volume control and balance

The loudspeaker channel (CH1) also consists of two parts for volume control (left and right). In each part the gain can be adjusted between + 16 dB and −62 dB in steps of 2 dB. An additional step allows an attenuation of $\geqslant$ 90 dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right.

Stereo/pseudo stereo/spatial stereo mode

It is possible to select three modes. Stereo, pseudo or spatial stereo. The pseudo stereo mode receives mono transmissions and the stereo and spatial stereo mode receives stereo transmissions.

Bass control

The bass control stage can be switched from an emphasis of 15 dB to an attenuation of 12 dB for low frequencies in steps of 3 dB.

Treble control

The treble control stage can be switched from + 12 dB to −12 dB in steps of 3 dB.

Bias and power supply

The TDA8420 includes a bias and power supply stage, which generates a voltage of ½ V_{CC} with a low output impedance and injector currents for the logic part.

Power-on reset

The on-chip power-on reset circuit sets the mute bit to active, which mutes both the loudspeaker channel (CH1) and the headphone channel (CH2). The muting can be switched by transmission of the mute bit.

I^2C bus receiver and data handling

Bus specification

The TDA8420 is controlled via the 2-wire I^2C bus by a microcomputer. The two wires (SDA — serial data, SCL — serial clock) carry information between the devices connected to the bus. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull up resistor.
When the bus is free both lines are HIGH. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The set up and hold times are specified in AC CHARACTERISTICS.

A HIGH-to-LOW transition of the SDA line while SCL is HIGH is defined as a start condition.
A LOW-to-HIGH transition of the SDA line while SCL is HIGH is defined as a stop condition.
The bus receiver will be reset by the reception of a start condition. The bus is considered to be busy after the start condition. The bus is considered to be free again after a stop condition.

Module address

Data transmission to the TDA8420 starts with the module address MAD.

MSB								LSB
1	0	0	0	0	0	MAD	R/W	ACK

Fig. 3 TDA8420 module address.

The module address is determined by pin 16. When connected to ground MAD = 0; when connected to V_{CC} MAD = 1. Thus two TDA8420s can be selected within a system.

Subaddress

After the module address byte a second byte is used to select the functions for both channels:

- CH1 – Volume left, volume right, bass, treble and switch functions
- CH2 – Volume left, volume right and switch functions

The subaddress SAD is stored within the TDA8420. Table 1 defines the coding of the second byte after the module address MAD.

Table 1 Second byte after module address MAD

		128	64	32	16	8	4	2	1
	function	MSB 7	6	5	4	3	2	1	LSB 0
CH1	volume left	0	0	0	0	0	0	0	0
	volume right	0	0	0	0	0	0	0	1
	bass	0	0	0	0	0	0	1	0
	treble	0	0	0	0	0	0	1	1
	switch functions	0	0	0	0	1	0	0	0
CH2	volume left	0	0	0	0	0	1	0	0
	volume right	0	0	0	0	0	1	0	1
	switch functions	0	0	0	0	1	1	0	0
						subaddress SAD			

Definition of 3rd byte

A third byte is used to transmit data to the TDA8420. Table 2 defines the coding of the third byte after module address MAD and subaddress SAD.

Table 2 Third byte after module address MAD and subaddress SAD

	function		MSB 7	6	5	4	3	2	1	LSB 0
	volume left	VL1	1	1	V05	V04	V03	V02	V01	V00
	volume right	VR1	1	1	V15	V14	V13	V12	V11	V10
CH1	bass	BA	1	1	1	1	BA3	BA2	BA1	BA0
	treble	TR	1	1	1	1	TR3	TR2	TR1	TR0
	switch functions	S1	1	1	MU	EFL	STL	ML1	ML0	IS
	volume left	VL2	1	1	V25	V24	V23	V22	V21	V20
CH2	volume right	VR2	1	1	V35	V34	V33	V32	V31	V30
	switch functions	S2	1	1	1	1	EXS	MH1	MH0	1

Truth tables

Truth tables for the switch functions

Table 3 Input selector

function	IS
IN1	0
IN2	1

Table 4 Mode selectors

	CH1		CH2	
mode	ML0	ML1	MH0	MH1
stereo	1	1	1	1
sound A	1	0	1	0
sound B	0	1	0	1
----------	0	0	0	0

Table 5 Stereo/pseudo stereo/spatial stereo

choice	STL	EFL
spatial	1	1
stereo	1	0
pseudo	0	1
----------	0	0

Table 6 Mute

mute	MU
active; automatic after POR*	1
not active	0

Table 7 Output for external switch

EXSN	EXS
ground	1
open collector	0

Where: POR = Power-On Reset.

Truth tables for the volume base and treble controls.

Table 8 Volume control

CH1	CH2	Vx5	Vx4	Vx3	Vx2	Vx1	Vx0
16	0	1	1	1	1	1	1
–46	–62	1	0	0	0	0	0
⩽ –90	⩽ –90	0	1	1	1	1	1
⩽ –90	⩽ –90	0	0	0	0	0	0

Where: The values of CH1 and CH2 are in 2 dB/step measured in dBs.

* Attenuation ⩾ 90 dB.

Table 9 Bass control

3dB/step (dB)	BA3	BA2	BA1	BA0
15	1	1	1	1
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
15	1	0	1	1
12	1	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
0	0	1	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	0	0

Table 10 Treble control

3dB/step (dB)	TR3	TR2	TR1	TR0
12	1	1	1	1
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
12	1	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
0	0	1	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	0	0

Sequence of data transmission

After a power-on reset all eight functions have to be adjusted with eight data transmissions. It is recommended that data information for switch functions in CH1 are transmitted last because all functions have to be adjusted when the muting is switched off. The sequence of transmission of other data information is not critical.

The order of data transmission is shown in Figures 4 and 5. The number of data transmissions is unrestricted but before each data byte the module address MAD and the correct subaddress SAD is required.

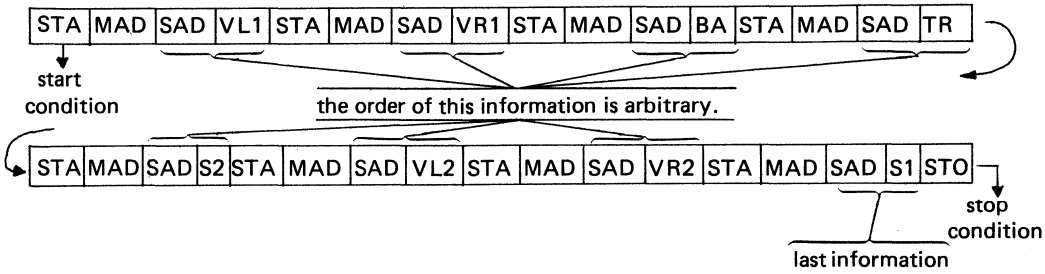


Fig. 4 Data transmission after a power-on reset.

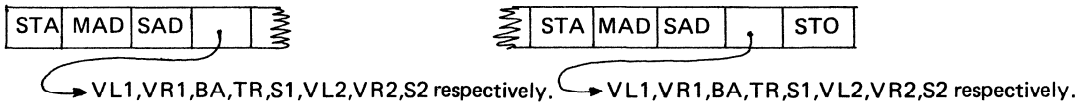


Fig. 5 Data transmission except after power-on reset.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{CC}	0	16	V
Voltage range for external capacitors				
pins 2, 6, 8 to 10, 19 to 21, 23 to 25, 27	V_{cap}	0	V_{CC}	V
pin 13	V_{SDA}	0	V_{CC}	V
pin 14	V_{SCL}	0	V_{CC}	V
pin 15	V_{EXSN}	0	V_{CC}	V
pin 16	V_{MAD}	0	V_{CC}	V
Input voltage range				
at pins 1, 3, 7, 11, 18, 22, 26, 28	V_I	0	V_{CC}	V
Output voltage range				
at pins 1, 3, 7, 11, 18, 22, 26, 28	V_O	0	V_{CC}	V
Output current at pins 7, 11, 18, 22	I_O	–	45	mA
Total power dissipation				
at $T_{amb} < 70\ ^oC$	P_{tot}	–	1350	mW
Operating ambient temperature range	T_{amb}	0	70	^oC
Storage temperature range	T_{stg}	–25	150	^oC

DC CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_{CC}	7,5	12	14	V
Supply current at V_{CC} = 12 V	I_{CC}	–	42	55	mA
Input voltage IN1 L, IN1 R, IN2 L, IN2 R DC voltage internally generated; capacitive coupling recommended	V_I	5,4	6,0	6,6	V
MAD (pin 16)					
input voltage HIGH	V_{IH}	3,0	–	V_{CC}	V
input voltage LOW	V_{IL}	0	–	1,5	V
input current HIGH	I_{IH}	–	–	1,0	μA
input current LOW	I_{IL}	–	1	10	μA
SDA; SCL (pins 13 and 14)					
input voltage HIGH	V_{IH}	3,0	–	V_{CC}	V
input voltage LOW	V_{IL}	−0,3	–	1,5	V
input current HIGH	I_{IH}	–	–	1,0	μA
input current LOW	I_{IL}	–	1	10	μA
Output voltage CH1 (pins 11 and 18); CH2 (pins 7 and 22)	V_O	5,4	½ V_{CC}	6,6	V
External capacitors					
pins 6 to 10; 19 to 21; 23 to 25	$V_{cap.n}$	–	½ V_{CC}	–	V
pin 2	$V_{cap.2}$	–	V_{CC}−0,1	–	V
External switch (pin 15) at I_{EXSN} = 1 mA					
Output voltage HIGH	V_{EXSNH}	–	–	16	V
Output voltage LOW	V_{EXSNL}	–	–	0,3	V

AC CHARACTERISTICS

V_{CC} = 12 V; bass/treble in linear position; pseudo and spatial stereo off; $R_L > 10$ kΩ; $C_L < 100$ pF; T_{amb} = 25 °C unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
I²C bus timing (see Fig. 6)					
SDA, SCL (pin 13 and 14)					
Clock frequency range	f_{SCL}	0	–	100	kHz
The HIGH period of the clock	t_{HIGH}	4	–	–	μs
The LOW period of the clock	t_{LOW}	4,7	–	–	μs
SCL rise time	t_r	–	–	1	μs
SCL fall time	t_f	–	–	0,3	μs
Set-up time for start condition	$t_{SU;STA}$	4,7	–	–	μs
Hold time for start condition	$t_{HD;STA}$	4	–	–	μs
Set-up time for stop condition	$t_{SU;STO}$	4,7	–	–	μs
Time bus must be free before a new transmission can start	t_{BUF}	4,7	–	–	μs
Set-up time DATA	$t_{SU;DAT}$	250	–	–	ns
Input signals					
IN1 L (pin 26) IN1 R (pin 28) IN2 L (pin 1) IN2 R (pin 3)					
Input signal handling (r.m.s. value) at V_u = −4 dB; THD ⩽ 0,5%	$V_{i(rms)}$	2	–	–	V
Input resistance	R_{n-5}	35	50	–	kΩ
Frequency response (−0,5 dB) bass and treble in linear position; stereo mode; effects off	f	20	–	20 000	Hz

AC CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
LOUDSPEAKER CHANNEL OUTPUTS					
CH1 LEFT (pin 18); CH1 RIGHT (pin 11)					
Output voltage range (r.m.s. value) at THD $\leqslant$ 0,5%	$V_{o(rms)}$	2	–	–	V
Load resistance	R_L	10	–	–	kΩ
Output impedance	Z_O	–	–	100	Ω
Noise level weighted according to CCIR468-2					
gain = 16 dB	V_n	–	90	–	μV
gain = 0 dB	V_n	–	20	40	μV
gain = $\leqslant$ –90 dB	V_n	–	15	–	μV
Total harmonic distortion (f = 20 Hz to 12,5 kHz)					
for $V_{i(rms)}$ = 0,5 V; gain = + 16 dB to –30 dB	THD	–	0,05	0,2	%
for $V_{i(rms)}$ = 1,0 V; gain = + 2 dB to –30 dB	THD	–	0,07	0,2	%
for $V_{i(rms)}$ = 2,0 V; gain = –4 dB to –30 dB	THD	–	0,1	–	%
Channel separation at 10 kHz gain = 0 dB	α_{cr}	–	75	–	dB
Ripple rejection (gain = 0 dB; bass and treble in linear position) f_{ripple} = 100 Hz	RR_{100}	–	50	–	dB
Crosstalk attenuation from logic inputs to AF outputs (gain = 0 dB; bass and treble in linear position)	α_L	–	110	–	dB
VOLUME CONTROL					
For truth table see Table 8					

parameter	symbol	min.	typ.	max.	unit
Loudspeaker channel (CH1)					
Control range at f = 1 kHz					
maximum voltage gain (16 dB step)	G_{max}	15	–	–	dB
minimum voltage gain (–46 dB step)	G_{min}	–43	–	–	dB
last position	G_{off}	–80	–85	–	dB
mute position	G_{mute}	–85	–90	–	dB
Resolution	G_{step}	–	2	–	dB/step
Gain difference between left and right AF channel (note 1)					
gain from 16 dB to –30 dB	ΔG	–	–	0,5	dB
gain from –30 dB to –46 dB	ΔG	–	–	1	dB
TREBLE CONTROL (CH1)					
For truth table see Table 10					
Control range for $C_{10\text{-}5}$; $C_{19\text{-}5}$ = 5,6 nF					
Maximum emphasis at 15 kHz with respect to linear position	G	11	12	13	dB
Maximum attenuation at 15 kHz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	–	3	–	dB/step
BASS CONTROL					
For truth table see Table 9					
Control range for $C_{8\text{-}9}$; $C_{20\text{-}21}$ = 33 nF					
Maximum emphasis at 40 kHz with respect to linear position	G	14	15	16	dB
Maximum attenuation at 40 kHz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	–	3	–	dB/step
SPATIAL AND PSEUDO FUNCTION					
Spatial:					
Antiphase crosstalk	α	–	50	–	%
Pseudo:					
Phase shift			(see Fig. 15)		

AC CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
HEADPHONE CHANNEL OUTPUTS					
CH2 LEFT (pin 22); CH2 RIGHT (pin 7)					
Output voltage range (r.m.s. value) at THD ⩽ 0,5%	$V_{o(rms)}$	2	–	–	V
Load resistance	R_L	10	–	–	kΩ
Output impedance	Z_O	–	–	100	Ω
Noise level (weighted according to CCIR468-2)					
gain = 0 dB	V_n	–	15	–	μV
gain = 16 dB	V_n	–	12	25	μV
gain = ⩽ –90 dB	V_n	–	10	–	μV
Total harmonic distortion (f = 20 Hz to 12,5 kHz)					
for $V_{i(rms)}$ = 0,2 V; gain = 0 dB to –30 dB	THD	–	0,01	0,2	%
for $V_{i(rms)}$ = 1,0 V; gain = 0 dB to –30 dB	THD	–	0,1	–	%
for $V_{i(rms)}$ = 2,0 V gain = –4 dB to –30 dB	THD	–	0,3	–	%
Channel separation at 10 kHz gain = 0 dB	α_{cr}	–	75	–	dB
Ripple rejection (gain = 0 dB; bass and treble in linear position) f_{ripple} = 100 Hz	RR_{100}	–	50	–	dB
Crosstalk attenuation from logic inputs to AF outputs (gain = 0 dB; bass and treble in linear position)	α_L	–	110	–	dB
Crosstalk between any input/output f = 100 Hz to 12,5 kHz	α	65	70	–	dB
Crosstalk IN1/IN2 gain = 0 dB; R_G = 0	α	95	100	–	dB

parameter	symbol	min.	typ.	max.	unit
Headphone channel (CH2)					
Control range					
maximum voltage gain (0 dB step)	G_{max}	−1	–	–	dB
minimum voltage gain (−62 dB step)	G_{min}	−57	–	–	dB
last position	G_{off}	−80	−85	–	dB
mute position	G_{mute}	−85	−90	–	dB
Resolution	G_{step}	–	2	–	dB/step
Gain difference between left and right AF channel (note 1)					
gain from 0 dB to −40 dB	ΔG	–	–	0,5	dB
gain from −40 dB to −62 dB	ΔG	–	–	2	dB

Note to the AC characteristics

1. Balance is realized via software by different volume settings in both channels.

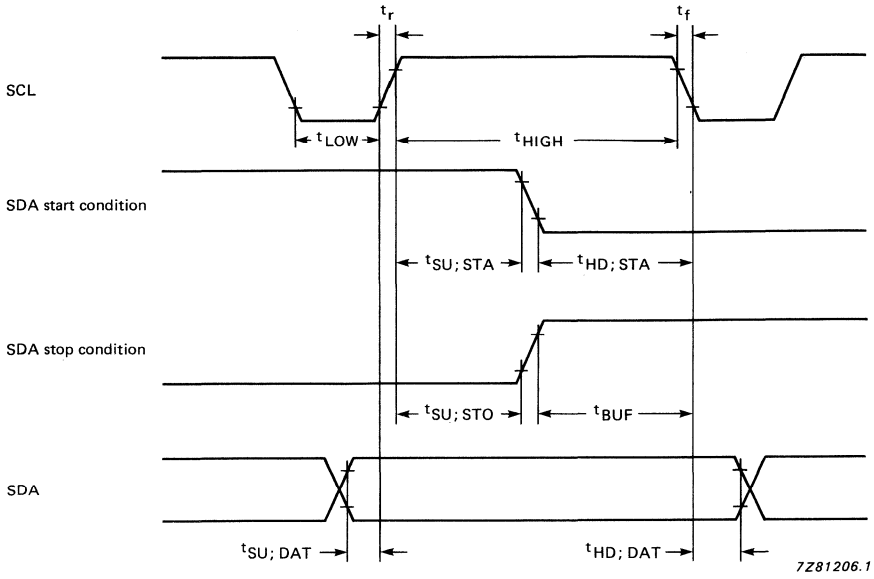


Fig. 6 Timing requirements for I²C bus.

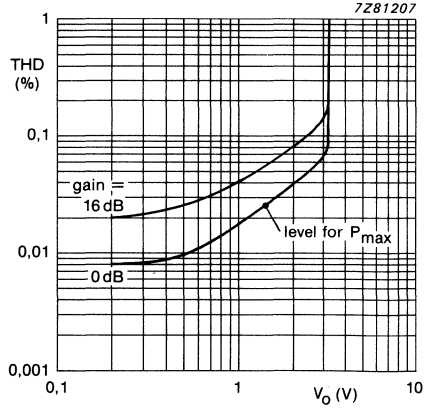


Fig. 7 Distortion loudspeaker channel CH1 as a function of the output voltage with gain as parameter.

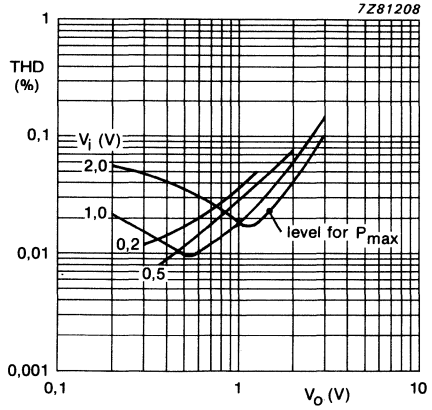


Fig. 8 Distortion loudspeaker channel CH1 as a function of the output voltage with input voltage as parameter.

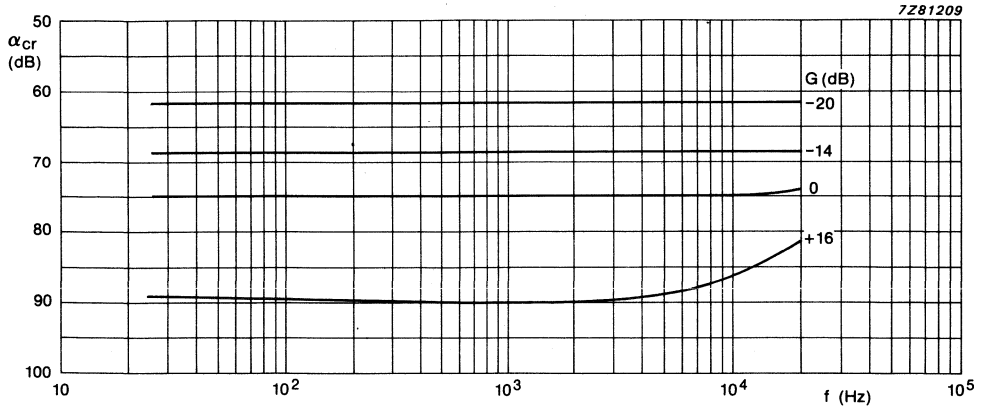


Fig. 9 Channel separation loudspeaker channel CH1 as a function of frequency.

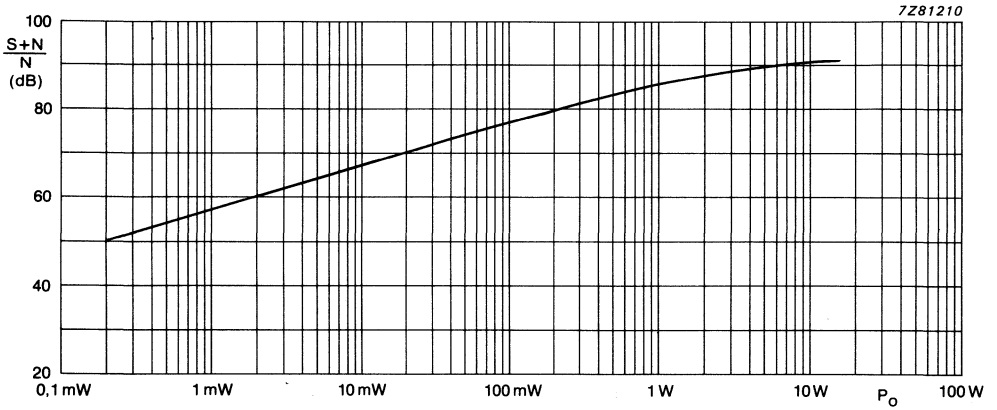


Fig. 10 Signal-to-noise ratio as a function of output power.
Input voltage V_i = 0,5 V; according to CCIR; quasi peak; P_o = 15 W.

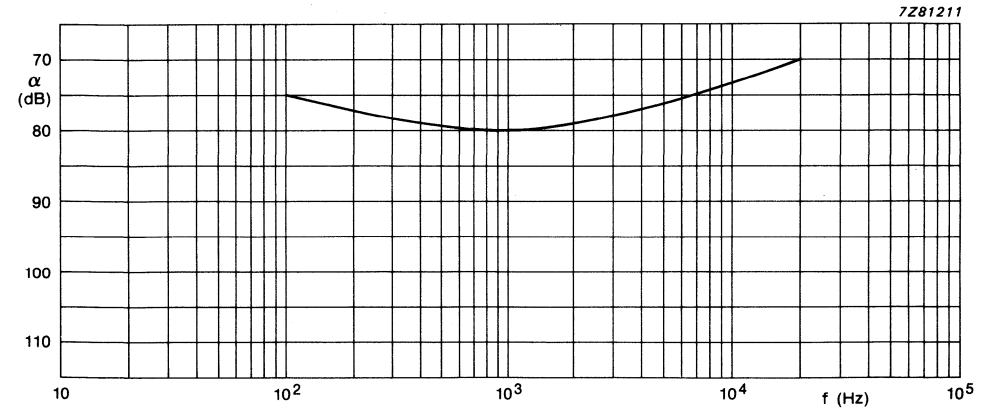


Fig. 11 Crosstalk 2-tone mode as a function of frequency.
CH1: mode AA, Gain + 16 dB; CH2: mode BB, Gain 0 dB. Signal input RIGHT; input LEFT to ground, measured at output CH1.

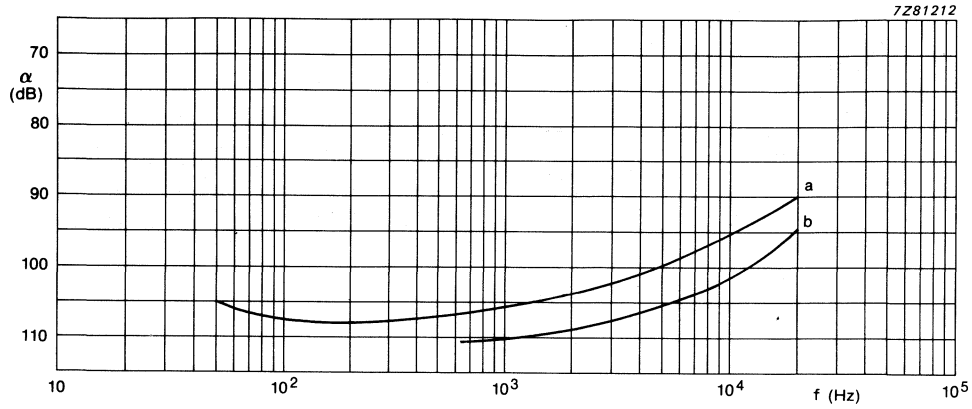


Fig. 12 Crosstalk between IN1 and IN2 as a function of frequency; measured at output CH1, R_G = 0.
a) Gain = + 16 dB; V_i = 200 mV. b) Gain = 0 dB; V_i = 1 V.

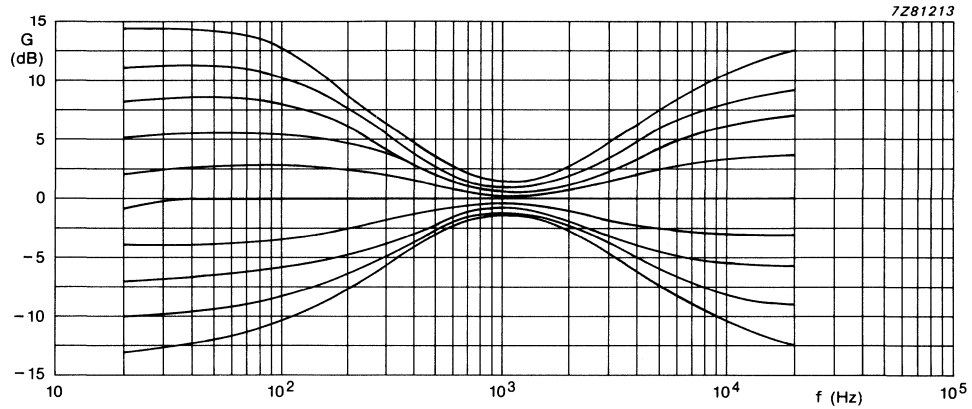


Fig. 13 Bass and treble tone control. C_{bass} = 33 nF, C_{treble} = 5,6 nF.

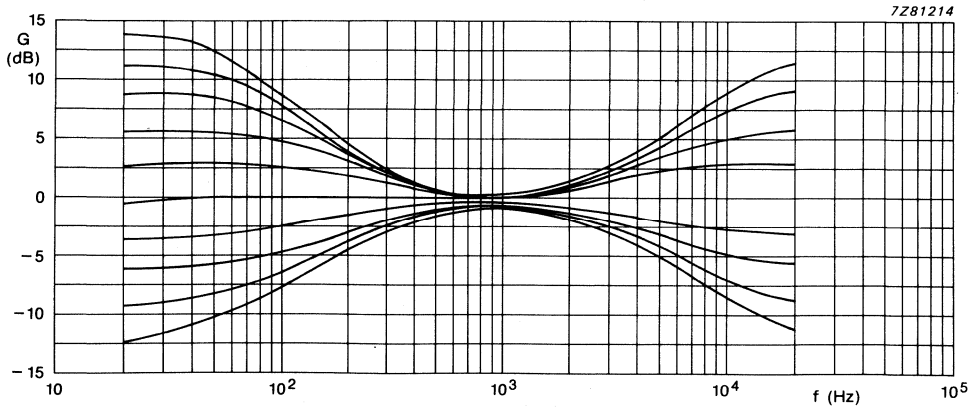
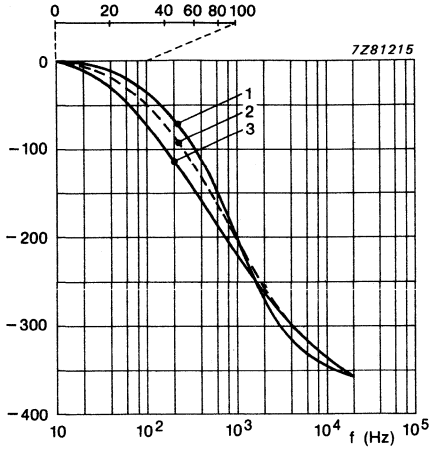


Fig. 14 Bass and treble tone control. C_{bass} = 68 nF, C_{treble} = 3,9 nF.



curve	C_{24} (nF)	C_{25} (nF)	effect
1	15	15	normal
2	5,6	47	intensified
3	5,6	68	more intensified

Fig. 15 Pseudo (phase) as a function of frequency CH1 left.

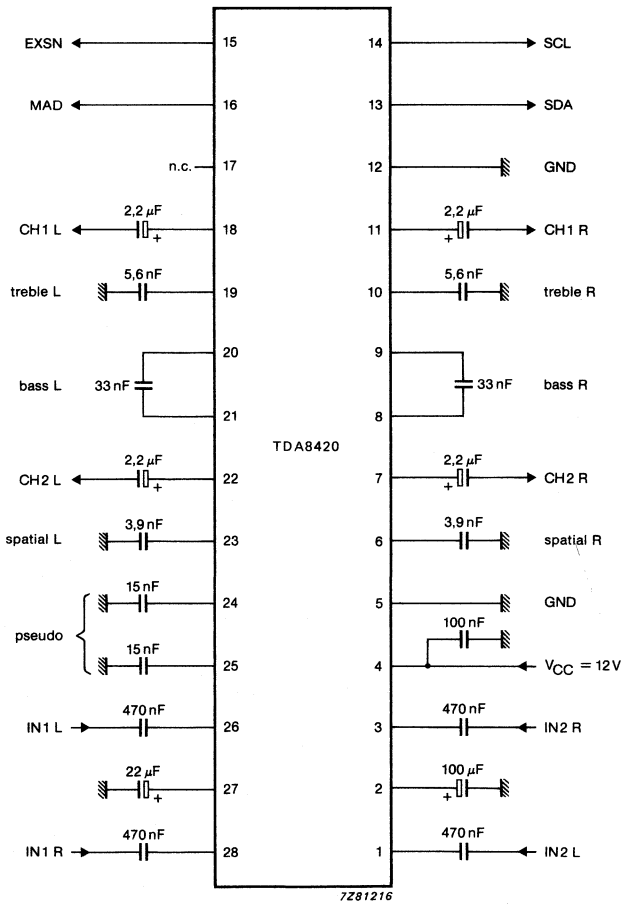
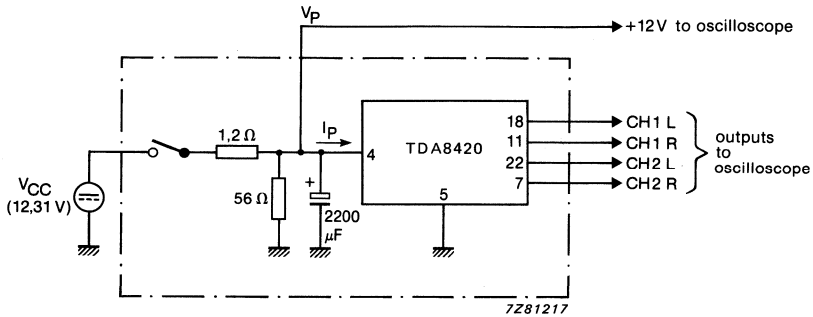


Fig. 16 Test and application circuit diagram.



I_{CC} = 45 mA;
I_{load} = 259 mA;
t_{on} = 2,64 ms;
t_{off} = 102 ms.

Fig. 17 Turn-on/off power supply circuit diagram.

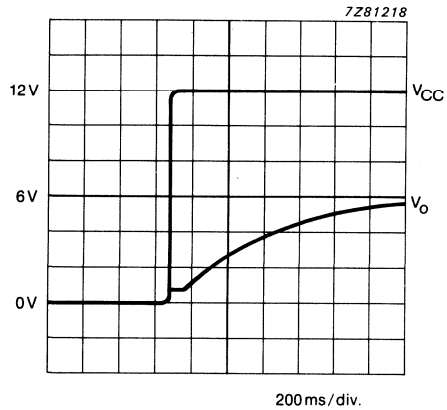


Fig. 18 Turn-on behaviour;
C = 2,2 μF; R_L = 10 kΩ.

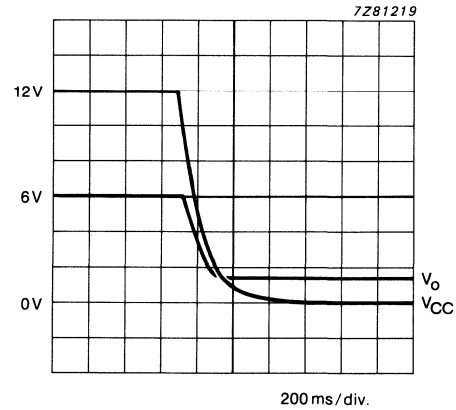


Fig. 19 Turn-off behaviour;
without modulation.

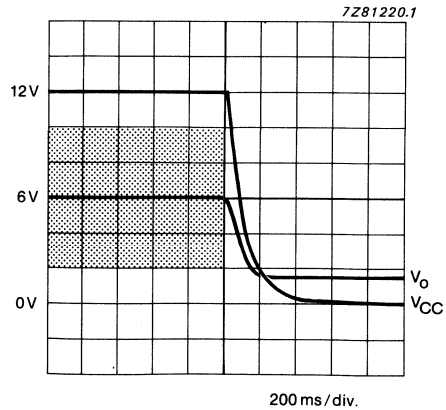


Fig. 20 Turn-off behaviour; with modulation (shaded area).

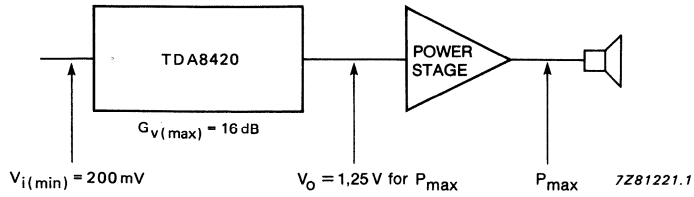


Fig. 21 Level diagram loudspeaker channel CH1 with $V_{i(min)}$ = 200 mV; V_o = 1,25 for P_{max}.

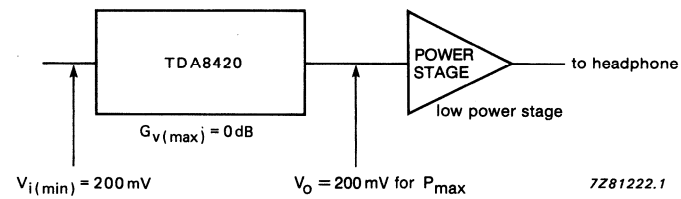


Fig. 22 Level diagram headphone channel CH2 with V_i = 200 mV; V_o = 200 mV for P_{max}.

HI-FI STEREO AUDIO PROCESSOR; I²C BUS

GENERAL DESCRIPTION

The TDA8421 is a monolithic bipolar integrated stereo sound circuit with a loudspeaker channel (CH1) and a headphone channel (CH2), digital controlled via the I²C bus, for application in hi-fi audio and television sound.

Features

- Input selector
- Mode selector
- Loudspeaker channel (CH1) } with volume control, balance control and mute
- Headphone channel (CH2) }
- Pseudo stereo and spatial function
- Bass and treble control
- Electrostatic discharge protection diodes

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_{CC}	7,5	12	14	V
Input signal handling	V_I	2	–	–	V
Input sensitivity full power at the output stage	V_i	–	200	–	mV
Signal plus noise-to-noise ratio	(S+N)/N	–	90	–	dB
Total harmonic distortion	THD	–	0,05	–	%
Channel separation	α	–	75	–	dB
Volume control range CH1	G	−62	–	16	dB
Treble control range	G	−12	–	12	dB
Bass control range	G	−12	–	15	dB
Volume control range CH2	G	−62	–	0	dB

PACKAGE OUTLINE

28-lead dual in-line; plastic (SOT117).

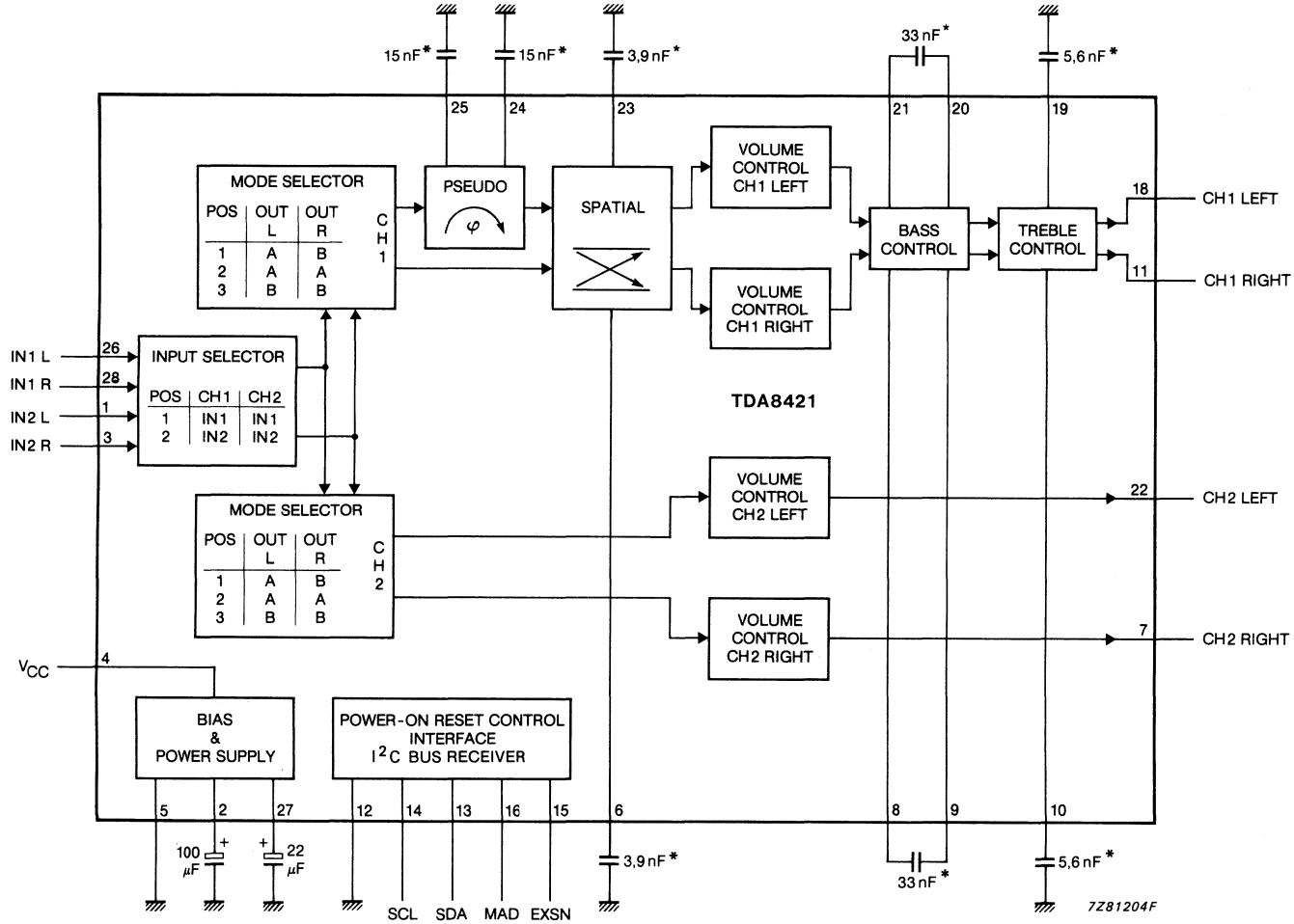


Fig. 1 Block diagram.

* These values are dependent on the required frequency response and effect.

PINNING

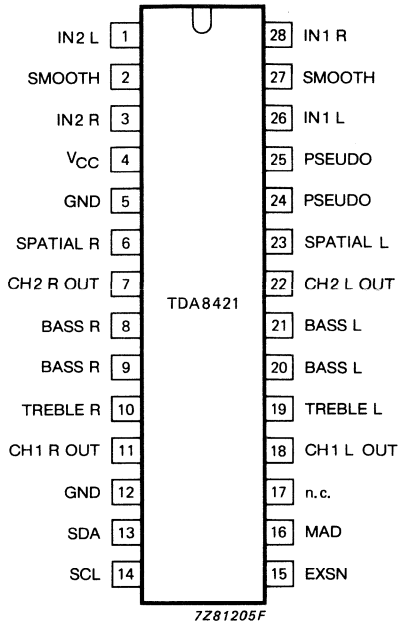


Fig. 2 Pinning diagram.

FUNCTIONAL DESCRIPTION

Input selector

The input to channel 1 (CH1) and channel 2 (CH2) is determined by the input selector. The selection is made from the following AF input signals:

- IN1 L (pin 26); IN1 R (pin 28)
  or
- IN2 L (pin 1); IN2 R (pin 3)

Where IN1 is an internal input signal and IN2 an external input signal.

Mode selector

For each channel (CH1 and CH2) there is a mode selector which selects between stereo, sound A and sound B in the event of bilingual transmission. Both mode selectors can be controlled independently.

Headphone channel (CH2)

Volume control and balance

The stages for volume control for CH2 consist of two parts for left and right. In each part the gain can be adjusted between 0 and −62 dB in steps of 2 dB. An additional step allows an attenuation of $\geqslant$ 90 dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right.

Loudspeaker channel (CH1)

Volume control and balance

The loudspeaker channel (CH1) also consists of two parts for volume control (left and right). In each part the gain can be adjusted between + 16 dB and −62 dB in steps of 2 dB. An additional step allows an attenuation of $\geqslant$ 90 dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right.

Stereo/pseudo stereo/spatial stereo mode

It is possible to select three modes. Stereo, pseudo or spatial stereo. The pseudo stereo mode receives mono transmissions and the stereo and spatial stereo mode receives stereo transmissions.

Bass control

The bass control stage can be switched from an emphasis of 15 dB to an attenuation of 12 dB for low frequencies in steps of 3 dB.

Treble control

The treble control stage can be switched from + 12 dB to −12 dB in steps of 3 dB.

Bias and power supply

The TDA8421 includes a bias and power supply stage, which generates a voltage of ½ V_{CC} with a low output impedance and injector currents for the logic part.

Power-on reset

The on-chip power-on reset circuit sets the mute bit to active, which mutes both the loudspeaker channel (CH1) and the headphone channel (CH2). The muting can be switched by transmission of the mute bit.

I^2C bus receiver and data handling

Bus specification

The TDA8421 is controlled via the 2-wire I^2C bus by a microcomputer. The two wires (SDA — serial data, SCL — serial clock) carry information between the devices connected to the bus. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull up resistor.
When the bus is free both lines are HIGH. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The set up and hold times are specified in AC CHARACTERISTICS.

A HIGH-to-LOW transition of the SDA line while SCL is HIGH is defined as a start condition.
A LOW-to-HIGH transition of the SDA line while SCL is HIGH is defined as a stop condition.
The bus receiver will be reset by the reception of a start condition. The bus is considered to be busy after the start condition. The bus is considered to be free again after a stop condition.

Module address

Data transmission to the TDA8421 starts with the module address MAD.

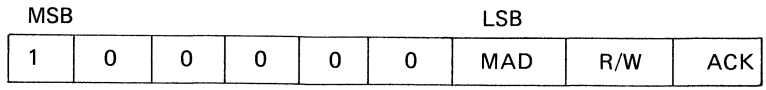


Fig. 3 TDA8421 module address.

The module address is determined by pin 16. When connected to ground MAD = 0; when connected to V_{CC} MAD = 1. Thus two TDA8421s can be selected within a system.

Subaddress

After the module address byte a second byte is used to select the functions for both channels:

- CH1 – Volume left, volume right, bass, treble and switch functions
- CH2 – Volume left, volume right and switch functions

The subaddress SAD is stored within the TDA8421. Table 1 defines the coding of the second byte after the module address MAD.

Table 1 Second byte after module address MAD

		128	64	32	16	8	4	2	1
	function	MSB 7	6	5	4	3	2	1	LSB 0
CH1	volume left	0	0	0	0	0	0	0	0
	volume right	0	0	0	0	0	0	0	1
	bass	0	0	0	0	0	0	1	0
	treble	0	0	0	0	0	0	1	1
	switch functions	0	0	0	0	1	0	0	0
CH2	volume left	0	0	0	0	0	1	0	0
	volume right	0	0	0	0	0	1	0	1
	switch functions	0	0	0	0	1	1	0	0
						subaddress SAD			

Definition of 3rd byte

A third byte is used to transmit data to the TDA8421. Table 2 defines the coding of the third byte after module address MAD and subaddress SAD.

Table 2 Third byte after module address MAD and subaddress SAD

	function		MSB 7	6	5	4	3	2	1	LSB 0
	volume left	VL1	1	1	V05	V04	V03	V02	V01	V00
	volume right	VR1	1	1	V15	V14	V13	V12	V11	V10
CH1	bass	BA	1	1	1	1	BA3	BA2	BA1	BA0
	treble	TR	1	1	1	1	TR3	TR2	TR1	TR0
	switch functions	S1	1	1	MU	EFL	STL	ML1	ML0	IS
	volume left	VL2	1	1	V25	V24	V23	V22	V21	V20
CH2	volume right	VR2	1	1	V35	V34	V33	V32	V31	V30
	switch functions	S2	1	1	1	1	EXS	MH1	MH0	1

Truth tables

Truth tables for the switch functions

Table 3 Input selector

function	IS
IN1	0
IN2	1

Table 4 Mode selectors

	CH1		CH2	
mode	ML0	ML1	MH0	MH1
stereo	1	1	1	1
sound A	1	0	1	0
sound B	0	1	0	1
----------	0	0	0	0

Table 5 Stereo/pseudo stereo/spatial stereo

choice	STL	EFL
spatial	1	1
stereo	1	0
pseudo	0	1
----------	0	0

Table 6 Mute

mute	MU
active; automatic after POR*	1
not active	0

Table 7 Output for external switch

EXSN	EXS
ground	1
open collector	0

Where: POR = Power-On Reset.

Truth tables for the volume base and treble controls.

Table 8 Volume control

CH1	CH2	V x 5	V x 4	V x 3	V x 2	V x 1	V x 0
16	0	1	1	1	1	1	1
14	−2	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
−46	−62	1	0	0	0	0	0
−48	⩽−90	0	1	1	1	1	1
.	.	.	.	.	.	.	.
−62	⩽−90	0	1	1	0	0	0
⩽−90	⩽−90	0	1	0	1	1	1
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
⩽−90	⩽−90	0	0	0	0	0	0

Where: The values of CH1 and CH2 are in 2 dB/step measured in dBs.

* Attenuation ⩾ 90 dB

Table 9 Bass control

3dB/step (dB)	BA3	BA2	BA1	BA0
15	1	1	1	1
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
15	1	0	1	1
12	1	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
0	0	1	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	0	0

Table 10 Treble control

3dB/step (dB)	TR3	TR2	TR1	TR0
12	1	1	1	1
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
12	1	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
0	0	1	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	0	0

Sequence of data transmission

After a power-on reset all eight functions have to be adjusted with eight data transmissions. It is recommended that data information for switch functions in CH1 are transmitted last because all functions have to be adjusted when the muting is switched off. The sequence of transmission of other data information is not critical.

The order of data transmission is shown in Figures 4 and 5. The number of data transmissions is unrestricted but before each data byte the module address MAD and the correct subaddress SAD is required.

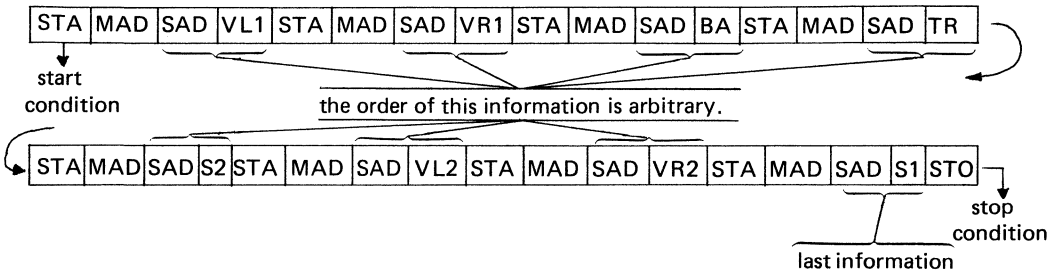


Fig. 4 Data transmission after a power-on reset.

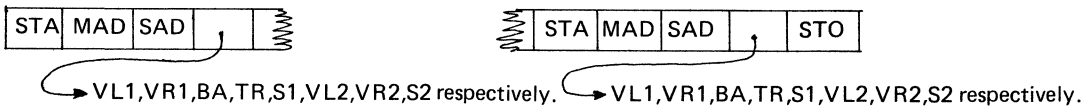


Fig. 5 Data transmission except after power-on reset.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{CC}	0	16	V
Voltage range at pins for external capacitors				
pins 2, 6, 8 to 10, 19 to 21, 23 to 25, 27	V_{cap}	0	V_{CC}	V
pin 13	V_{SDA}	0	V_{CC}	V
pin 14	V_{SCL}	0	V_{CC}	V
pin 15	V_{EXSN}	0	V_{CC}	V
pin 16	V_{MAD}	0	V_{CC}	V
Voltage range at pins 1, 3, 7, 11, 18, 22, 26, 28	V_I, V_O	0	V_{CC}	V
Output current at pins 7, 11, 18, 22	I_O	–	45	mA
Total power dissipation at $T_{amb} < 70\ ^oC$	P_{tot}	–	1350	mW
Operating ambient temperature range	T_{amb}	0	70	^oC
Storage temperature range	T_{stg}	–25	150	^oC
Electrostatic handling *	$\pm V_{ESD}$	–	2000	V

* Equivalent to discharging a 100 pF capacitor through a 1,5 kΩ resistor.

DC CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_{CC}	7,5	12	14	V
Supply current at V_{CC} = 12 V	I_{CC}	–	42	55	mA
Internal input voltage IN1 L,R (pins 26,28) IN2 L,R (pins 1,3) DC voltage internally generated; capacitive coupling recommended	V_I	5,4	6,0	6,6	V
MAD (pin 16)					
input voltage HIGH	V_{IH}	3,0	–	V_{CC}	V
input voltage LOW	V_{IL}	0	–	1,5	V
input current HIGH	I_{IH}	–	–	1,0	μA
input current LOW	I_{IL}	–	1	10	μA
SDA; SCL (pins 13 and 14)					
input voltage HIGH	V_{IH}	3,0	–	V_{CC}	V
input voltage LOW	V_{IL}	−0,3	–	1,5	V
input current HIGH	I_{IH}	–	–	1,0	μA
input current LOW	I_{IL}	–	1	10	μA
Output voltage at CH1 (pins 11 and 18); CH2 (pins 7 and 22)	V_O	5,4	½ V_{CC}	6,6	V
pins with external capacitors					
pins 6 to 10; 19 to 21; 23 to 25	$V_{cap.n}$	–	½ V_{CC}	–	V
pin 2	$V_{cap.2}$	–	V_{CC}−0,1	–	V
External switch (pin 15) at I_{EXSN} = 1 mA					
Output voltage HIGH	V_{EXSNH}	–	–	16	V
Output voltage LOW	V_{EXSNL}	–	–	0,3	V

AC CHARACTERISTICS

V_{CC} = 12 V; bass/treble in linear position; pseudo and spatial stereo off; $R_L > 10\ k\Omega$; $C_L < 100\ pF$; T_{amb} = 25 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
I²C bus timing (see Fig. 6)					
SDA, SCL (pin 13 and 14)					
Clock frequency range	f_{SCL}	0	–	100	kHz
The HIGH period of the clock	t_{HIGH}	4	–	–	μs
The LOW period of the clock	t_{LOW}	4,7	–	–	μs
SCL rise time	t_r	–	–	1	μs
SCL fall time	t_f	–	–	0,3	μs
Set-up time for start condition	$t_{SU;STA}$	4,7	–	–	μs
Hold time for start condition	$t_{HD;STA}$	4	–	–	μs
Set-up time for stop condition	$t_{SU;STO}$	4,7	–	–	μs
Time bus must be free before a new transmission can start	t_{BUF}	4,7	–	–	μs
Set-up time DATA	$t_{SU;DAT}$	250	–	–	ns
Input signals					
IN1 L (pin 26) IN1 R (pin 28) IN2 L (pin 1) IN2 R (pin 3)					
Input signal handling (r.m.s. value) at V_u = –4 dB; THD ≤ 0,5%	$V_{i(rms)}$	2	–	–	V
Input resistance	R_{n-5}	35	50	–	kΩ
Frequency response (–0,5 dB) bass and treble in linear position; stereo mode; effects off	f	20	–	20 000	Hz

AC CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
LOUDSPEAKER CHANNEL OUTPUTS					
CH1 LEFT (pin 18); CH1 RIGHT (pin 11)					
Output voltage range (r.m.s. value) at THD ⩽ 0,5%	$V_{o(rms)}$	2	–	–	V
Load resistance	R_L	10	–	–	kΩ
Output impedance	Z_O	–	–	100	Ω
Noise level weighted according to CCIR468-2					
gain = 16 dB	V_n	–	90	–	μV
gain = 0 dB	V_n	–	20	40	μV
gain = ⩽ –90 dB	V_n	–	15	–	μV
Total harmonic distortion (f = 20 Hz to 12,5 kHz)					
for $V_{i(rms)}$ = 0,5 V; gain = + 16 dB to –30 dB	THD	–	0,05	0,2	%
for $V_{i(rms)}$ = 1,0 V; gain = + 2 dB to –30 dB	THD	–	0,07	0,2	%
for $V_{i(rms)}$ = 2,0 V; gain = –4 dB to –30 dB	THD	–	0,1	–	%
Channel separation at 10 kHz gain = 0 dB	α_{cr}	–	75	–	dB
Ripple rejection (gain = 0 dB; bass and treble in linear position) f_{ripple} = 100 Hz	RR_{100}	–	50	–	dB
Crosstalk attenuation from logic inputs to AF outputs (gain = 0 dB; bass and treble in linear position)	α_L	–	110	–	dB
VOLUME CONTROL					
For truth table see Table 8					

parameter	symbol	min.	typ.	max.	unit
Loudspeaker channel (CH1)					
Control range at f = 1 kHz					
maximum voltage gain (16 dB step)	G_{max}	15	–	–	dB
minimum voltage gain (–62 dB step)	G_{min}	–60	–	–	dB
last position	G_{off}	–80	–85	–	dB
mute position	G_{mute}	–85	–90	–	dB
Resolution	G_{step}	–	2	–	dB/step
Gain difference between left and right AF channel (note 1)					
gain from 16 dB to –30 dB	ΔG	–	–	0,5	dB
gain from –30 dB to –62 dB	ΔG	–	–	1	dB
TREBLE CONTROL (CH1)					
For truth table see Table 10					
Control range for $C_{10\text{-}5}$; $C_{19\text{-}5}$ = 5,6 nF					
Maximum emphasis at 15 kHz with respect to linear position	G	11	12	13	dB
Maximum attenuation at 15 kHz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	–	3	–	dB/step
BASS CONTROL					
For truth table see Table 9					
Control range for $C_{8\text{-}9}$; $C_{20\text{-}21}$ = 33 nF					
Maximum emphasis at 40 kHz with respect to linear position	G	14	15	16	dB
Maximum attenuation at 40 kHz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	–	3	–	dB/step
SPATIAL AND PSEUDO FUNCTION					
Spatial: Antiphase crosstalk	α	–	50	–	%
Pseudo: Phase shift (see Fig. 15)					

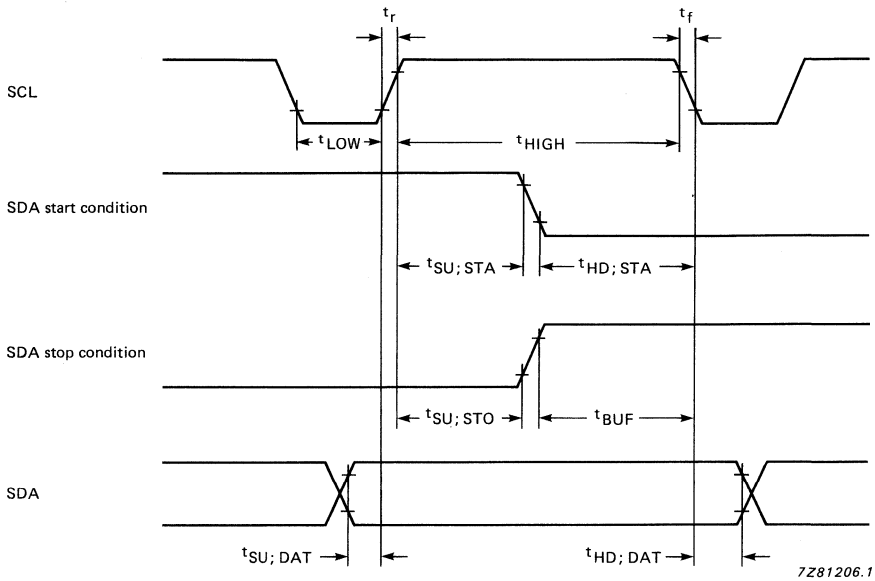
AC CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
HEADPHONE CHANNEL OUTPUTS					
CH2 LEFT (pin 22); CH2 RIGHT (pin 7)					
Output voltage range (r.m.s. value) at THD ⩽ 0,5%	$V_{o(rms)}$	2	–	–	V
Load resistance	R_L	10	–	–	kΩ
Output impedance	Z_O	–	–	100	Ω
Noise level (weighted according to CCIR468-2)					
gain = 0 dB	V_n	–	15	–	μV
gain = 16 dB	V_n	–	12	25	μV
gain = ⩽ –90 dB	V_n	–	10	–	μV
Total harmonic distortion (f = 20 Hz to 12,5 kHz)					
for $V_{i(rms)}$ = 0,2 V; gain = 0 dB to –30 dB	THD	–	0,01	0,2	%
for $V_{i(rms)}$ = 1,0 V; gain = 0 dB to –30 dB	THD	–	0,1	–	%
for $V_{i(rms)}$ = 2,0 V gain = –4 dB to –30 dB	THD	–	0,3	–	%
Channel separation at 10 kHz gain = 0 dB	α_{cr}	–	75	–	dB
Ripple rejection (gain = 0 dB; bass and treble in linear position) f_{ripple} = 100 Hz	RR_{100}	–	50	–	dB
Crosstalk attenuation from logic inputs to AF outputs (gain = 0 dB; bass and treble in linear position)	α_L	–	110	–	dB
Crosstalk between any input/output f = 100 Hz to 12,5 kHz	α	65	70	–	dB
Crosstalk IN1/IN2 gain = 0 dB; R_G = 0	α	95	100	–	dB

parameter	symbol	min.	typ.	max.	unit
Headphone channel (CH2)					
Control range					
maximum voltage gain (0 dB step)	G_{max}	−1	–	–	dB
minimum voltage gain (−62 dB step)	G_{min}	−57	–	–	dB
last position	G_{off}	−80	−85	–	dB
mute position	G_{mute}	−85	−90	–	dB
Resolution	G_{step}	–	2	–	dB/step
Gain difference between left and right AF channel (note 1)					
gain from 0 dB to −40 dB	ΔG	–	–	0,5	dB
gain from −40 dB to −62 dB	ΔG	–	–	2	dB

Note to the AC characteristics

1. Balance is realized via software by different volume settings in both channels.



$t_{SU;STA}$ = start code set-up time
$t_{HD;STA}$ = start code hold time
$t_{SU;STO}$ = stop code set-up time

t_{BUF} = BUS free time
$t_{SU;DAT}$ = data set-up time
$t_{HD;DAT}$ = DATA hold time

Fig. 6 Timing requirements for I²C bus.

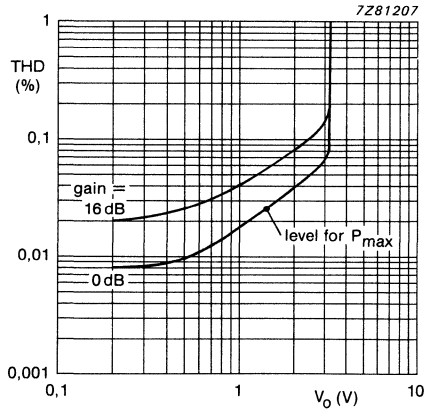


Fig. 7 Distortion loudspeaker channel CH1 as a function of the output voltage with gain as parameter.

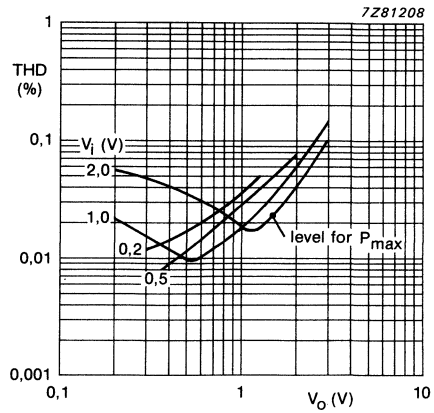


Fig. 8 Distortion loudspeaker channel CH1 as a function of the output voltage with input voltage as parameter.

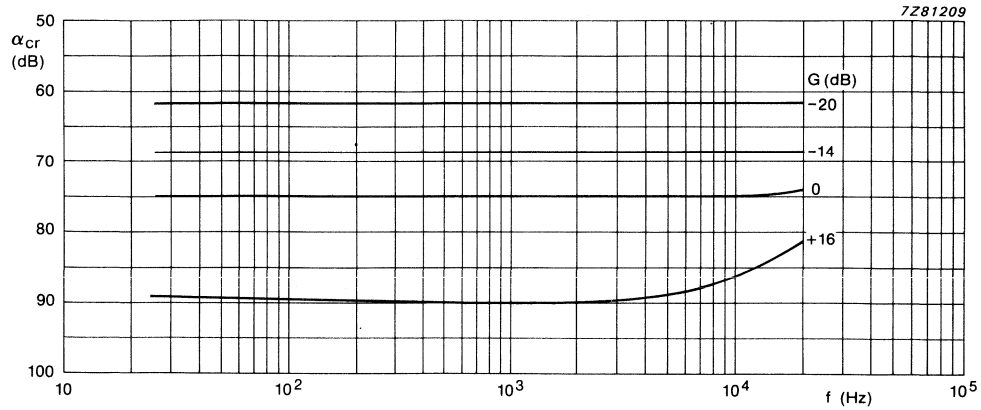


Fig. 9 Channel separation loudspeaker channel CH1 as a function of frequency.

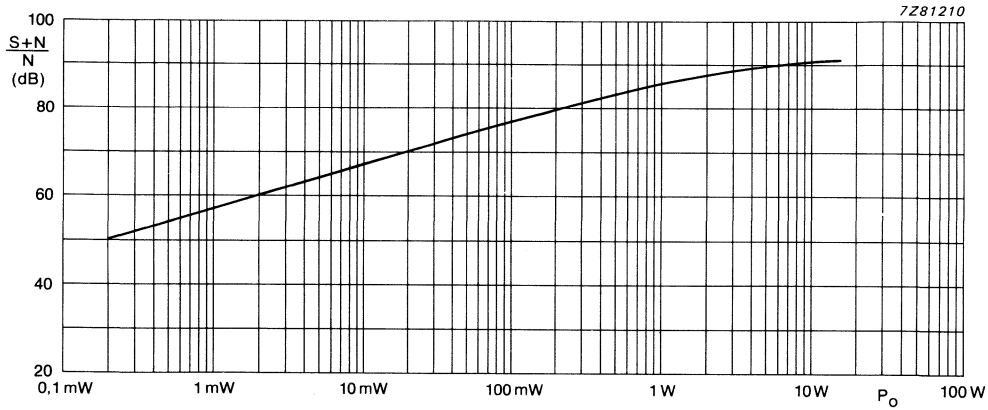


Fig. 10 Signal-to-noise ratio as a function of output power.
Input voltage V_i = 0,5 V; according to CCIR; quasi peak; P_o = 15 W.

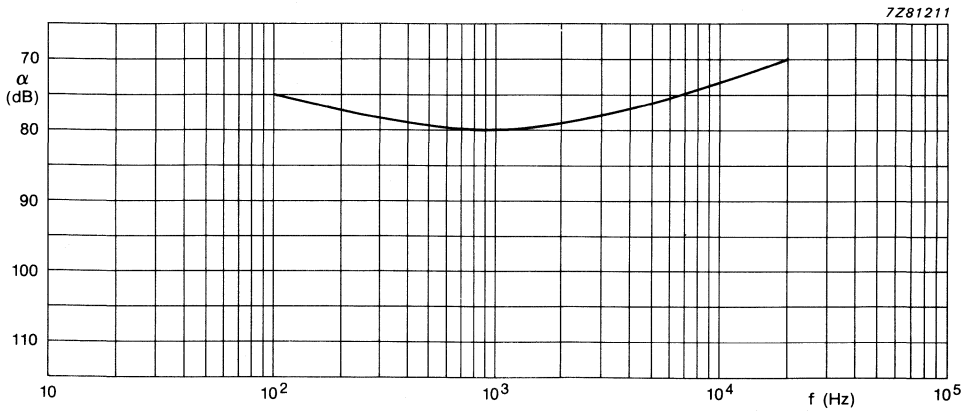


Fig. 11 Crosstalk 2-tone mode as a function of frequency.
CH1: mode AA, Gain + 16 dB; CH2: mode BB, Gain 0 dB. Signal input RIGHT; input LEFT to ground, measured at output CH1.

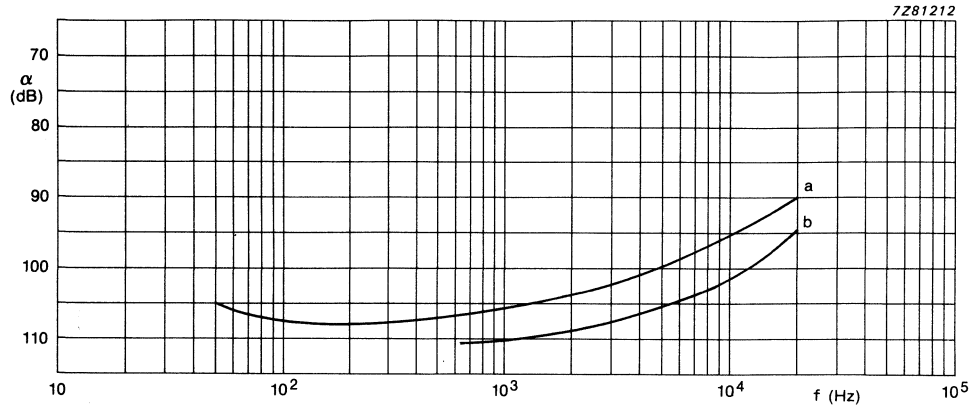


Fig. 12 Crosstalk between IN1 and IN2 as a function of frequency; measured at output CH1, $R_G = 0$.
a) Gain = + 16 dB; V_i = 200 mV. b) Gain = 0 dB; V_i = 1 V.

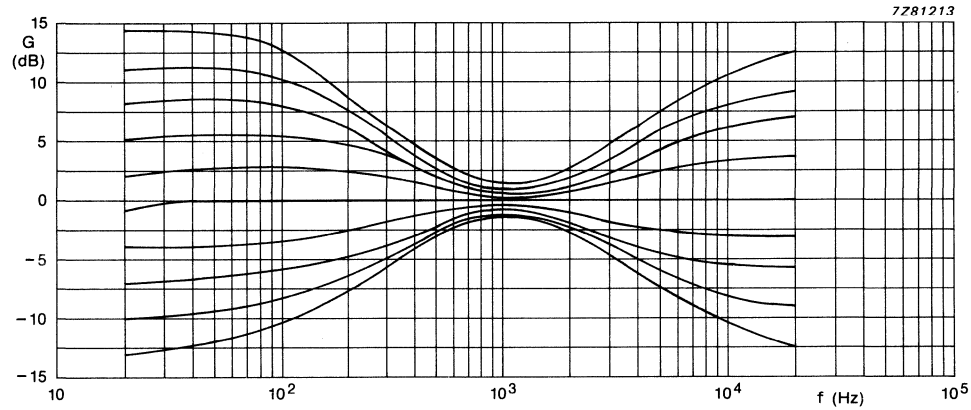


Fig. 13 Bass and treble tone control. C_{bass} = 33 nF, C_{treble} = 5,6 nF.

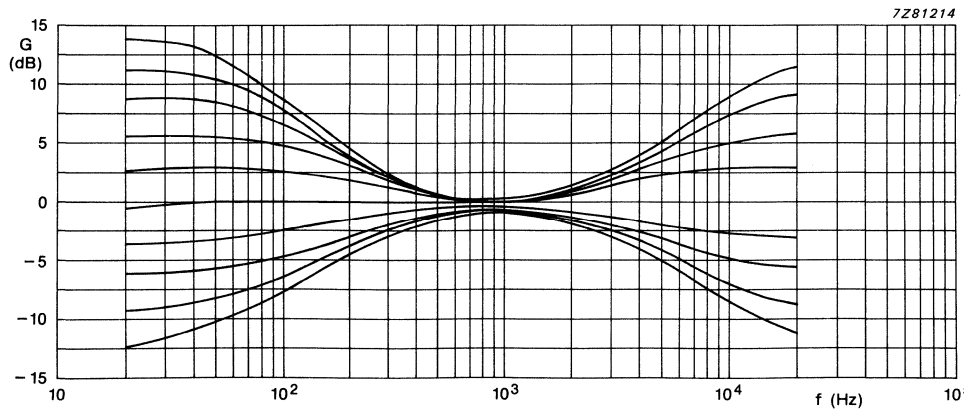
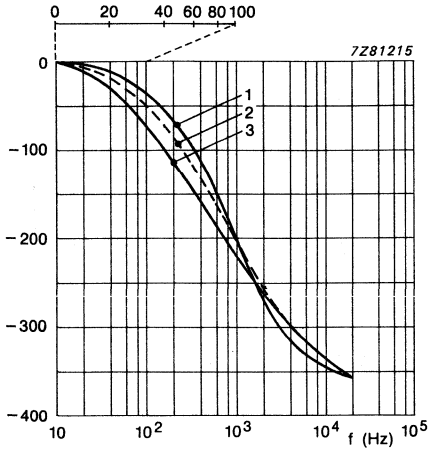


Fig. 14 Bass and treble tone control. C_{bass} = 68 nF, C_{treble} = 3,9 nF.



curve	pin 24 (nF)	pin (nF)	effect
1	15	15	normal
2	5,6	47	intensified
3	5,6	68	more intensified

Fig. 15 Pseudo (phase) as a function of frequency CH1 left.

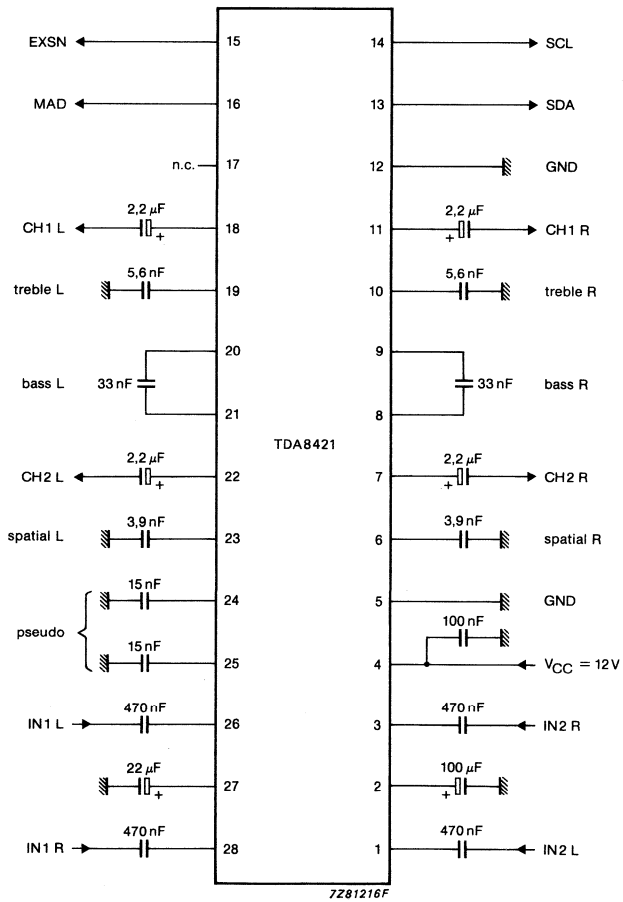
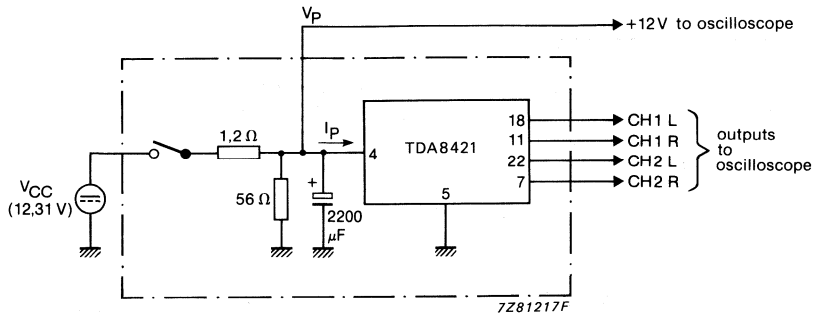


Fig. 16 Test and application circuit diagram.



I_{CC} = 45 mA;
I_{load} = 259 mA;
t_{on} = 2,64 ms;
t_{off} = 102 ms.

Fig. 17 Turn-on/off power supply circuit diagram.

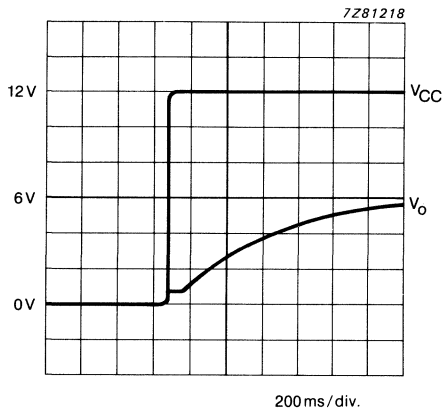


Fig. 18 Turn-on behaviour;
C = 2,2 μF; R_L = 10 kΩ.

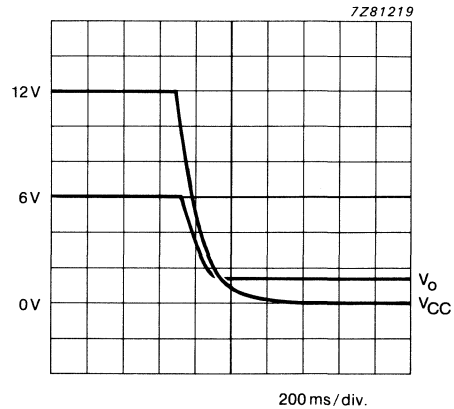


Fig. 19 Turn-off behaviour;
without modulation.

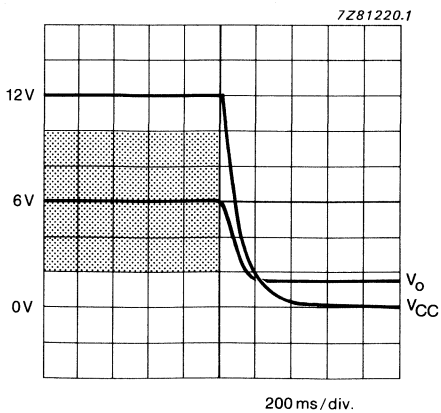


Fig. 20 Turn-off behaviour; with modulation (shaded area).

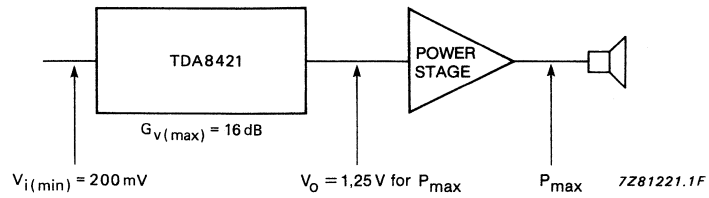


Fig. 21 Level diagram loudspeaker channel CH1 with $V_{i(min)}$ = 200 mV; V_o = 1,25 for P_{max}.

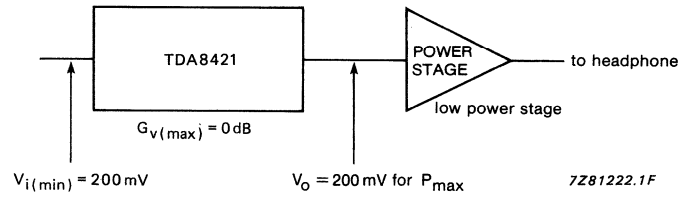


Fig. 22 Level diagram headphone channel CH2 with V_i = 200 mV; V_o = 200 mV for P_{max}.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

HI-FI STEREO AUDIO PROCESSOR; I²C-BUS

GENERAL DESCRIPTION

The TDA8425 is a monolithic bipolar integrated stereo sound circuit with a loudspeaker channel facility, digitally controlled via the I²C bus for application in hi-fi audio and television sound.

Features

- Source and mode selector for two stereo channels
- Pseudo stereo, spatial stereo, linear stereo and forced mono switch
- Volume and balance control
- Bass, treble and mute control
- Power supply with power-on reset

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_{CC}	10.8	12.0	13.2	V
Input signal handling	V_I	2	–	–	V
Input sensitivity full power at the output stage	V_i	–	300	–	mV
Signal plus noise-to-noise ratio	(S+N)/N	–	86	–	dB
Total harmonic distortion	THD	–	0.05	–	%
Channel separation	α	–	80	–	dB
Volume control range	G	–64	–	6	dB
Treble control range	G	–12	–	12	dB
Bass control range	G	–12	–	15	dB

PACKAGE OUTLINE

20-lead dual in-line; plastic (SOT146).

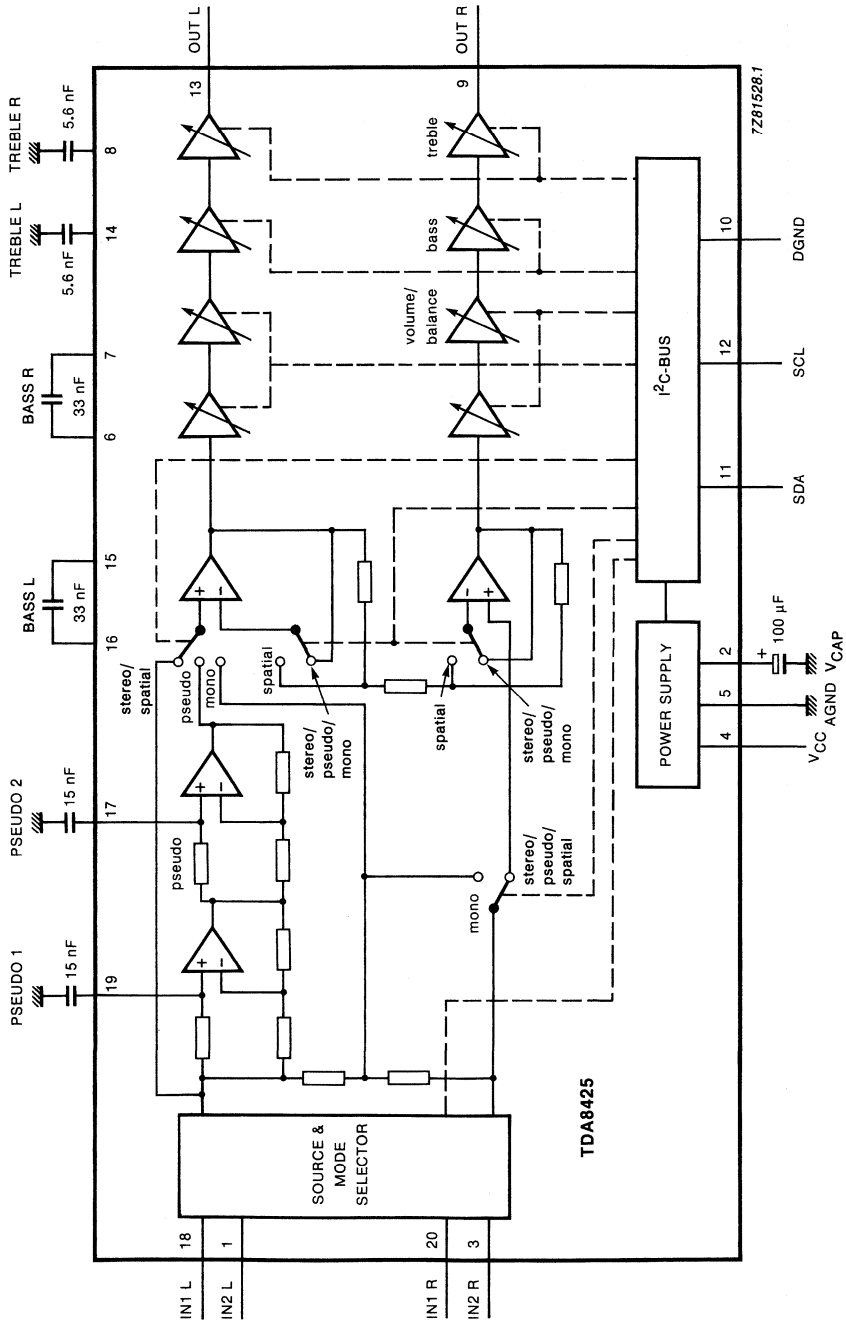


Fig. 1 Block diagram.

PINNING

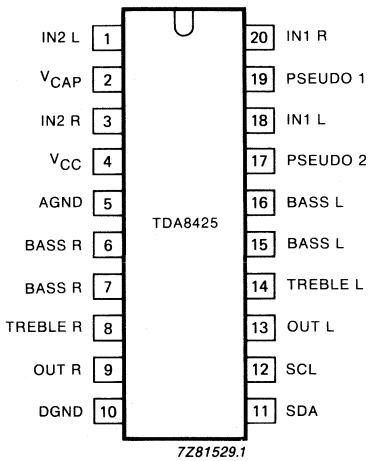


Fig. 2 Pinning diagram.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Source selector

The input to channel 1 (CH1) and channel 2 (CH2) is determined by the source selector. The selection is made from the following AF input signals:

- IN1 L (pin 18); IN1 R (pin 20)
  or
- IN2 L (pin 1); IN2 R (pin 3)

Mode selector

The mode selector selects between stereo, sound A and sound B (in the event of bilingual transmission) for OUT R and OUT L.

Volume control and balance

The volume control consists of two stages (left and right). In each part the gain can be adjusted between +6 dB and −64 dB in steps of 2 dB. An additional step allows an attenuation of $\geqslant$ 80 dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right output channels.

Linear stereo, pseudo stereo, spatial stereo and forced mono mode*

It is possible to select four modes: linear stereo, pseudo stereo, spatial stereo or forced mono. The pseudo stereo mode handles mono transmissions, the spatial stereo mode handles stereo transmissions and the forced mono can be used in the event of stereo signals.

Bass control

The bass control stage can be switched from an emphasis of 15 dB to an attenuation of 12 dB for low frequencies in steps of 3 dB.

* During forced mono mode the pseudo stereo mode cannot be used.

Treble control

The treble control stage can be switched from + 12 dB to −12 dB in steps of 3 dB.

Bias and power supply

The TDA8425 includes a bias and power supply stage, which generates a voltage of $0.5 \times V_{CC}$ with a low output impedance and injector currents for the logic part.

Power-on reset

The on-chip power-on reset circuit sets the mute bit to active, which mutes both parts of the treble amplifier. The muting can be switched by transmission of the mute bit.

I^2C-bus receiver and data handling

Bus specification

The TDA8425 is controlled via the 2-wire I^2C-bus by a microcomputer.
The two wires (SDA — serial data, SCL — serial clock) carry information between the devices connected to the bus. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull up resistor.
When the bus is free both lines are HIGH.
The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The set up and hold times are specified in AC CHARACTERISTICS.

A HIGH-to-LOW transition of the SDA line while SCL is HIGH is defined as a start condition.
A LOW-to-HIGH transition of the SDA line while SCL is HIGH is defined as a stop condition.
The bus receiver will be reset by the reception of a start condition. The bus is considered to be busy after the start condition.
The bus is considered to be free again after a stop condition.

Module address

Data transmission to the TDA8425 starts with the module address MAD.

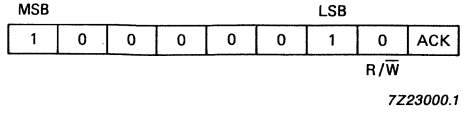


Fig. 3 TDA8425 module address.

Subaddress

After the module address byte a second byte is used to select the following functions:

- Volume left, volume right, bass, treble and switch functions

The subaddress SAD is stored within the TDA8425. Table 1 defines the coding of the second byte after the module address MAD.

Table 1 Second byte after module address MAD

	128	64	32	16	8	4	2	1
	MSB							LSB
function	7	6	5	4	3	2	1	0
volume left	0	0	0	0	0	0	0	0
volume right	0	0	0	0	0	0	0	1
bass	0	0	0	0	0	0	1	0
treble	0	0	0	0	0	0	1	1
switch functions	0	0	0	0	1	0	0	0
					subaddress SAD			

The automatic increment feature of the slave address enables a quick slave receiver initialization, within one transmission, by the I²C-bus controller (see Fig. 5).

Definition of 3rd byte

A third byte is used to transmit data to the TDA8425. Table 2 defines the coding of the third byte after module address MAD and subaddress SAD.

Table 2 Third byte after module address MAD and subaddress SAD

function		MSB 7	6	5	4	3	2	1	LSB 0
volume left	VL	1	1	V05	V04	V03	V02	V01	V00
volume right	VR	1	1	V15	V14	V13	V12	V11	V10
bass	BA	1	1	1	1	BA3	BA2	BA1	BA0
treble	TR	1	1	1	1	TR3	TR2	TR1	TR0
switch functions	S1	1	1	MU	EFL	STL	ML1	ML0	IS

DEVELOPMENT DATA

Truth tables

Truth tables for the switch functions

Table 3 Source selector

function	ML1	ML0	IS	channel
stereo	1	1	0	1
stereo	1	1	1	2
sound A	0	1	0	1
sound B	1	0	0	1
sound A	0	1	1	2
sound B	1	0	1	2

Table 4 Pseudo stereo/spatial stereo/linear stereo/forced mono

choice	STL	EFL
spatial stereo	1	1
linear stereo	1	0
pseudo stereo	0	1
forced mono*	0	0

Table 5 Mute

mute	MU
active; automatic after POR	1
not active	0

Where: POR = Power-ON Reset.

Truth tables for the volume, bass and treble controls

Table 6 Volume control

2 dB/step (dB)	V x 5	V x 4	V x 3	V x 2	V x 1	V x 0
6	1	1	1	1	1	1
4	1	1	1	1	1	0
−62	0	1	1	1	0	1
−64	0	1	1	1	0	0
⩽ −80	0	1	1	0	1	1
⩽ −80	0	0	0	0	0	0

* Pseudo stereo function is not possible in this mode.

DEVELOPMENT DATA

Table 7 Bass control

3 dB/step (dB)	BA3	BA2	BA2	BA0
15	1	1	1	1
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
15	1	0	1	1
12	1	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
0	0	1	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
−12	0	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
−12	0	0	0	0

Table 8 Treble control

3 dB/step (dB)	TR3	TR2	TR2	TR0
12	1	1	1	1
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
12	1	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
0	0	1	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
−12	0	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
−12	0	0	0	0

Sequence of data transmission

After a power-on reset all five functions have to be adjusted with five data transmissions. It is recommended that data information for switch functions are transmitted last because all functions have to be adjusted when the muting is switched off. The sequence of transmission of other data information is not critical.

The order of data transmission is shown in Figures 4 and 6. The number of data transmissions is unrestricted but before each data byte the module address MAD and the correct subaddress SAD is required.

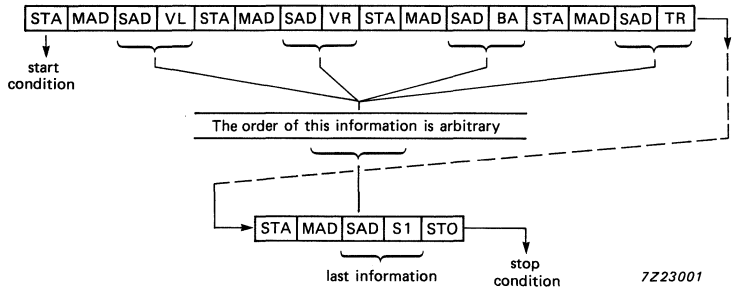


Fig. 4 Data transmission after a power-on reset.

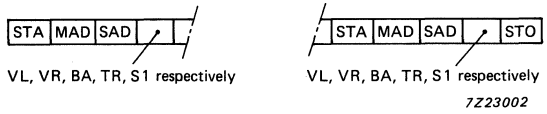


Fig. 5 Data transmission after a power-on reset with auto increment.

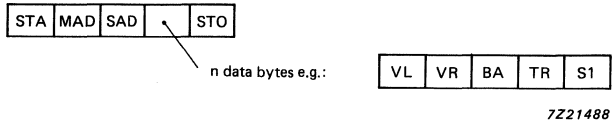


Fig. 6 Data transmission except after power-on reset.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{CC}	0	16	V
Voltage range for pins with external capacitors	V_{cap}	0	V_{CC}	V
Voltage range for pins 11 and 12	$V_{SDA, SCL}$	0	V_{CC}	V
Voltage range at pins 1, 3, 9, 11, 12, 13, 18 and 20	$V_{I/O}$	0	V_{CC}	V
Output current at pins 9 and 13	I_O	–	45	mA
Total power dissipation at $T_{amb} < 70$ °C	P_{tot}	–	450	mW
Operating ambient temperature range	T_{amb}	0	70	°C
Storage temperature range	T_{stg}	–25	+ 150	°C
Electrostatic handling, classification A*				

DEVELOPMENT DATA

* Human body model: C = 100 pF, R = 1.5 kΩ and V ⩾ 4 kV; charge device model: C = 200 pF, R = 0 Ω and V ⩾ 500 V.

DC CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	10.8	12.0	13.2	V
Supply current					
at V_{CC} = 12 V	I_{CC}	–	26	35	mA
Internal reference voltage	V_{ref}	5.4	0.5 x V_{CC}	6.6	V
Internal voltage at pins 1, 3, 18 and 20 DC voltage internally generated; capacitive coupling recommended	V_I	–	V_{REF}	–	V
Internal voltage at pins 9 and 13	V_O	–	V_{REF}	–	V
SDA; SCL (pins 11 and 12)					
input voltage HIGH	V_{IH}	3.0	–	V_{CC}	V
input voltage LOW	V_{IL}	−0.3	–	1.5	V
input current HIGH	I_{IH}	–	–	+ 10	μA
input current LOW	I_{IL}	−10	–	–	μA
Output voltage at pins with external capacitors					
pins 6 to 8, 14 to 17, 19	$V_{cap.n}$	–	V_{REF}	–	V
pin 2	$V_{cap.2}$	–	V_{CC}−0.3	–	V

DEVELOPMENT DATA

AC CHARACTERISTICS

V_{CC} = 12 V; bass/treble in linear position; pseudo and spatial stereo off; $R_L > 10\ k\Omega$; $C_L < 1000\ pF$; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
I²C bus timing (see Fig. 7)					
SDA, SCL (pin 11 and 12)					
Clock frequency range	f_{SCL}	0	–	100	kHz
The HIGH period of the clock	t_{HIGH}	4	–	–	μs
The LOW period of the clock	t_{LOW}	4.7	–	–	μs
SCL rise time	t_r	–	–	1	μs
SCL fall time	t_f	–	–	0.3	μs
Set-up time for start condition	$t_{SU;STA}$	4.7	–	–	μs
Hold time for start condition	$t_{HD;STA}$	4	–	–	μs
Set-up time for stop condition	$t_{SU;STO}$	4.7	–	–	μs
Time bus must be free before a new transmission can start	t_{BUF}	4.7	–	–	μs
Set-up time DATA	$t_{SU;DAT}$	250	–	–	ns
INPUTS					
IN1 L (pin 18) IN1 R (pin 20); IN2 L (pin 1) IN2 R (pin 3)					
Input signal handling (RMS value) at V_u = −12 dB; THD ⩽ 0.5%	$V_{i(rms)}$	2	–	–	V
Input resistance	R_i	20	30	40	kΩ
Frequency response (−0,5 dB) bass and treble in linear position; stereo mode; effects off	f	20	–	20 000	Hz
OUTPUTS					
OUT R (pin 9); OUT L (pin 13)					
Output voltage range (rms value) at THD ⩽ 0.7%; $V_{i(max)}$ ⩽ 2 V	$V_{o(rms)}$	0.6	–	–	V
Load resistance	R_L	10	–	–	kΩ
Output impedance	Z_O	–	–	100	Ω
Signal plus noise-to-noise ratio (weighted according to CCIR 468-2); V_o = 600 mV					
gain = 6 dB	(S+N)/N	–	78	–	dB
gain = 0 dB	(S+N)/N	–	86	–	dB
gain = ⩽ −20 dB	(S+N)/N	–	68	–	dB

AC CHARACTERISTICS (continued)

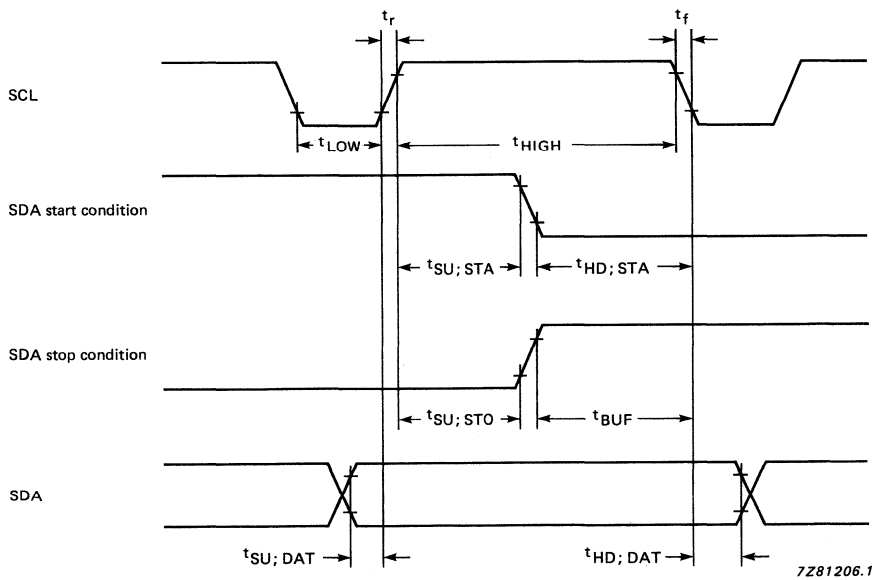
parameter	symbol	min.	typ.	max.	unit
OUTPUTS (continued)					
Crosstalk between inputs at gain = 0 dB; 1 kHz; opposite inputs grounded (50 Ω); IN1L (pin 18) to IN2L (pin 1) or IN1R (pin 20) to IN2R (pin 3)	α_{cr}	–	100	–	dB
Total harmonic distortion (f = 20 Hz to 12.5 kHz)					
for $V_{i(rms)}$ = 0.3 V; gain = + 6 dB to –40 dB	THD	–	0.05	–	%
for $V_{i(rms)}$ = 0.6 V; gain = 0 dB to –40 dB	THD	–	0.07	0.4	%
for $V_{i(rms)}$ = 2.0 V; gain = –12 dB to –40 dB	THD	–	0.1	–	%
Channel separation at 10 kHz gain = 0 dB	α_{cs}	–	80	–	dB
Ripple rejection (gain = 0 dB; bass and treble in linear position) f_{ripple} = 100 Hz	RR_{100}	–	50	–	dB
Crosstalk attenuation from logic inputs to AF outputs (gain = 0 dB; bass and treble in linear position)	α_L	–	100	–	dB
VOLUME CONTROL					
For truth table see Table 6					
Control range at f = 1 kHz (36 steps)					
maximum voltage gain (6 dB step)	G_{max}	5	6	–	dB
minimum voltage gain (–64 dB step)	G_{min}	–63	–64	–	dB
mute position	G_{mute}	–80	–90	–	dB
Gain tracking error; balance in mid-position	G	–	–	2	dB
Step resolution					
gain from 6 dB to –40 dB	G_{step}	1.5	2.0	2.5	dB/step
gain from –42 dB to –64 dB	G_{step}	1.0	2.0	3.0	dB/step
TREBLE CONTROL					
For truth table see Table 8					
Control range for $C_{8\text{-}5}$; $C_{14\text{-}5}$ = 5.6 nF					
Maximum emphasis at 15 kHz with respect to linear position	G	11	12	13	dB
Maximum attenuation at 15 kHz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	2.5	3.0	3.5	dB/step

parameter	symbol	min.	typ.	max.	unit
BASS CONTROL					
For truth table see Table 7					
Control range for C_{6-7}; C_{15-16} = 33 nF					
Maximum emphasis at 40 Hz with respect to linear position	G	14	15	16	dB
Maximum attenuation at 40 Hz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	2.5	3.0	3.5	dB/step
SPATIAL AND PSEUDO FUNCTION					
Spatial: Antiphase crosstalk	α	–	52	–	%
Pseudo: Phase shift (see Fig. 8)					

DEVELOPMENT DATA

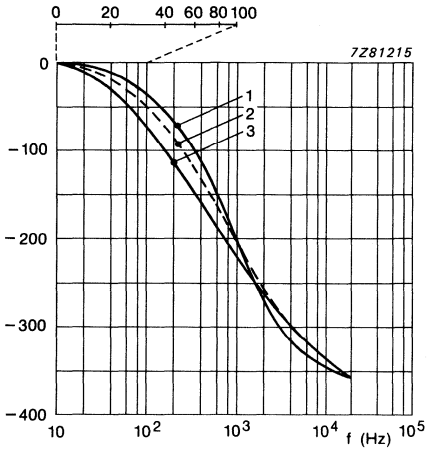
Note to the AC characteristics

1. Balance is realized via software by different volume settings in both channels (left and right).



$t_{SU;STA}$ = start code set-up time.
$t_{HD;STA}$ = start code hold time.
$t_{SU;STO}$ = stop code set-up time.
t_{BUF} = bus free time.
$t_{SU;DAT}$ = data set-up time.
$t_{HD;DAT}$ = data hold time.

Fig. 7 Timing requirements for I²C-bus.



curve	pin 17 (nF)	pin 19 (nF)	effect
1	15	15	normal
2	5.6	47	intensified
3	5.6	68	more intensified

Fig. 8 Pseudo (phase in degrees) as a function of frequency (left output).

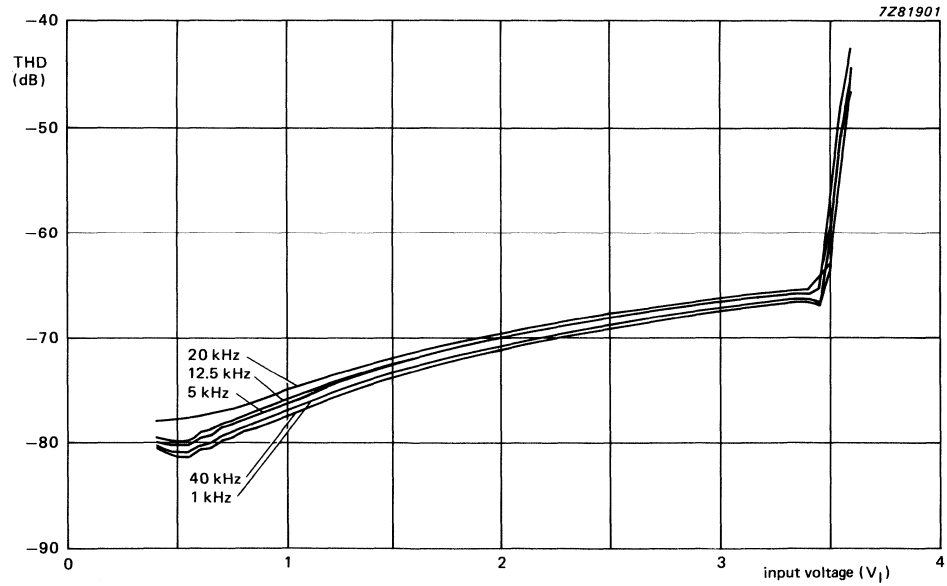


Fig. 9 Input signal handling capability; gain = −10 dB; R_S = 600 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

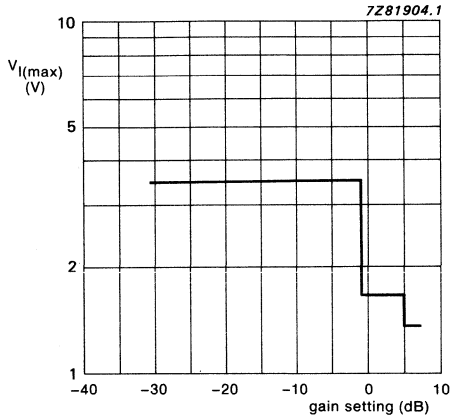


Fig. 10 Input signal handling capacility plotted against gain setting; THD = −60 dB; f = 1 kHz; R_S = 600 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

DEVELOPMENT DATA

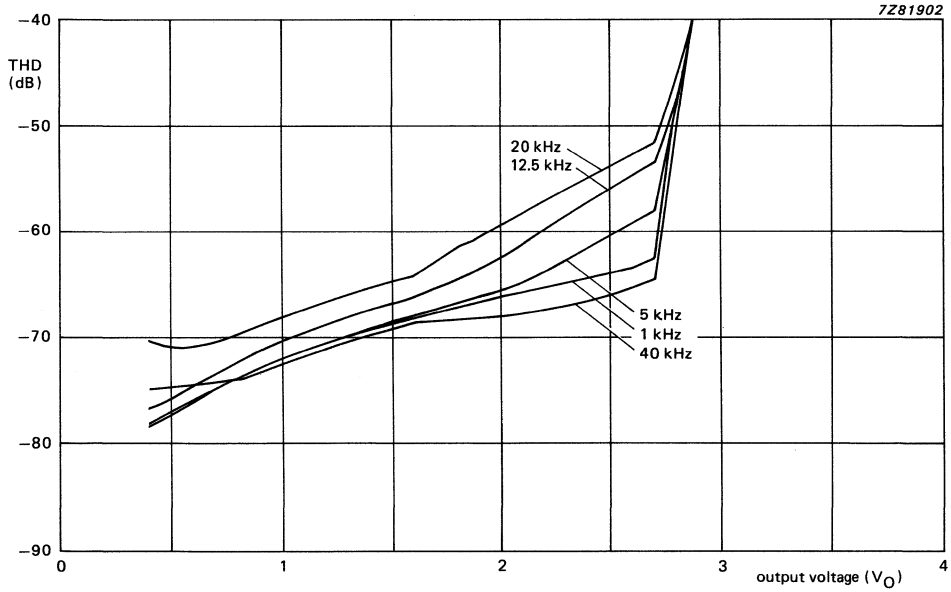


Fig. 11 Output signal handling capability; gain = 6 dB; R_S = 600 Ω; R_L = 10 kΩ, bass/trebble = 0 dB, V_{CC} = 12 V.

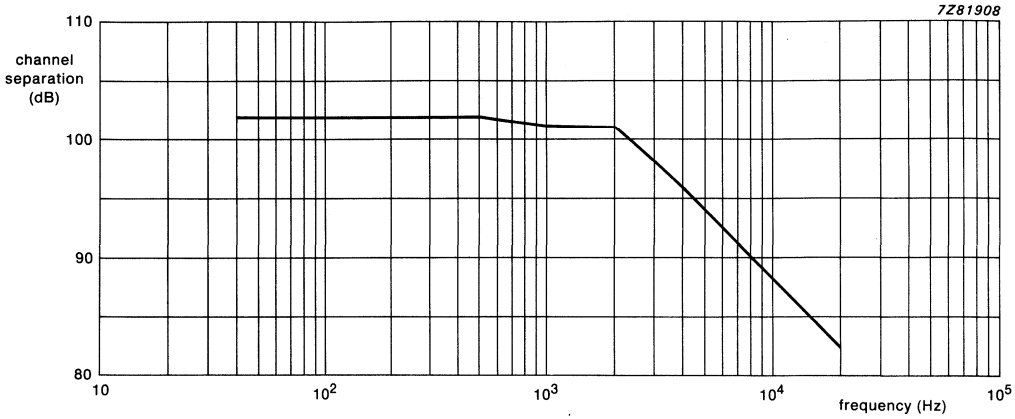
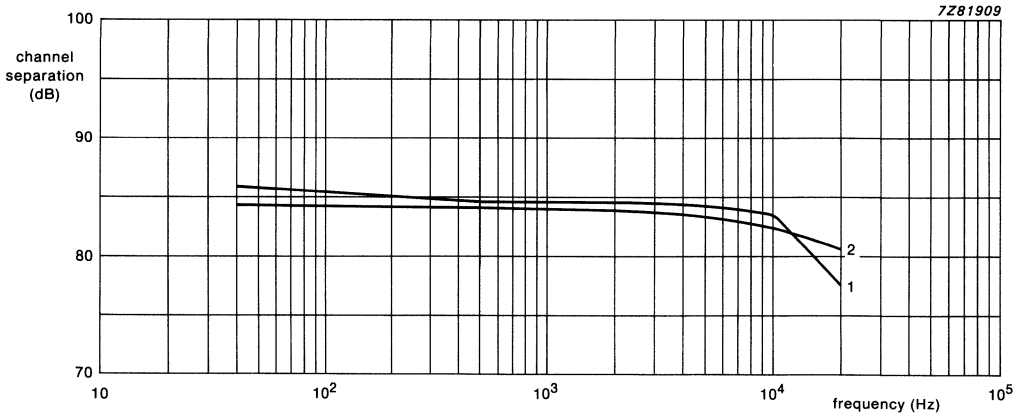


Fig. 12 Source selector separation (channel 2 and channel 1); gain = 0 dB; V_{i1} = 0 V; V_{i2} = 1 V, R_S = 0 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.



(1) gain = 0 dB; V_i = 1.0 V.
(2) gain = 6 dB; V_i = 0.5 V.

Fig. 13 Stereo channel separation as a function of frequency; R_S = 0 Ω, R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

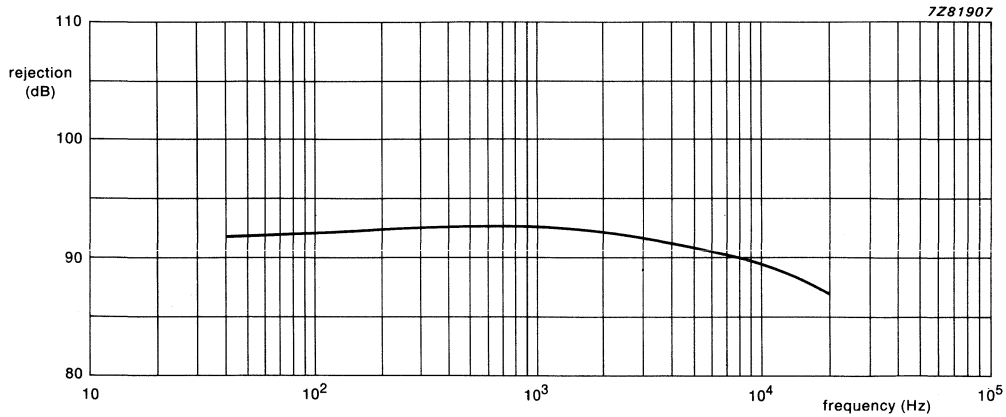


Fig. 14 Mute signal rejection as a function of frequency; gain = 0 dB; V_i = 1.0 V; R_S = 0 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

DEVELOPMENT DATA

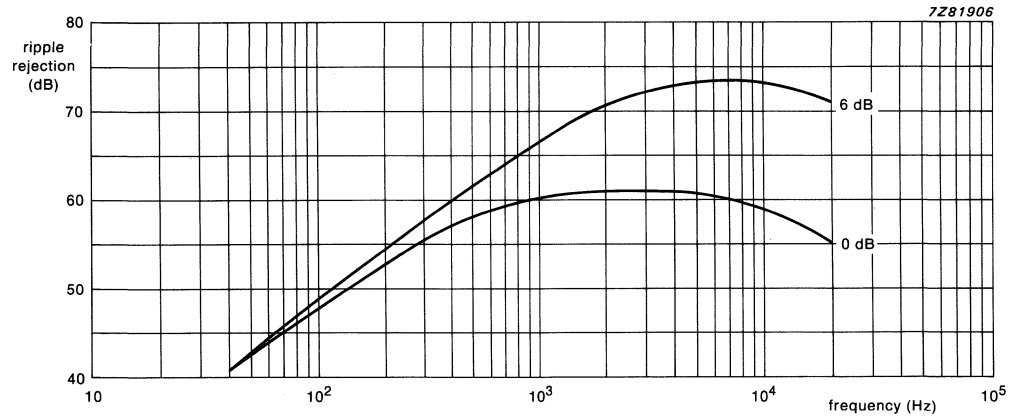


Fig. 15 Ripple rejection as a function of frequency; voltage ripple = 0.3 V (rms); R_S = 0 Ω, R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

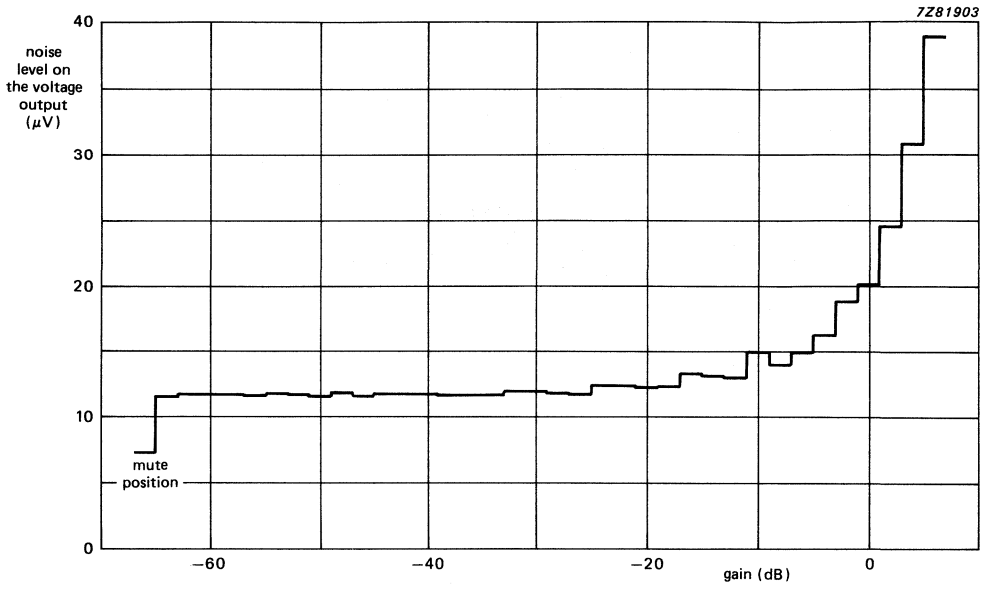


Fig. 16 Noise output voltage as a function of gain; weighted CCIR468 quasi peak gain, + 6 dB to −64 dB; V_i = 0 V, R_S = 0 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

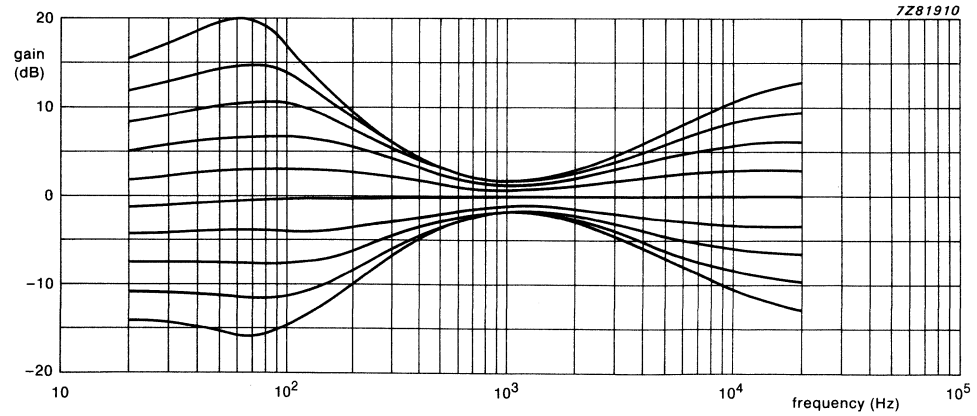


Fig. 17 Frequency response of bass and trebble control; bass and trebble gain settings = −12 to + 15 dB; gain is 0 dB; V_i = 0.1 V; R_{S9} = 600 Ω; R_L = 10 kΩ; V_{CC} = 12 V.

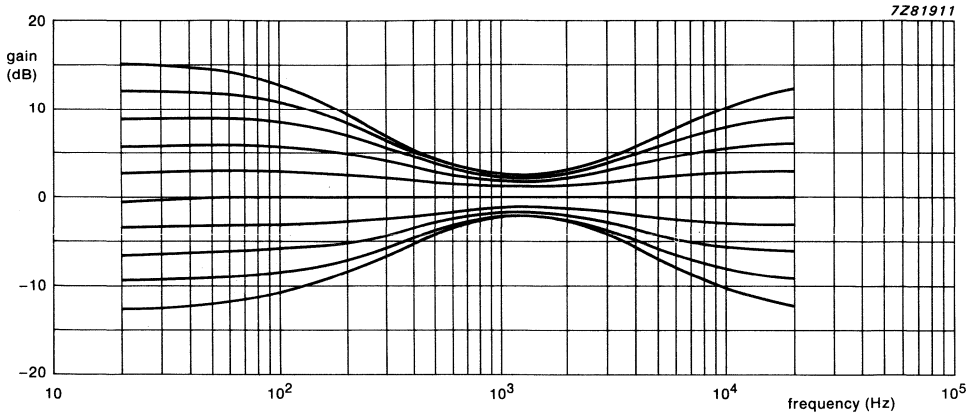


Fig. 18 Tone control with T-filter.

DEVELOPMENT DATA

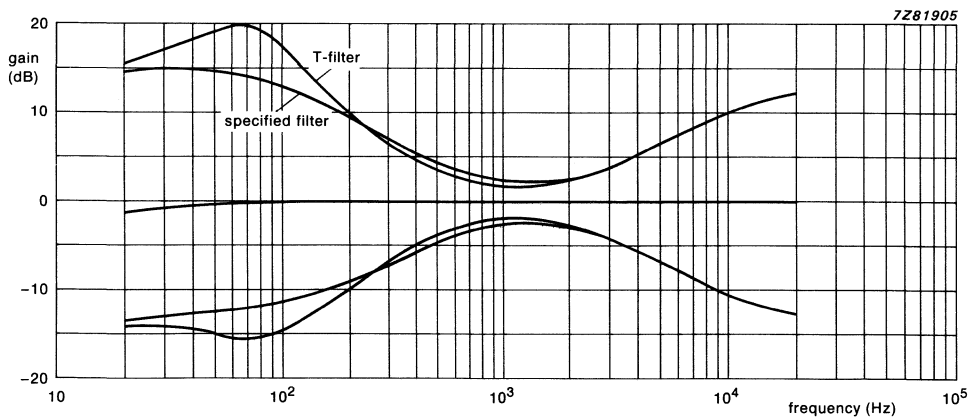


Fig. 19 Tone control.

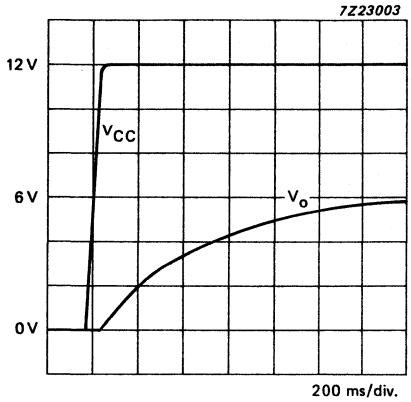


Fig. 20 Turn-on behaviour;
$C = 2.2\ \mu F$; $R_L = 10\ k\Omega$.

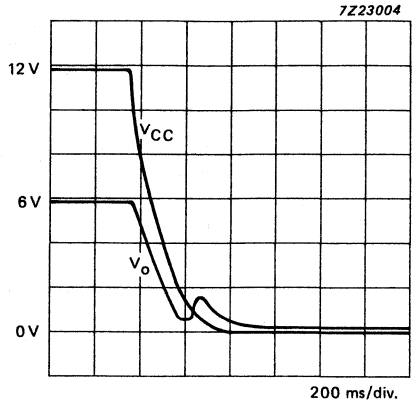


Fig. 21 Turn-off behaviour;
without modulation.

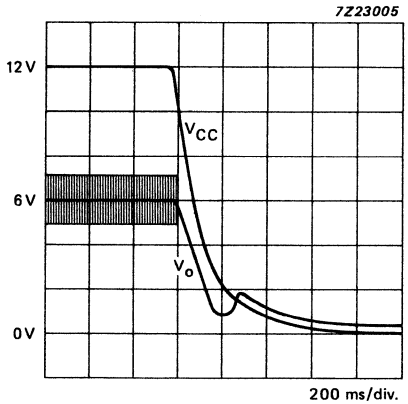
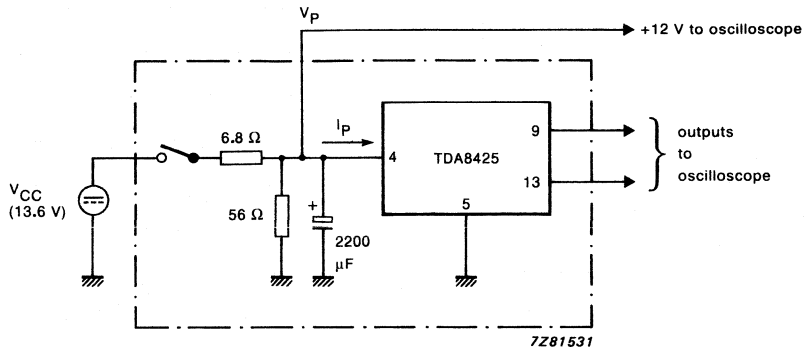


Fig. 22 Turn-off behaviour; with modulation (shaded area).



I_{CC} = 25 mA
I_{load} = 239 mA
t_{on} = 15 ms
t_{off} = 110 ms

Fig. 23 Turn-on/off power supply circuit diagram.

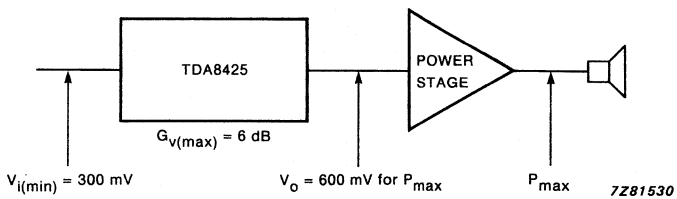


Fig. 24 Level diagram.

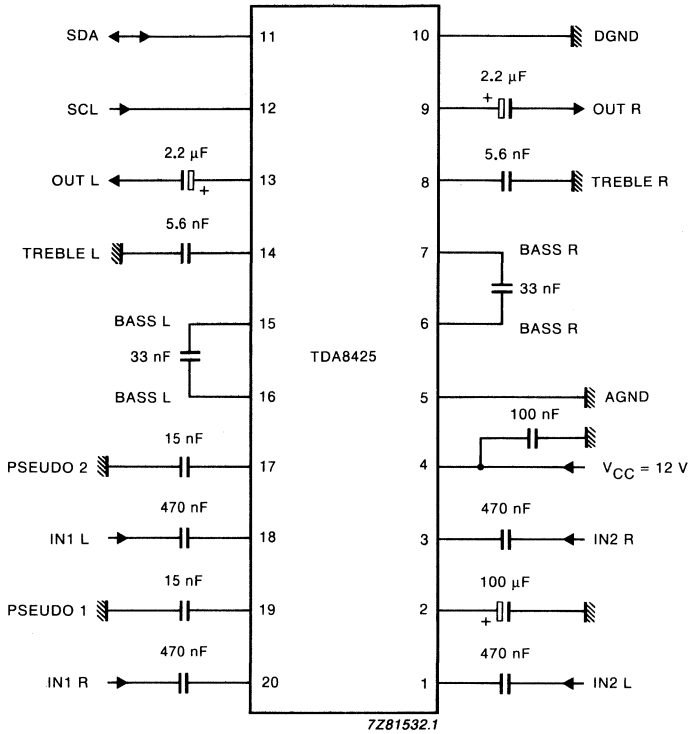


Fig. 25 Test and application circuit diagram.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

SWITCH FOR CTV RECEIVERS

GENERAL DESCRIPTION

The TDA8440 is a versatile video/audio switch, intended to be used in CTV receivers equipped with an AUXILIARY VIDEO/AUDIO plug.

It provides two 3-state switches for audio channels and one 3-state switch for the video channel and a video amplifier with selectable gain (times 1 or times 2).

The integrated circuit can be used in conjunction with a microcontroller from the MAB8400 family, and is controlled via a bidirectional I^2C bus. Sufficient sub-addressing is provided for the I^2C bus mode. It can also be controlled directly by d.c. switching signals.

Features

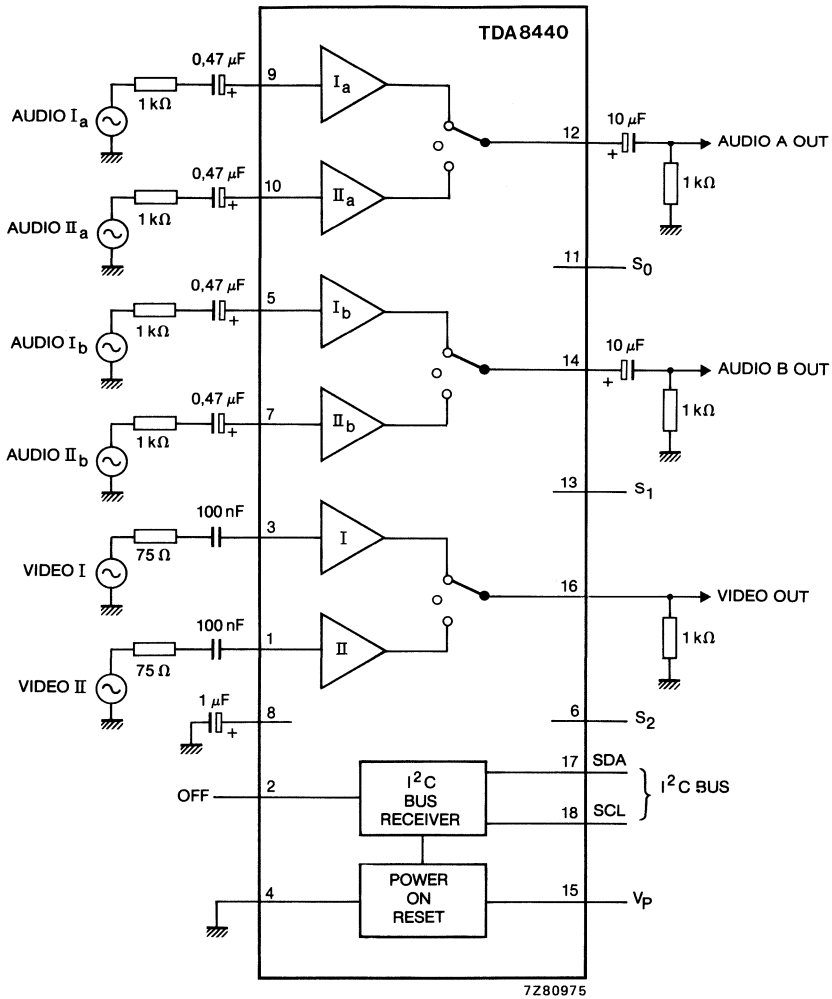
- Combined analogue and digital circuitry gives maximum flexibility in channel switching
- 3-state switches for all channels
- Selectable gain for the video channels
- Sub-addressing facility
- I^2C bus or non-I^2C bus mode (controlled by d.c. voltages)
- Slave receiver in the I^2C bus mode
- External OFF command
- System expansion possible up to 7 devices (14 sources)
- Static short-circuit proof outputs

QUICK REFERENCE DATA

Supply voltage range	V_{15-4}	10 to 13,2	V
Supply current (without load)	I_{15}	typ. 33 max. 50	mA mA
Storage temperature	T_{stg}	max. + 125	°C
Operating ambient temperature range	T_{amb}	0 to + 70	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



S0, S1, S2 and OFF (pins 11, 13, 6 and 2) connected to V_P or GND.
If more than 1 device is used, then the outputs and the pins 8 (bias decoupling of the audio inputs) mau may be connected in parallel.

Fig. 1 Block diagram and test circuit.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

The TDA8440 is a monolithic system of switches and can be used in CTV receivers equipped with an AUXILIARY VIDEO/AUDIO plug.

The IC incorporates 3-state switches they comprise:

a) An electronic video switch with selectable gain (times 1 or times 2) for switching between an internal video signal (from the IF amplifier) and an AUXILIARY input signal.

b) Two electronic audio switches, for two sound channels (stereo or dual language), for switching between internal audio sources and signals from the AUXILIARY VIDEO/AUDIO plug.

A selection can be made between two input signals and an OFF-state. The OFF-state is necessary if more than one TDA8440 device is used.

The SDA and SCL pins can be connected to the I²C bus or to d.c. switching voltages. Inputs S_0 (pin 11), S_1 (pin 13), and S_2 (pin 6) are used for selection of sub-addresses or switching to the non-I²C mode. Inputs S_0, S_1 and S_2 can be connected to the supply voltage (H) or to ground (L). In this way no peripheral components are required for selection.

Table 1 Sub-addressing

			sub-address		
S_2	S_1	S_0	A_2	A_1	A_0
L	L	L	0	0	0
L	L	H	0	0	1
L	H	L	0	1	0
L	H	H	0	1	1
H	L	L	1	0	0
H	L	H	1	0	1
H	H	L	1	1	0
H	H	H	non I²C addressable		

NON-I²C BUS CONTROL

If the TDA8440 switching device has to be operated via the AUXILIARY VIDEO/AUDIO plug, inputs S_2, S_1 and S_0 must be connected to the supply line (12 V).

The sources (internal and external) and the gain of the video amplifier can be selected via the SDA and SCL pins with the switching voltage from the AUXILIARY VIDEO/AUDIO plug:

- Sources I are selected if SDA = 12 V (external source)
- Sources II are selected if SDA = 0 V (TV mode)
- Video amplifier gain is 2 x if SCL = 12 V (external source)
- Video amplifier gain is 1 x if SCL = 0 V (TV mode)

If more than one TDA8440 device is used in the non-I²C bus system, the OFF pin can be used to switch off the desired devices. This can be done via the 12 V switching voltage on the AUXILIARY VIDEO/AUDIO plug.

- All switches are in the OFF position if OFF = H (12 V)
- All switches are in the selected position via SDA and SCL pins if OFF = L (0 V)

I²C BUS CONTROL

Detailed information on the I²C bus is available on request.

Table 2 TDA8440 I²C bus protocol.

STA	A_6	A_5	A_4	A_3	A_2	A_1	A_0	R/W	AC	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	AC	STO

STA = start condition
A_6 = 1
A_5 = 0
A_4 = 0
A_3 = 1
} Fixed address bits
A_2 = sub-address bit, fixed via S_2 input
A_1 = sub-address bit, fixed via S_1 input
A_0 = sub-address bit, fixed via S_0 input
R/W = read/write bit (has to be 0, only write mode allowed)
AC = acknowledge bit (= 0) generated by the TDA8440
D_7 = 1 audio Ia is selected to audio output a
D_7 = 0 audio Ia is not selected
D_6 = 1 audio IIa is selected to audio output a
D_6 = 0 audio IIa is not selected
D_5 = 1 audio Ib is selected to audio output b
D_5 = 0 audio Ib output is not selected
D_4 = 1 audio IIb is selected to audio output b
D_4 = 0 audio IIb is not selected
D_3 = 1 video I is selected to video output
D_3 = 0 video I is not selected
D_2 = 1 video II is selected to video output
D_2 = 0 video II is not selected
D_1 = 1 video amplifier gain is times 2
D_1 = 0 video amplifier gain is times 1
D_0 = 1 OFF-input inactive
D_0 = 0 OFF-input active
STO = stop condition

OFF FUNCTION

With the OFF input all outputs can be switched off (mode high ohmic), depending on the value of D_0.

D_0/OFF gating

D_0	OFF input	Outputs
0 (off input active)	H	OFF
0	L	in accordance with last defined D_7-D_1 (may be entered while OFF = HIGH)
1 (off input inactive)	H	in accordance with D_7-D_1
1	L	in accordance with D_7-D_1

DEVELOPMENT DATA

Power-on reset

The circuit is provided with a power-on reset function.

When the power supply is switched on an internal pulse will be generated that will reset the internal memory S_0, in the initial state all the switches will be in the off position and the OFF input is active (D_7-D_0 = 0) (I^2C mode), position defined via SDA and SCL inputs (non-I^2C mode).

When the power supply decreases below 5 V a pulse will be generated and the internal memory will be reset. The behaviour of the switches will be the same as described above.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

		min.	typ.	max.	unit
Supply voltage	pin 15 V_P	–	–	14	V
Input voltage range	pin 17 V_{SDA}	−0,3	–	V_P + 0,3	V
	pin 18 V_{SCL}	−0,3	–	V_P + 0,3	V
	pin 2 V_{OFF}	−0,3	–	V_P + 0,3	V
	pin 11 V_{S0}	−0,3	–	V_P + 0,3	V
	pin 13 V_{S1}	−0,3	–	V_P + 0,3	V
	pin 6 V_{S2}	−0,3	–	V_P + 0,3	V
Video output current	pin 16 $-I_{16}$	–	–	50	mA
Storage temperature range	T_{stg}	–	–	+ 125	°C
Operating ambient temperature range	T_{amb}	0	–	+ 70	°C
Junction temperature	T_j	–	–	+ 150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	50	K/W

CHARACTERISTICS

T_{amb} = 25 °C; V_P = 12 V; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_{15-4}	10	–	13,2	V
Supply current (without load)	I_{15}	–	37	50	mA
Video switch					
Input coupling capacitor	C_1C_3	100	–	–	nF
Voltage gain (times 1; SLC = L)	A_{3-16}	−1	0	+ 1	dB
(times 2; SCL = H)	A_{3-16}	+5	+ 6	+ 7	dB
Voltage gain (times 1; SCL = L)	A_{1-16}	−1	0	+ 1	dB
(times 2; SCL = H)	A_{1-16}	+5	+ 6	+ 7	dB
Input video signal amplitude (gain times 1)	V_{3-4}	–	–	4,5	V
Input video signal amplitude (gain times 1)	V_{1-4}	–	–	4,5	V
Output impedance	Z_{16-4}	–	7	–	Ω
Output impedance in 'OFF' state	Z_{16-4}	100	–	–	kΩ
Isolation (off state) (f_o = 5 MHz)		60	–	–	dB
Signal-to-noise ratio (note 2)	S/S + N	60	–	–	dB
Output top-sync level	V_{16-4}	2,4	2,8	3,2	V
Differential gain	G	–	–	3	%
Minimum crosstalk attenuation (note 1)	V_{16-4}	60	–	–	dB
Supply voltage rejection (note 3)	RR	36	–	–	dB
Bandwidth (1 dB)	B	10	–	–	MHz
Crosstalk attenuation for interference caused by bus signals (source impedance 75 Ω)	α	60	–	–	dB
Audio switch a and b					
Input signal level	$V_{9-4(rms)}$	–	–	2	V
	$V_{10-4(rms)}$	–	–	2	V
	$V_{5-4(rms)}$	–	–	2	V
	$V_{7-4(rms)}$	–	–	2	V
Input impedance	Z_{9-4}	50	100	–	kΩ
	Z_{10-4}	50	100	–	kΩ
	Z_{5-4}	50	100	–	kΩ
	Z_{7-4}	50	100	–	kΩ
Output impedance	Z_{12-4}	–	–	10	Ω
	Z_{14-4}	–	–	10	Ω
Output impedance (off state)	Z_{14-4}	100	–	–	kΩ

parameter	symbol	min.	typ.	max.	unit
Voltage gain	$V_{9\text{-}12}$	−1	0	+ 1	dB
	$V_{10\text{-}12}$	−1	0	+ 1	dB
	$V_{5\text{-}14}$	−1	0	+ 1	dB
	$V_{7\text{-}14}$	−1	0	+ 1	dB
Isolation (off state) (f = 20 kHz)		90	–	–	dB
Signal-to-noise ratio (note 4)	S/S + N	90	–	–	dB
Total harmonic distortion (note 6)	THD	–	–	0,1	%
Crosstalk attenuation for interferences caused by video signals (note 5)					
Weighted	α	80	–	–	dB
Unweighted	α	80	–	–	dB
Crosstalk attenuation for interferences caused by sinusoidal sound signals (note 5)	α	80	–	–	dB
Crosstalk attenuation for interferences caused by the bus signal (weighted) (source impedance = 1 kΩ)		80	–	–	dB
Supply voltage rejection	RR	50	–	–	dB
Bandwidth (−1 dB)	B	50	–	–	kHz
I^2C bus inputs/outputs SDA (pin 17) and SCL (pin 18)					
Input voltage HIGH	V_{IH}	3	–	V_P	V
Input voltage LOW	V_{IL}	−0,3	–	+ 1,5	V
Input current HIGH*	I_{IH}	–	–	10	μA
Input current LOW*	I_{IL}	–	–	10	μA
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	5	–	mA
Capacitance of SDA and SDL inputs, pins 17 and 18	C_I	–	–	10	pF
Sub-address inputs S_0 (pin 11), S_1 (pin 13), S_2 (pin 6)					
Input voltage HIGH	V_{IH}	3	–	V_P	V
Input voltage LOW	V_{IL}	−0,3	–	+ 0,4	V
Input current HIGH	I_{IH}	–	–	10	μA
Input current LOW	I_{IL}	−50	–	0	μA
OFF input (pin 2)					
Input voltage HIGH	V_{IH}	+3	–	V_P	V
Input voltage LOW	V_{IL}	−0,3	–	+ 0,4	V
Input current HIGH	I_{IH}	–	–	20	μA
Input current LOW	I_{IL}	−10	–	2	μA

* Also if the supply is switched off.

DEVELOPMENT DATA

CHARACTERISTICS (continued)

I^2C bus load conditions are as follows:
4 kΩ pull-up resistor to + 5 V; 200 pF to GND.
All values are referred to V_{IH} = 3 V and V_{IL} = 1,5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4	–	–	μs
Start condition set-up time	$t_{s(STA)}$	4	–	–	μs
Start condition hold time	$t_{h(STA)}$	4	–	–	μs
SCL, SDA LCW period	t_{LOW}	4	–	–	μs
SCL, HIGH period	t_{HIGH}	4	–	–	μs
SCL, SDA rise time	t_r	–	–	1	μs
SCL, SDA fall time	t_f	–	–	0,3	μs
Data set-up time (write)	$t_{s(DAT)}$	1	–	–	μs
Data hold time (write)	$t_{h(DAT)}$	1	–	–	μs
Acknowledge (from TDA8440) set-up time	$t_{s(CAC)}$	–	–	2	μs
Acknowledge (from TDA8440) hold time	$t_{h(CAC)}$	0	–	–	μs
Stop condition set-up time	$t_{s(STO)}$	4	–	–	μs

Notes to the characteristics

1. Caused by drive on any other input at maximum level, measured in B = 5 MHz, source impedance for the used input 75 Ω,

   $$\text{crosstalk} = 20 \log \frac{V_{out}}{V_{IN\ max}}.$$

2. $$S/N = 20 \log \frac{V_O \text{ video noise (p-p) (2 V)}}{V_O \text{ noise rms B = 5 MHz}}.$$

3. $$\text{Supply voltage ripple rejection} = 20 \log \frac{V_r \text{ supply}}{V_r \text{ on output}} \text{ at f = max. 100 kHz.}$$

4. $$S/N = 20 \log \frac{V_O \text{ nominal (0,5 V)}}{V_O \text{ noise B = 20 kHz}}.$$

5. Caused by drive of any other input at maximum level, measured in B = 20 kHz, source impedance of the used input = 1 kΩ,

   $$\text{crosstalk} = 20 \log \frac{V_{out}}{V_{in\ max}}$$ according to DIN 45405 (CCIR 468).

6. f = 20 Hz to 20 kHz.
7. All outputs are short-circuit proof (static).
8. The inputs and output (apart from SDA, SCL and OFF) withstand tests of MIL-STD-883 C. It is advisable to connected series resistors to these pins.
9. Timings $t_{S,\ DAT}$ and $t_{H,\ DAT}$ deviate from the I^2C bus specification. After reset has been activated, transmission may only be started after a 50 μs delay.

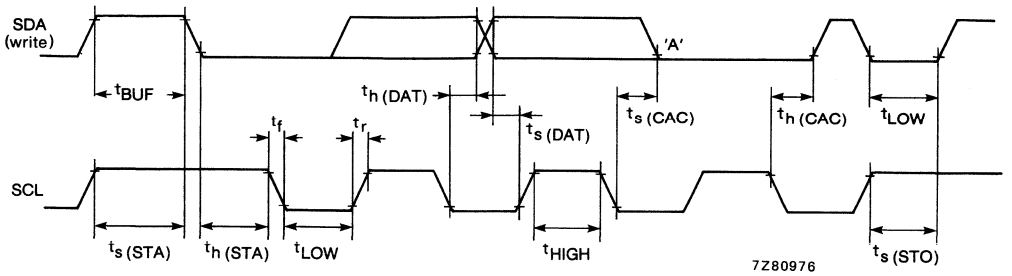


Fig. 2 Timing diagram I^2C bus.

DEVELOPMENT DATA

Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

I²C-BUS INTERFACE FOR COLOUR DECODERS

GENERAL DESCRIPTION

The TDA8442 provides control of four analogue functions and has one high-current and two switching outputs. Control of the IC is performed via the two-line, bidirectional I²C-bus.

Features

- Four analogue control outputs
- One high-current output port (npn open emitter)
- Two switching output ports (npn collector with internal pull-up resistor)
- I²C-bus slave receiver
- Power-down reset

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 9)		V_P	10.8	12.0	13.2	V
Supply current	no outputs loaded	I_P	8	13	18	mA
Total power dissipation	no outputs loaded	P_{tot}	–	–	1	W
Operating ambient temperature range		T_{amb}	–20	–	+ 70	°C

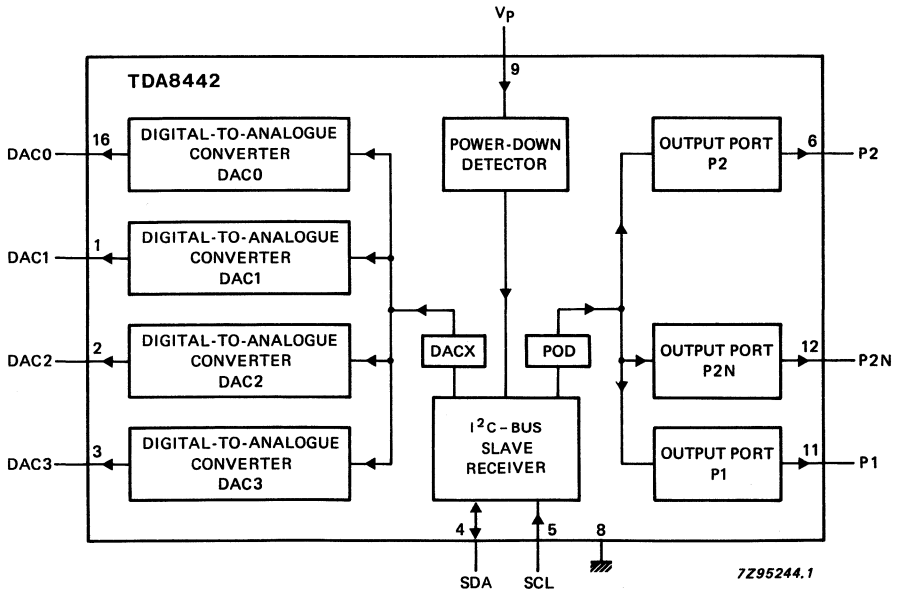


Fig. 1 Block diagram.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

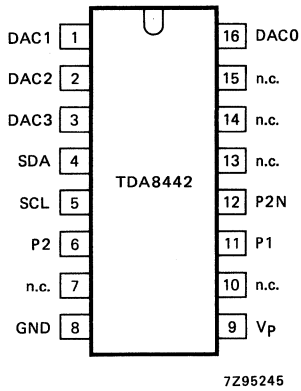


Fig. 2 Pinning diagram

PINNING

1	DAC1	analogue output 1
2	DAC2	analogue output 2
3	DAC3	analogue 3
4	SDA	serial data line } I^2C-bus
5	SCL	serial clock line } I^2C-bus
6	P2	Port 2 npn collector output with internal pull-up resistor
7	n.c.	not connected
8	GND	supply return (ground)
9	V_P	positive supply voltage
10	n.c.	not connected
11	P1	Port 1 open npn emitter output
12	P2N	inverted P2 output
13	n.c.	not connected
14	n.c.	not connected
15	n.c.	not connected
16	DAC0	analogue output 0

FUNCTIONAL DESCRIPTION

Control

Analogue control is facilitated by four 6-bit digital-to-analogue converters (DAC0 to DAC3). The values of the output voltages from the DACs are set via the I^2C-bus.

The high-current output port (P1) is suitable for switching between internal and external RGB signals. It is an open npn emitter output capable of sourcing 14 mA (min.).

The two output ports (P2 and P2N) can be used for NTSC/PAL switching. These are npn collector outputs with internal pull-up resistors of 10 kΩ (typ.). Both outputs are capable of sinking up to 2 mA with a voltage drop of less than 400 mV. If one output is switched on (LOW), the other output is switched off, and vice versa.

Reset

The power-down-reset mode occurs whenever the positive supply voltage falls below 8.5 V (typ.) and resets all registers to a defined state.

OPERATION

Write

The TDA8442 is controlled via the I²C-bus (specifications for the I²C-bus will be supplied on request). Programming of the TDA8442 is performed using the format shown in Fig. 3.

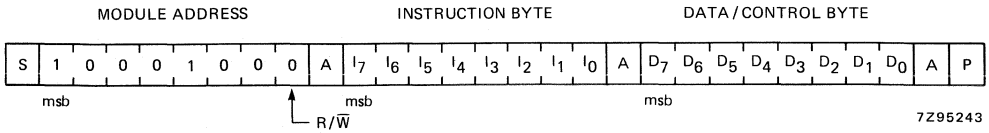


Fig. 3 TDA8442 programming format.

Acknowledge (A) is generated by the TDA8442 only when a valid address is received and the device is not in the power-down-reset mode ($V_P > 8.5$ V (typ.)).

Control

Control is implemented by the instruction bytes POD (port output data) and DACX (digital-to-analogue converter control) together with the corresponding data/control bytes (see Fig. 4).

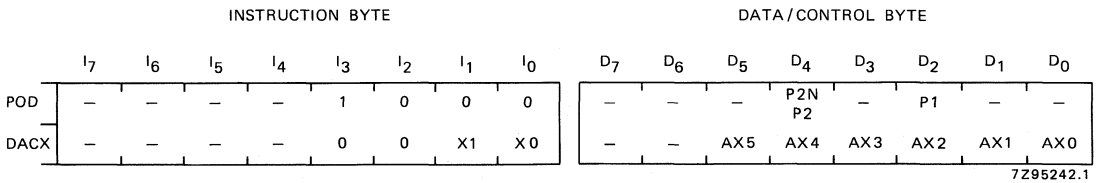


Fig. 4 Control programming.

POD bit P1: If a logic 1 is programmed, the P1 output is switched on. If a logic 0 is programmed or after a power-down-reset, the P1 output is switched off (high-impedance state).

POD bit P2/P2N: If a logic 1 is programmed, the P2 output is switched off and the P2N output is switched on (LOW). If a logic 0 is programmed or after a power-down-reset, the P2 output is switched on (LOW) and the P2N output is switched off.

DAX bits AX5 to AX0: The digital-to-analogue converter selected corresponds to the decimal equivalent of the two bits X1 and X0. The output voltage of the selected DAC is programmed using bits AX5 to AX0, the lowest value being with all data AX5 to AX0 at logic 0 or when power-down-reset has been activated.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 9)	V_P	−0.3	+ 13.2	V
Input/output voltage ranges				
pin 4	V_{SDA}	−0.3	+ 13.2	V
pin 5	V_{SCL}	−0.3	+ 13.2	V
pin 6	V_{P2}	−0.3	V_P*	V
pin 11	V_{P1}	−0.3	V_P*	V
pin 12	V_{P2N}	−0.3	V_P*	V
pins 1 to 3 and pin 16	V_{DAX}	−0.3	V_P*	V
Total power dissipation	P_{tot}	–	1	W
Operating ambient temperature range	T_{amb}	−20	+ 70	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = + 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage (pin 9)		V_P	10.8	12.0	13.2	V
Supply current (pin 9)	no outputs loaded	I_P	8	13	18	mA
I²C-bus inputs						
SDA (pin 4); SCL (pin 5)						
Input voltage HIGH	note 1	V_{IH}	3.0	–	V_P−1	V
Input voltage LOW		V_{IL}	−0.3	–	1.5	V
Input current HIGH	note 1	I_{IH}	–	–	10	μA
Input current LOW	note 1	I_{IL}	–	–	10	μA
I²C-bus output						
SDA (pin 4)	open collector					
Output voltage LOW	I_{OL} = 3.0 mA	V_{OL}	–	–	0.4	V
Maximum output sink current		I_{OL}	3	5	–	mA

* Pin voltage may exceed V_P if the current in that pin is limited to 10 mA.

parameter	conditions	symbol	min.	typ.	max.	unit
Ports P2 and P2N (pins 6 and 12)	npn collector output with pull-up resistor to V_P					
Internal pull-up resistor to V_P		R_O	5	10	15	kΩ
Output voltage switched on (LOW)	I_{OL} = 2 mA	V_{OL}	–	–	0.4	V
Maximum output sink current		I_{OL}	2	5	–	μA
Leakage current output switched off		$-I_{leak}$	–	–	25	μA
Port P1 (pin 11)	open npn emitter output					
Output current switched on	V_O = 0 to 5 V	I_O	14	–	–	mA
Leakage current switched off	V_O = 0 to V_P	$\pm I_{leak}$	–	–	100	μA
Digital-to-analogue outputs	note 2					
DAC0 (pin 16)						
Maximum output voltage	unloaded; note 3	$V_{O\,max}$	3.0	–	4.25	V
Minimum output voltage	unloaded; note 3	$V_{O\,min}$	0.15	–	1.0	V
Positive value of smallest step	I_O = 2 mA (1 lsb); note 3	$V_{O\,lsb}$	16	–	72	mV
Deviation from linearity	I_O = 2 mA	ΔV	–	–	45	mV
Output impedance	I_O = –2 to + 2 mA	Z_O	–	–	30	Ω
Maximum output source current		$-I_{OH}$	2	–	6	mA
Maximum output sink current		I_{OL}	2	8	–	mA
DAC1 (pin 1)						
Maximum output voltage	unloaded; note 3	$V_{O\,max}$	4.0	–	5.0	V
Minimum output voltage	unloaded; note 3	$V_{O\,min}$	1.0	–	1.7	V
Positive value of smallest step	I_O = 2 mA (1 lsb); note 3	$V_{O\,lsb}$	18	–	86	mV
Deviation from linearity	I_O = 2 mA	ΔV	–	–	50	mV
Output impedance	I_O = –2 to + 2 mA	Z_O	–	–	30	Ω
Maximum output source current		$-I_{OH}$	2	–	6	mA
Maximum output sink current		I_{OL}	2	8	–	mA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Digital-to-analogue outputs (continued)						
DAC2 (pin 2)						
Maximum output voltage	unloaded; note 3	$V_{O\,max}$	4.0	–	5.0	V
Minimum output voltage	unloaded; note 3	$V_{O\,min}$	1.0	–	1.7	V
Positive value of smallest step	I_O = 2 mA (1 lsb); note 3	$V_{O\,lsb}$	18	–	86	mV
Deviation from linearity	I_O = 2 mA	ΔV	–	–	50	mV
Output impedance	I_O = −2 to + 2 mA	Z_O	–	–	30	Ω
Maximum output source current		$-I_{OH}$	2	–	6	mA
Maximum output sink current		I_{OL}	2	8	–	mA
DAC3 (pin 3)						
Maximum output voltage	unloaded; note 3	$V_{O\,max}$	10.0	–	11.2	V
Minimum output voltage	unloaded; note 3	$V_{O\,min}$	0.1	–	1.0	V
Positive value of smallest step	I_O = 2 mA (1 lsb); note 3	$V_{O\,lsb}$	70	–	250	mV
Deviation from linearity	I_O = 2 mA	ΔV	–	–	150	mV
Output impedance	I_O = −2 to + 2 mA	Z_O	–	–	30	Ω
Maximum output source current		$-I_{OH}$	2	–	6	mA
Maximum output sink current		I_{OL}	2	8	–	mA
Power-down reset						
Maximum value of V_P at which power-down reset is active		V_{PD}	6	–	10	V
Rise time of V_P during power-on	V_P rising from 0 V to V_{PD}	t_r	5	–	–	μs

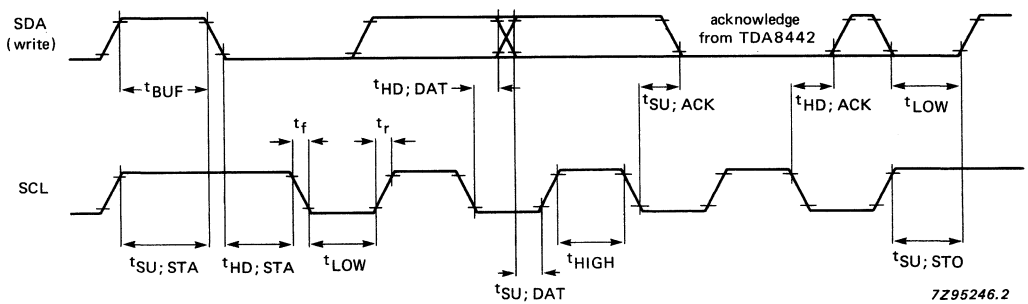
Notes to the characteristics

1. If $V_p < 1$ V, the input current is limited to 10 μA at input voltages up to 13.2 V.
2. Pure capacitive load should be avoided because of possible oscillations.
3. Values are proportional to V_P.

I²C-BUS TIMING

Bus loading conditions: 4 kΩ pull-up resistor to + 5 V; 200 pF capacitor to GND. All values are referred to V_{IH} = 3 V and V_{IL} = 1.5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4.0	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4.0	–	–	μs
Start condition hold time	$t_{HD;STA}$	4.0	–	–	μs
LOW period SCL, SDA	t_{LOW}	4.0	–	–	μs
HIGH period SCL	t_{HIGH}	4.0	–	–	μs
Rise time SCL, SDA	t_r	–	–	1.0	μs
Fall time SCL, SDA	t_f	–	–	0.30	μs
Data set-up time (write)	$t_{SU;DAT}$	1	–	–	μs
Data hold time (write)	$t_{HD;DAT}$	1	–	–	μs
Acknowledge (from TDA8442) set-up time	$t_{SU;ACK}$	–	–	3.5	μs
Acknowledge (from TDA8442) hold time	$t_{HD;ACK}$	0	–	–	μs
Stop condition set-up time	$t_{SU;STO}$	4.0	–	–	μs



Reference levels are 10 and 90%.

Fig. 5 I²C-bus timing; TDA8442.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

I²C-BUS CONTROLLED YUV/RGB SWITCH

GENERAL DESCRIPTION

The TDA8443A is a general purpose two-channel switch for YUV or RGB signals. One channel provides matrixing from RGB to YUV, which can be bypassed.
The IC ic controlled via I²C-bus by seven different addresses or can be used in a non-I²C-bus mode. In the non-I²C-bus mode, control of the circuit is achieved by DC voltages.

Features

- Two RGB/YUV selectable clamped inputs with associated synchronization
- RGB/YUV matrix
- 3-state switching with an OFF-state
- Selectable gain
- I²C-bus or non-I²C-bus mode
- Address selection for 7 devices
- Fast switching

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 18)		$V_P = V_{18-22}$	10.8	12.0	13.2	V
Supply current		I_P	–	65	90	mA
RGB/YUV channels						
Output impedance						
pin 19		$\|Z_{19-22}\|$	–	7	30	Ω
pin 20		$\|Z_{20-22}\|$	–	7	30	Ω
pin 21		$\|Z_{21-22}\|$	–	7	30	Ω
Bandwidth						
–3 dB	mode 0 or 2	B	–	25	–	MHz
+3 dB	mode 0 or 2	B	–	12	–	MHz
+/–3 dB	mode 1	B	–	10	–	MHz
Maximum output amplitude of YUV signals (peak-to-peak)	gain x 1	$V_{O(p-p)}$	2.1	–	–	V
	gain x 2	$V_{O(p-p)}$	4.2	–	–	V
Operating ambient temperature range		T_{amb}	0	–	+70	°C

PACKAGE OUTLINE

24-lead DIL; plastic with internal heat spreader (SOT101B).

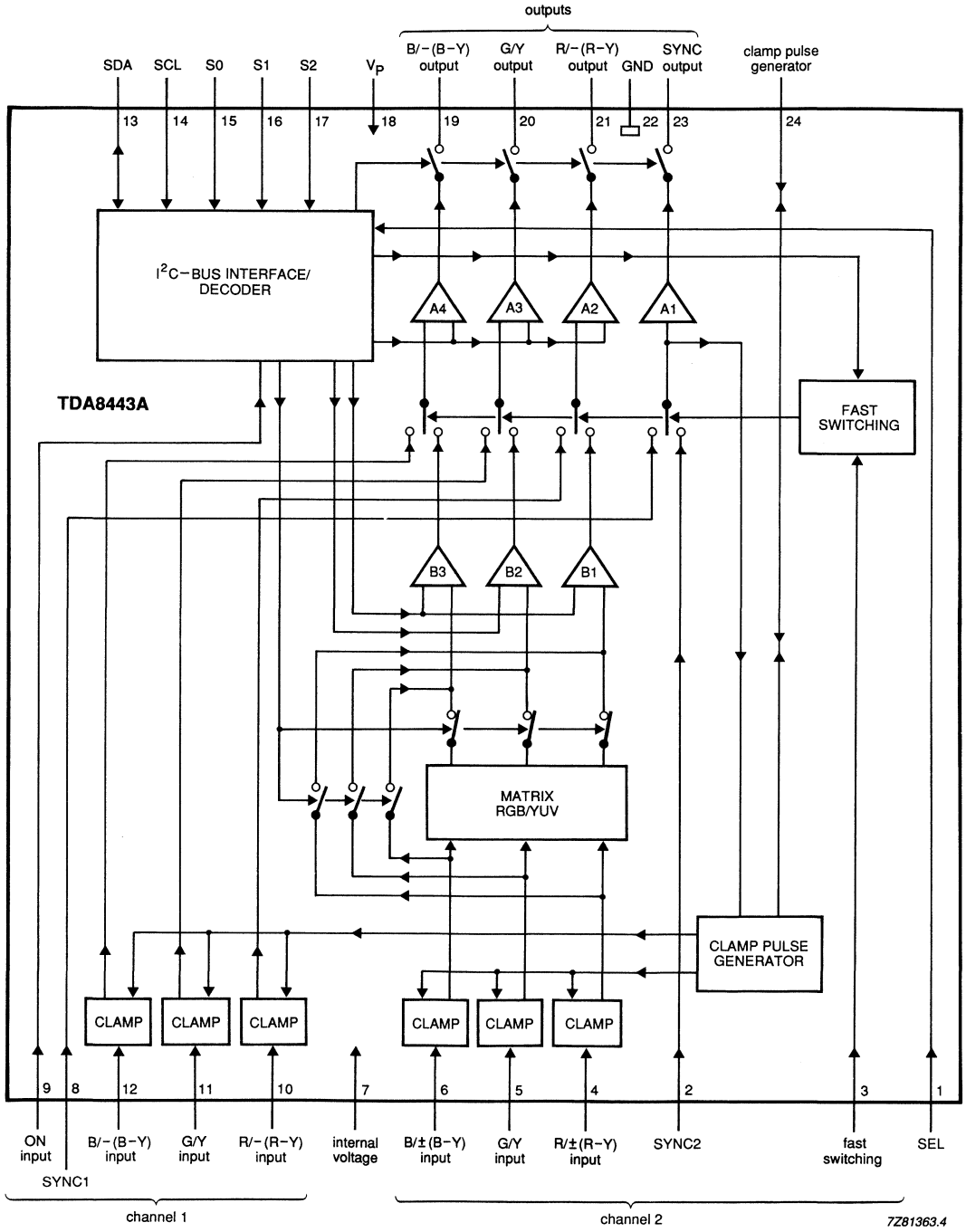


Fig.1 Block diagram.

PINNING

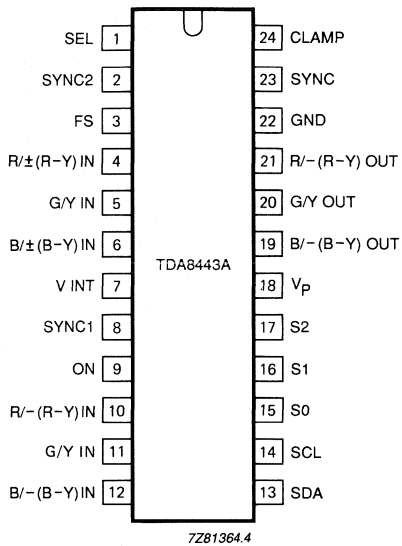


Fig.2 Pinning diagram.

1	SEL	select input (non-I²C-bus mode only)	
2	SYNC2	synchronization input for channel 2	
3	FS	fast switching input	
4	R/± (R-Y) IN	R or (R-Y) signal input	
5	G/Y IN	G or Y signal input	
6	B/± (B-Y) IN	B or (B-Y) signal input	
7	V INT	internal voltage supply	
8	SYNC1	synchronization input for channel 1	
9	ON	ON input	
10	R/−(R-Y) IN	R or −(R-Y) signal input	
11	G/Y IN	G or Y signal input	
12	B/−(B-Y) IN	B or −(B-Y) signal input	
13	SDA	serial data input/output	I²C-bus
14	SCL	serial clock input	I²C-bus
15	S0	address selection inputs	I²C-bus
16	S1	address selection inputs	I²C-bus
17	S2	address selection inputs	I²C-bus
18	V_P	positive supply voltage	
19	B/−(B-Y)	B or −(B-Y) signal output	
20	G/Y OUT	G or Y signal output	
21	R/−(R-Y)	R or −(R-Y) signal output	
22	GND	ground	
23	SYNC	synchronization output	
24	CLAMP	clamping pulse generator input/output	

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

The circuit contains two sets of inputs (see Fig.1). Both channels can receive RGB or YUV signals. Each set of inputs has its own synchronization input, which internally generates a pulse to clamp the inputs. The internal clamping pulse can also be controlled by a signal (e.g. a sandcastle pulse) applied to pin 24. The pulse will occur during the time that the signal at pin 24 is between 5.5 and 6.5 V. If both a sync signal and a pin 24 signal are used the signal should be applied to pin 24 via a 1 kΩ resistor.

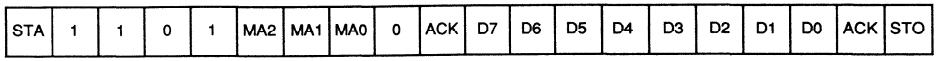
RGB signals of channel 2 can be matrixed to YUV signals.

The outputs can be set in a high impedance OFF state, which allows the use of up to seven devices in parallel (I^2C-bus mode).

The circuit can be controlled by an I^2C-bus compatible microcontroller or directly by DC voltages. The fast switching input can be operated via pin 16 of the peritelevision connector.

I²C-bus mode

The protocol for the devices in I²C-bus mode is shown in Fig.3.



MSA003

Fig.3 I²C-bus protocol.

Where:

STA : start condition
MA2, MA1, MA0 : address selection bits, see Table 1
ACK : acknowledge bit
D7 : channel selection bit, see Table 2
D6 : matrix selection bit, see Table 2
D5, D4, D3 : gain control bits, see Table 3
D2 : fast switching priority bit, see Table 4
D1, D0 : output state control bits, see Table 5
STO : stop condition

Table 1 Address selection

address select pins			address select bits		
S2 pin 17	S1 pin 16	S0 pin 15	MA2	MA1	MA0
L	L	L	*	*	*
L	L	H	0	0	1
L	H	L	0	1	0
L	H	H	0	1	1
H	L	L	1	0	0
H	L	H	1	0	1
H	H	L	1	1	0
H	H	H	1	1	1

Where:

L = input voltage LOW
H = input voltage HIGH
* = non-I²C-bus operation

Table 2 Mode control bits D7, D6

mode	D7	D6	function
0	0	0	channel 2 selected, no matrix
1	0	1	channel 2 selected, matrix active
2	1	0	channel 1 selected
—	1	1	not allowed

DEVELOPMENT DATA

I²C-bus mode (continued)

Table 3 Gain setting (see also Table 9)

D5	D4	D3	A1	A2, A3, A4	B1, B3	B2
0	0	0	1	1	−1	0.45
0	0	1	1	1	1	1
0	1	0	not allowed			
0	1	1	1	1	−1	0.45
1	0	0	2	2	−1	0.45
1	0	1	2	1	1	1
1	1	0	2	2	1	1
1	1	1	2	1	−1	0.45

Matrix equations

The relationship between output and input signals of the matrix is as follows:

$Y = 0.3\ R + 0.59\ G + 0.11\ B$
$R\text{-}Y = 0.7\ R - 0.59\ G - 0.11\ B$
$B\text{-}Y = -0.3\ R - 0.59\ G + 0.89\ B$

Table 4 Priority/fast switching bit D2

D2	fast switching pin 3	mode
0	X	0 to 2, depending on D7, D6
1	0.4 V	2

Where:
X = don't care

Table 5 Output state control bits

D1	D0	pin 9	function
0	X	X	OFF
1	0	L	OFF
1	0	H	ON
1	1	X	ON

Where:
X = don't care

Power-on reset

If the circuit is switched on in the I²C-bus mode, all bits of D0 to D7 are set to zero.

DEVELOPMENT DATA

Timing specifications

I²C-bus load conditions are as follows:
4 kΩ pull-up resistor to + 5 V; 200 pF capacitor to GND.
All values are referred to V_{IH} = 3 V and V_{IL} = 1.5 V.

parameter	symbol	min.	max.	unit
Bus free before start	t_{BUF}	4.7	–	μs
Start condition set-up time	$t_{SU;STA}$	4.7	–	μs
Start condition hold time	$t_{HD;STA}$	4.0	–	μs
SCL and SDA LOW time	t_{LOW}	4.7	–	μs
SCL HIGH time	t_{HIGH}	4.0	–	μs
SCL and SDA rise time	t_r	–	1.0	μs
SCL and SDA fall time	t_f	–	0.3	μs
Data set-up time (write)	$t_{SU;DAT}$	250	–	ns
Data hold time (write)	$t_{HD;DAT}$	1.0	–	μs
Acknowledge set-up time	$t_{SU;ACK}$	–	2	μs
Acknowledge hold time	$t_{HD;ACK}$	0	–	μs
Set-up time for stop condition	$t_{SU;STO}$	4.7	–	μs

Note

Timing $t_{HD;DAT}$ deviates from the I²C-bus specification. After reset has been activated, a delay of 50 μs must occur before transmission may be resumed.

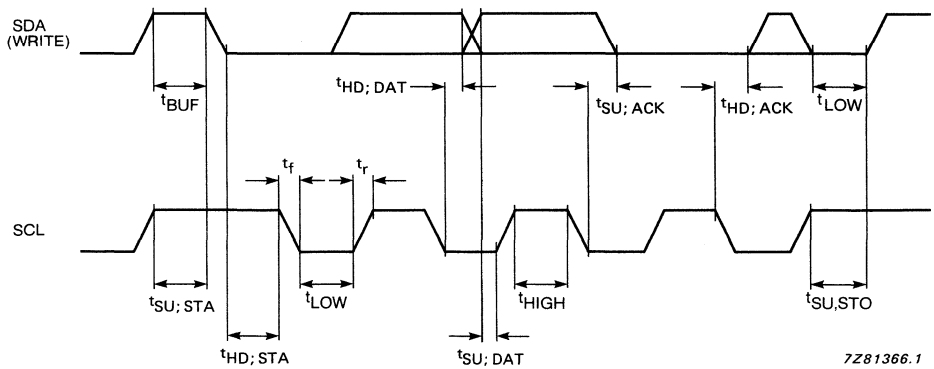


Fig.4 I²C-bus timing diagram.

Non-I²C-bus mode

Table 6 Non-I²C-bus mode (S2 = S1 = S0 = L)

control			mode switched	gain settings			
pin 13	pin 14	pin 1	by FS (pin 3)	A1	A4, A3, A2	B1, B3	B2
L	L	L	2/0	1	1	1	1
L	L	H	2/0	1	2	1	1
L	H	L	2/1	1	1	−1	0.45
L	H	H	2/0	1	1	−1	0.45
H	L	L	2/0	2	1	1	1
H	L	H	2/0	2	2	1	1
H	H	L	2/1	2	1	−1	0.45
H	H	H	2/0	2	1	−1	0.45

Table 7 Fast switching input (pin 3)

FS	mode selected
⩽ 0.4 V	mode 2
1 to 3 V	mode 0 or mode 1 as set by control

Table 8 ON input (pin 9)

ON	function
L	OFF, no output signal, high impedance OFF state
H	function is determined in Table 6

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 18)	V_P	–	14	V
Input voltage range				
SDA (pin 13)	V_I	−0.3	14	V
SCL (pin 14)	V_I	−0.3	14	V
any other pin	V_I	−0.3	V_P + 0.3	V
Maximum output current	I_O	–	20	mA
Operating ambient temperature range	T_{amb}	0	+ 70	°C
Storage temperature range	T_{stg}	−55	+ 125	°C
Maximum junction temperature	T_j	–	+ 125	°C

DEVELOPMENT DATA

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage (pin 18)		V_P	10.8	12.0	13.2	V
Supply current		I_P	–	65	90	mA
RGB/YUV channels						
Absolute gain difference (programmed value)			–	0	10	%
Relative gain difference						
between Y output and the (R-Y) and (B-Y) channel inputs			–	0	10	%
between any two other channels			–	0	5	%
Input current		I_I	–	0.5	1.0	μA
Output impedance						
pin 19		$\|Z_{19-22}\|$	–	7	30	Ω
pin 20		$\|Z_{20-22}\|$	–	7	30	Ω
pin 21		$\|Z_{21-22}\|$	–	7	30	Ω
Bandwidth						
–3 dB	mode 0 or 2	B	–	25	–	MHz
+3 dB	mode 0 or 2	B	–	12	–	MHz
±3 dB	mode 1	B	–	10	–	MHz
Mutual time difference at output	all inputs of one source connected together		–	–	25	ns
Maximum output amplitude of YUV signals (peak-to-peak value)	gain x 1	$V_{O(p-p)}$	2.1	–	–	V
	gain x 2	$V_{O(p-p)}$	4.2	–	–	V
Crosstalk between	note 1					
inputs of same source	f = 5 MHz	α	–	–	–30	dB
different sources		α	–	–	–40	dB
Isolation (OFF state)	f = 10 MHz		50	–	–	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Differential gain at nominal output signals (peak-to-peak value)	R-Y = 1.05 $V_{(p-p)}$		–	–	10	%
	B-Y = 1.33 $V_{(p-p)}$		–	–	10	%
	Y = 0.34 $V_{(p-p)}$		–	–	10	%
Signal-to-noise ratio nominal input	note 2 B = 5 MHz	S/N	50	–	–	dB
Supply voltage ripple rejection	note 3	RR	30	–	–	dB
DC output levels during clamping		V_O	–	5.3	–	V
Synchronization channels						
Gain difference (programmed value)			–	–	10	%
Bandwidth						
–3 dB		B	–	50	–	MHz
+ 3 dB gain x 1		B	–	20	–	MHz
+ 3 dB gain x 2		B	–	13	–	MHz
Input amplitude of sync signal for correct operation of clamp pulse generator (peak-to-peak value)		$V_{I(p-p)}$	0.2	–	2.5	V
Output impedance (pin 23)		$\lvert Z_{23-22}\rvert$	–	20	30	Ω
Maximum undistorted output amplitude (pin 23) (peak-to-peak value)		$V_{O(p-p)}$	2.5	–	–	V
DC output level on top of sync pulse		V_O	1.5	1.9	2.4	V
I²C-bus inputs						
SDA, SCL						
Input voltage HIGH		V_{IH}	3	–	V_P	V
Input voltage LOW		V_{IL}	–0.3	–	1.5	V
Input current HIGH		I_{IH}	–	–	10	μA
Input current LOW		I_{IL}	–	–	10	μA
I²C-bus output						
SDA (open collector)						
Output voltage LOW	I_{OL} = 3 mA	V_{OL}	–	–	0.4	V

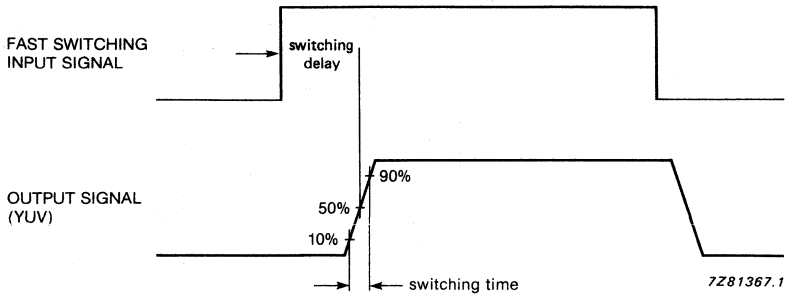
DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Address selection inputs						
S0, S1, S2						
Input voltage HIGH		V_{IH}	3	–	V_P	V
Input voltage LOW		V_{IL}	–0.3	–	0.4	V
Input current HIGH		I_{IH}	–	0	10	μA
Input current LOW		I_{IL}	–50	–10	0	μA
Fast switching input						
Input voltage HIGH		V_{IH}	1	–	3	V
Input voltage LOW		V_{IL}	–0.3	–	0.4	V
Input current HIGH		I_{IH}	–	0	500	μA
Input current LOW		I_{IL}	–100	–	–	μA
Switching time	see Fig.5	t	–	10	–	ns
Switching delay	see Fig.5	t_d	–	20	–	ns
Select input						
Input voltage HIGH		V_{IH}	3	–	V_P	V
Input voltage LOW		V_{IL}	–0.3	–	0.4	V
Input current HIGH		I_{IH}	–	0	10	μA
Input current LOW		I_{IL}	–50	–10	0	μA
ON input						
Input voltage HIGH		V_{IH}	3	–	V_P	V
Input voltage LOW		V_{IL}	–0.3	–	1.5	V
Input current HIGH		I_{IH}	–	–	10	μA
Input current LOW		I_{IL}	–	–	10	μA

Notes to the characteristics

1. Crosstalk is defined as the unwanted data transfer from an output, driven at nominal level, to other inputs and outputs on the IC and is expressed as a ratio in dBs.
2. Signal-to-noise ratio = $20 \log \frac{V_{O(p\text{-}p)}}{V_O \text{ noise (RMS) } B = 5 \text{ MHz}}$
3. Supply voltage ripple rejection = $20 \log \frac{V_{RR \text{ supply}}}{V_{RR \text{ on the output}}}$



Input = 0 V (input 1; Mode 2)
Input = 0.75 V (RGB; Mode 1)

Fig.5 Fast switching signal diagram.

DEVELOPMENT DATA

APPLICATION INFORMATION

Table 9 Application information

input 1	input 2	output	mode	G2	G1	G0
Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.3 V		Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.6 V	2	1	1	1
	R = 0.75 V G = 0.75 V B = 0.75 V S = 0.3 V		1	1	1	1
Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.3 V		Y = 0.68 V U = −2.66 V V = −2.10 V S = 0.6 V	2	1	0	0
	R = 0.75 V G = 0.75 V B = 0.75 V S = 0.3 V		1	1	0	0
Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.3 V		Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.6 V	2	1	0	1
	Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.3 V		0	1	0	1
Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.3 V		Y = 0.68 V U = −2.66 V V = −2.10 V S = 0.6 V	2	1	1	0
	Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.3 V		0	1	1	0

APPLICATION INFORMATION (continued)

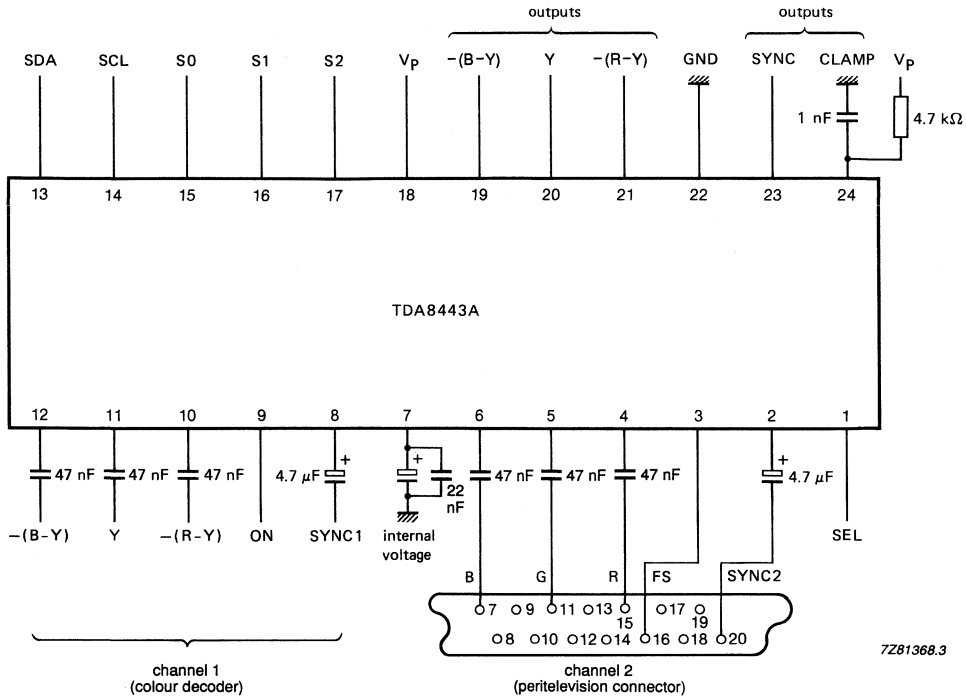


Fig.6 Application diagram (example).

DEVELOPMENT DATA

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

OCTUPLE 6-BIT DAC WITH I²C-BUS

GENERAL DESCRIPTION

The TDA8444 comprises eight digital-to-analogue converters (DACs) each controlled via the two-wire I²C-bus. The DACs are individually programmed using a 6-bit word to select an output from one of 64 voltage steps. The maximum output voltage of all DACs is set by the input V_{max} and the resolution is approximately $V_{max}/64$. At power-on all DAC outputs are set to their lowest value. The I²C-bus slave receiver has a 7-bit address of which 3 bits are programmable via pins A0, A1 and A2.

Features

- Eight discrete DACs
- I²C-bus slave receiver
- 16-pin DIL package

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	10.8	12.0	13.2	V
Supply current	no loads; $V_{max} = V_P$; all data = 00	I_{CC}	8	12	15	mA
Total power dissipation	no loads; $V_{max} = V_P$; all data = 00	P_{tot}	–	150	–	mW
Effective range of V_{max} input	V_P = 12 V	V_{max}	1	–	10.5	V
DAC output voltage range		V_O	0.1	–	V_P–0.5	V
Step value of 1 LSB	$V_{max} = V_P$; I_O = –2 mA	V_{LSB}	70	160	250	mV

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

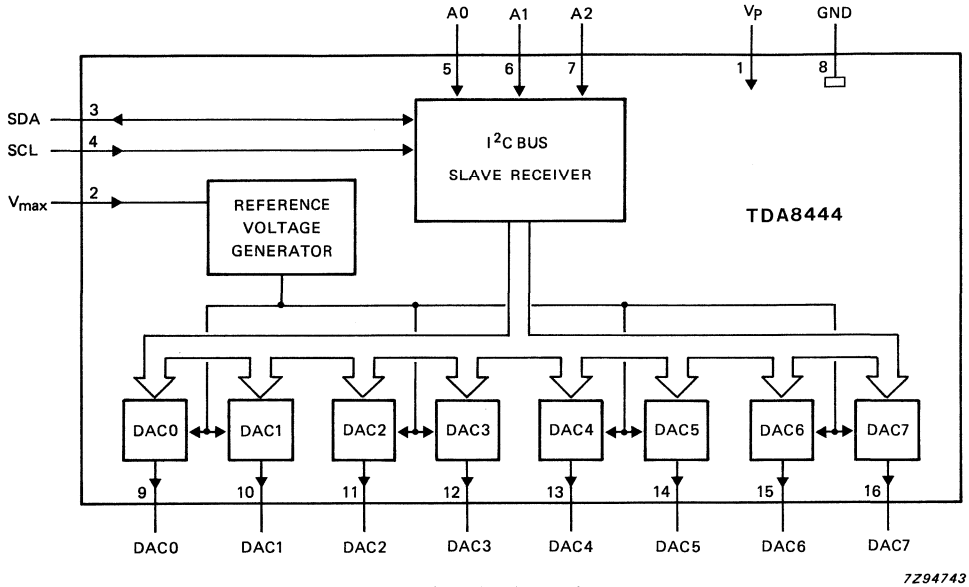


Fig. 1 Block diagram.

PINNING

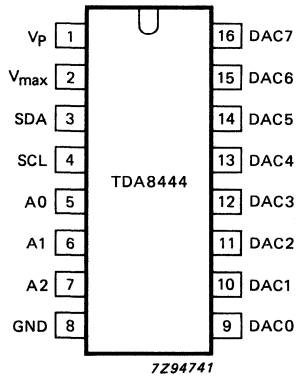


Fig. 2 Pinning diagram.

1	V_P	positive supply voltage
2	V_{max}	control input for DAC maximum output voltage
3	SDA	I^2C-bus serial data input/output
4	SCL	I^2C-bus serial data clock
5	A0	programmable address bits for I^2C-bus slave receiver
6	A1	
7	A2	
8	GND	ground
9-16	DAC0-7	analogue voltage outputs

FUNCTIONAL DESCRIPTION

I²C-bus

The TDA8444 I²C-bus interface is a receive-only slave. Data is accepted from the I²C-bus in the following format:

S	0 1 0 0 A2 A1 A0 0	A	I3 I2 I1 I0 SD SC SB SA	A	X X D5 D4 D3 D2 D1 D0	A	P
	← address byte →		← instruction byte →		← first data byte →		

Where:

S	= start condition	A2, A1, A0	= programmable address bits
P	= stop condition	I3, I2, I1, I0	= instruction bits
A	= acknowledge	SD, SC, SB, SA	= subaddress bits
X	= don't care	D5, D4, D3, D2, D1, D0	= data bits

Fig. 3 Data format.

Address byte

Valid addresses are 40, 42, 44, 46, 48, 4A, 4C, 4E (hexadec), depending on the programming of bits A2, A1 and A0. With these addresses, up to eight TDA8444 ICs can be operated independently from one I²C-bus. No other addresses are acknowledged by the TDA8444.

Instruction and data bytes

Valid instructions are 00 to 0F and F0 to FF (hexadec); the TDA8444 will not respond to other instruction values.

Instructions 00 to 0F cause auto-incrementing of the subaddress (bits SD to SA) when more than one data byte is sent within one transmission. With auto-incrementing, the first data byte is written into the DAC addressed by bits SD to SA and then the subaddress is automatically incremented by one position for the next data byte in the series.

Auto-incrementation does not occur with instructions F0 to FF. Other than auto-incrementation there is no difference between instructions 00 to 0F and F0 to FF. When only one data byte per transmission is present, the DAC addressed by the subaddress will always receive the data.

Valid subaddresses (bits SD to SA) are 0 to 7 (hexadec) relating numerically to DAC0 to DAC7. When the auto-incrementing function is used, the subaddress will sequence through all possible values (0 to F, 0 to F, etc.).

I²C-bus

Input SCL (pin 3) and input/output SDA (pin 4) conform to I²C-bus specifications.* Pins 3 and 4 are protected against positive voltage pulses by internal zener diodes connected to the ground plane and therefore the normal bus line voltage should not exceed 5.5 V.

The address inputs A0, A1, A2 are programmed by a connection to GND for An = 0 or to V_P for An = 1. If the inputs are left floating, An = 1 will result.

FUNCTIONAL DESCRIPTION (continued)

Input V_{max}

Input V_{max} (pin 2) provides a means of compressing the output voltage swing of the DACs. The maximum DAC output voltage is restricted to approximately V_{max} while the 6-bit resolution is maintained, so giving a finer voltage resolution of smaller output swings.

Digital-to-analogue converters

Each DAC comprises a 6-bit data latch, current switches and an output driver. Current sources with values weighted by 2^0 up to 2^5 are switched according to the data input so that the sum of the selected currents gives the required analogue voltage from the output driver. The range of the output voltage is approximately 0.5 to 10.5 V when $V_{max} = V_P$.

The DAC outputs are protected against short-circuits to V_P and GND.

To avoid the possibility of oscillations, capacitive loading at the DAC outputs should not exceed 2 nF.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		$V_P = V_1$	−0.5	18	V
Supply current (source)		$I_p = I_1$	−	−10	mA
		$I_P = I_I$	−	40	mA
I^2C-bus line voltage		$V_{3,4}$	−0.5	5.9	V
Input voltage		V_I	−0.5	$V_P + 0.5$	V
Output voltage		V_O	−0.5	$V_P + 0.5$	V
Maximum current on any pin (except pins 1 and 8)		$\pm I_{max}$	−	10	mA
Total power dissipation		P_{tot}	−	500	mW
Operating ambient temperature range		T_{amb}	−20	+ 70	°C
Storage temperature range		T_{stg}	−65	+ 150	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 75 K/W

Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

CHARACTERISTICS

All voltages are with respect to GND; T_{amb} = 25 °C; V_P = 12 V unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	10.8	12.0	13.2	V
Voltage level for power-on reset		V_1	1	–	4.8	V
Supply current	no loads; $V_{max} = V_P$; all data = 00	$I_P = I_1$	8	12	15	mA
Total power dissipation	no loads; $V_{max} = V_P$; all data = 00	P_{tot}	–	150	–	mW
Effective range of V_{max} input (pin 2)	V_P = 12 V	$V_{max} = V_2$	1.0	–	10.5	V
Pin 2 current	V_2 = 1 V	I_2	–	–	−10	μA
	$V_2 = V_P$	I_2	–	–	10	μA
SDA, SCL inputs (pins 3 and 4)						
Input voltage range		V_I	0	–	5.5	V
Input voltage LOW		V_{IL}	–	–	1.5	V
Input voltage HIGH		V_{IH}	3.0	–	–	V
Input current LOW	$V_{3;4}$ = 0.3 V	I_{IL}	–	–	−10	μA
Input current HIGH	$V_{3;4}$ = 6 V	I_{IH}	–	–	±10	μA
SDA output (pin 3)						
Output voltage LOW	I_3 = 3 mA	V_{OL}	–	–	0.4	V
Sink current		I_O	3	8	–	mA
Address inputs (pins 5 to 7)						
Input voltage range		V_I	0	–	V_P	V
Input voltage LOW		V_{IL}	–	–	1	V
Input voltage HIGH		V_{IH}	2.1	–	–	V
Input current LOW		I_{IL}	–	−7	−12	μA
Input current HIGH		I_{IH}	–	–	1	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
DAC outputs (pins 9 to 16)						
Output voltage range		V_O	0.1	–	V_P–0.5	V
Minimum output voltage	data = 00; I_O = –2 mA	V_{Omin}	0.1	0.4	0.8	V
Maximum output voltage	data = 3F; I_O = –2 mA					
at $V_{max} = V_P$		V_{Omax}	10	10.5	11.5	V
at $1 < V_{max} < 10.5$ V		V_{Omax}		see note		V
Output sink current	V = V_P; data = 1F	I_O	2	8	15	mA
Output source current	V = 0V; data = 1F	I_O	–2	–	–6	mA
Output impedance	data = 1F; $-2 < I_O < +2$ mA	Z_O	–	4	50	Ω
Step value of 1 LSB	$V_{max} = V_P$; I_O = –2 mA	V_{LSB}	70	160	250	mV
Deviation from linearity	I_O = –2 mA; N ≠ 32		0	–	50	mV
Deviation from linearity	I_O = –2 mA; N = 32		0	–	70	mV

Note to the characteristics

$V_O = 0.95\ V_{max} + V_{Omin}$.

APPLICATION INFORMATION

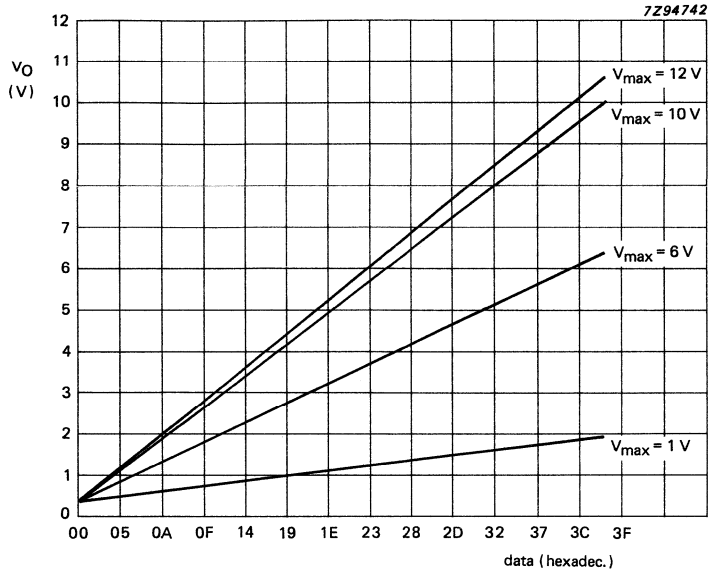


Fig. 4 Graph showing output voltage as a function of the input data value for V_{max} values of 1, 6, 10 and 12 V; V_P = 12 V.

P²CCD DELAY LINE AND MATRIX

GENERAL DESCRIPTION

The TDA8451 is an integrated P²CCD (Profiled Peristaltic Charge Coupled Device) delay line and matrix which has been designed to be used in conjunction with various colour decoder ICs (e.g. TDA8461, TDA8390). The device incorporates two comb filters with a delay length of 64 μs on the base-band frequencies and clock drivers for the delay lines which are driven from an internal voltage controlled oscillator (VCO) locked to the 2 x f_{sc} signal. The 2 x f_{sc} signal is obtained from the decoder IC.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage						
analogue (pin 3)		$V_{P(a)}$	10.8	12.0	13.2	V
digital (pin 16)		$V_{P(d)}$	10.8	12.0	13.2	V
Supply current						
analogue (pin 3)		$I_{P(a)}$	4	7	10	mA
digital (pin 16)		$I_{P(d)}$	10	25	40	mA

PACKAGE OUTLINE

16-lead DIL; plastic with internal heat spreader (SOT38WE2).

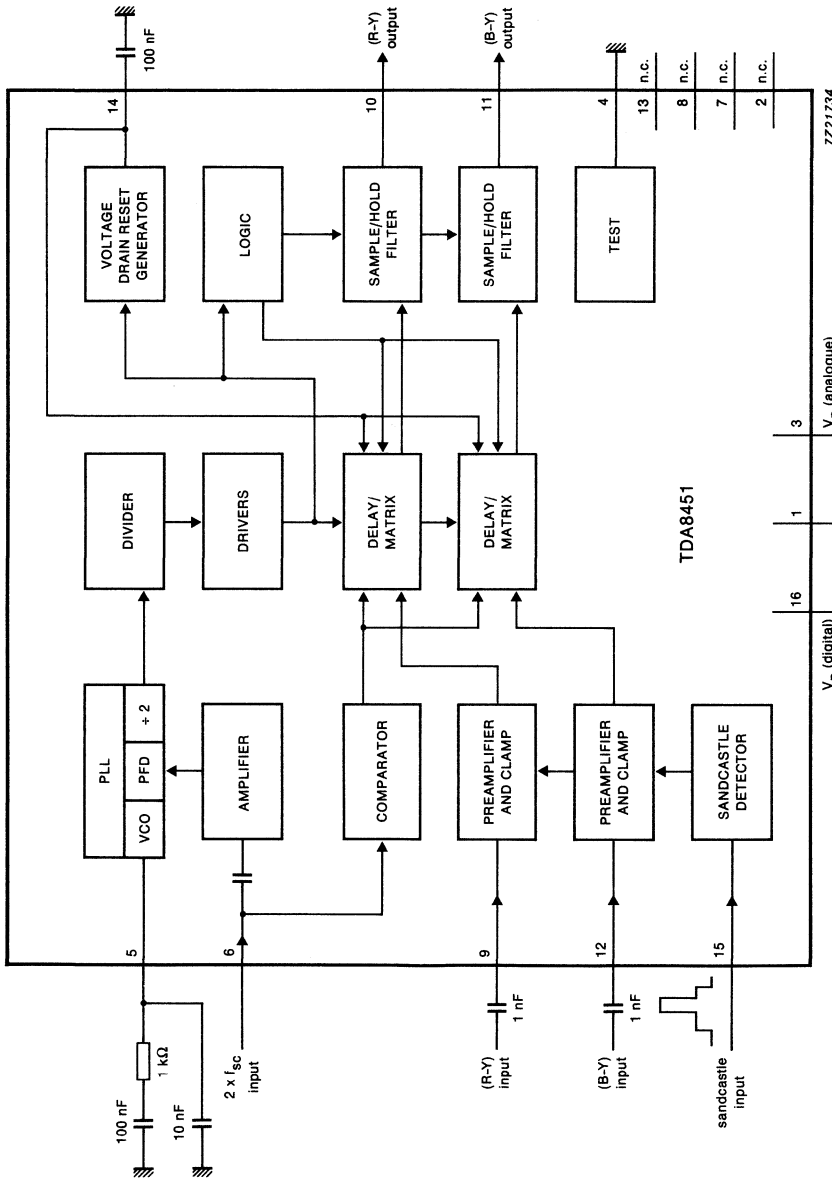


Fig.1 Block diagram.

PINNING

1. Ground
2. Not connected
3. Supply voltage input (analogue)
4. Test pin (grounded for normal operation)
5. PLL filter
6. Input 2 x f_{SC} plus PAL/NTSC mode signal
7. Not connected
8. Not connected
9. (R-Y) input
10. (R-Y) output
11. (B-Y) output
12. (B-Y) input
13. Not connected
14. Voltage drain reset generator decoupling
15. Sandcastle input
16. Supply voltage input (digital)

FUNCTIONAL DESCRIPTION

When the (R-Y) and (B-Y) signals have been demodulated in the decoder, the resultant signals are applied to the comb-filter delay lines via pins 9 and 12. The delay lines are only active when a PAL or SECAM signal is received. When NTSC signals are received the delayed signal is suppressed so that the colour decoded signals are fed directly to the output.

The decoder (e.g. TDA8461) establishes whether or not the received signal is NTSC. This signal is then applied to the P^2CCD delay lines via the DC level of the $2 \times f_{SC}$ signal at pin 6.

The delay lines are driven by the internal clock drivers. The outputs from the delay lines are applied to the sample-and-hold low-pass filter output stages which are used to reduce the clock signals.

The reference for the PLL is obtained from the decoder IC which derives the $2 \times f_{SC}$ signal from its reference oscillator (the amplitude of this signal may be small, min. 200 mV(p-p)). The VCO operates at $4 \times f_{SC}$ and the delay lines are 4 phase clocked at f_{SC}.

The P^2CCD delay line and matrix requires a supply voltage of 12 V. The output stages require a higher voltage (approximately 14 V). This voltage is generated internally with a decoupling capacitor connected to pin 14. A circuit for the TDA8451 together with PAL decoder (TDA8390) is illustrated in Fig.2.

A circuit for the TDA8451 together with PAL/NTSC decoder (TDA8461) and the SECAM decoder (TDA8490) is illustrated in Fig.3. The TDA8490 can also be used in combination with the TDA8390.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (analogue)		$V_{P(a)}$	–	13.2	V
Supply voltage (digital)		$V_{P(d)}$	–	13.2	V
Total power dissipation		P_{tot}	–	1.45	W
Operating ambient temperature range		T_{amb}	–25	+70	°C
Storage temperature range		T_{stg}	–65	+150	°C

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j\text{-}a}$ 55 K/W

DEVELOPMENT DATA

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage (pin 3) analogue		$V_{P(a)}$	10.8	12.0	13.2	V
Supply current (pin 3) analogue		$I_{P(a)}$	4	7	10	mA
Supply voltage (pin 3) ripple rejection at 100 mVeff	f = 100 Hz	SVRR	–	10	–	dB
Supply voltage (pin 16) digital		$V_{P(d)}$	10.8	12.0	13.2	V
Supply current (pin 16) digital		$I_{P(d)}$	10	25	40	mA
Supply voltage (pin 16) ripple rejection at 100 mVeff	f = 100 Hz	SVRR	–	20	–	dB
Total power dissipation		P_{tot}	–	0.4	0.66	W
Inputs for demodulated colour difference signals (pins 9 and 12) AC coupled and clamped by sandcastle pulse						
Input signal PAL mode (peak-to-peak value)		$V_{I(p-p)}$	–	0.8	1.6	V
Input signal NTSC or SECAM (peak-to-peak value)		$V_{I(p-p)}$	–	1.6	2.0	V
Input current (outside clamping time)		I_I	–	–	0.1	μA
Input capacitance		C_I	–	5	–	pF
Sandcastle input (pin 15)						
Input resistance		R_{15}	1000	–	–	kΩ
Detection level		V_{15}	6.0	7.0	7.5	V
Oscillator signal input and mode select (pin 6)						
Input signal (peak-to-peak value)	2 x f_{sc}	$V_{6(p-p)}$	200	–	–	mV
Input capacitance		C_6	–	6	–	pF
Input voltage at which the delayed signal is suppressed in the comb-filter (NTSC)		V_6	6.7	–	–	V
Input voltage at which the delayed and direct signals are matrixed (PAL or SECAM)		V_6	0	–	5.3	V

parameter	conditions	symbol	min.	typ.	max.	unit
Input voltage	$I_6 = 0$	V_6	–	0	–	V
Input current	$V_6 = 12$ V	I_6	–	1	5	μA
CD signal output (pins 10 and 11)						
Output signals where input signal is PAL at 0.8 V (peak-to-peak value)		$V_{10;\,11(p\text{-}p)}$	0.63	0.8	1.01	V
Output signals (where input signal is NTSC and SECAM at 1.6 V (peak-to-peak value)	note 1	$V_{10;\,11(p\text{-}p)}$	0.63	0.8	1.01	V
Output resistance		R_O	300	500	800	Ω
Internal current load of CD outputs		$I_{10;\,11}$	0.4	–	1.5	mA
DC output level		$V_{10;\,11}$	4	–	8	V
Rest clock signals (RMS value)	note 2					
at 4.4 MHz		$V_{10\text{-}11(rms)}$	–	–	12	mV
at 8.8 MHz		$V_{10\text{-}11(rms)}$	–	–	6	mV
at 17.7 MHz		$V_{10\text{-}11(rms)}$	–	–	6	mV
Signal-to-noise ratio	note 3	S/N	60	65	–	dB
Linearity of output signals (peak-to-peak value)	note 4					
(R-Y); pin 9 to pin 10 PAL	$V_I = 0.74$ V	α	0.95	–	–	V
(R-Y); pin 9 to pin 10 SECAM	$V_I = 1.48$ V	α	0.92	–	–	V
(R-Y); pin 9 to pin 10 NTSC	$V_I = 1.48$ V	α	0.90	–	–	V
(B-Y); pin 12 to pin 11 PAL	$V_I = 0.96$ V	α	0.95	–	–	V
(B-Y); pin 12 to pin 11 SECAM	$V_I = 1.92$ V	α	0.92	–	–	V
(B-Y); pin 12 to pin 11 NTSC	$V_I = 1.92$ V	α	0.90	–	–	V
Frequency response	at –3 dB	Δf	1.0	1.3	–	MHz
Difference in amplitude between delayed and undelayed signal			–	–	1.5	%
Difference in amplitude of the two output signals for equal input signals			–	–	5	%
Additional signal delay time at 8.87 MHz reference input		t_d	650	670	690	ns
at 7.16 MHz reference input		t_d	775	800	825	ns

DEVELOPMENT DATA

Notes to the characteristics

1. During NTSC, the delayed channel is switched off (switching information fed from the decoder) thereby halving the amplification in comparison with other signal conditions.
   During SECAM, the input signal is only available during one of two sequential lines thereby halving the output signal in comparison with the PAL signal. This can be compensated for if the NTSC decoder (e.g. TDA8461) and the SECAM decoder (TDA8490) supply colour difference signals of double amplitude (as compared to PAL) to the TDA8451.
2. The sandcastle input is LOW. The rest clock signals are measured with an FET probe (3.5 pF in parallel with a 1 MHz resistor) connected directly to pin 1 and pin 10 or pin 1 and pin 11.
3. The signal-to-noise ratio is calculated by:

   $\frac{V_{O(p\text{-}p)}}{V_{noise(rms)}\ (0 - 1\ MHz)}$ at an input voltage of 0.8 V(p-p), 0 dB gain.
4. The linearity is defined as the amplification of the given input voltage swing divided by the amplification when the input voltage swing is decreased to 70%.

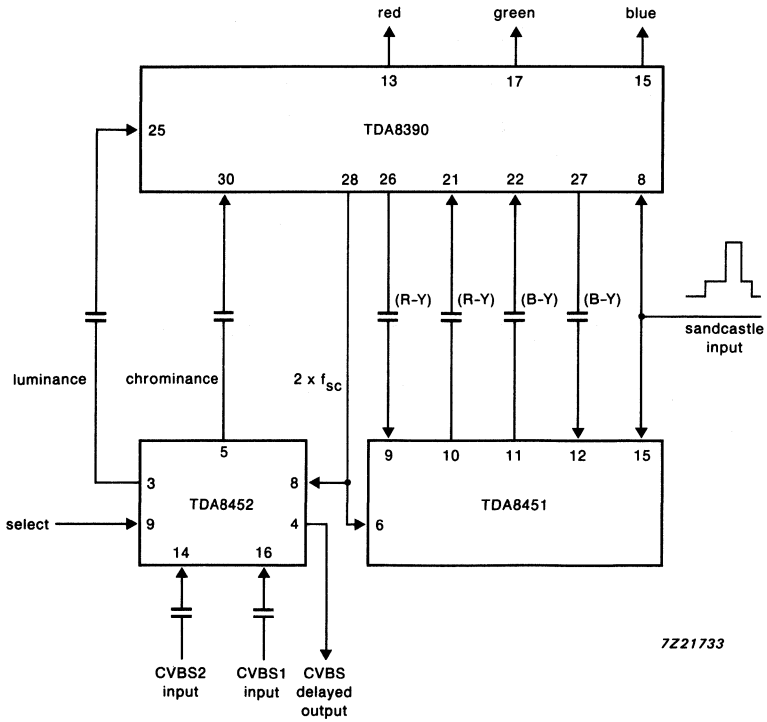


Fig.2 PAL decoder configuration.

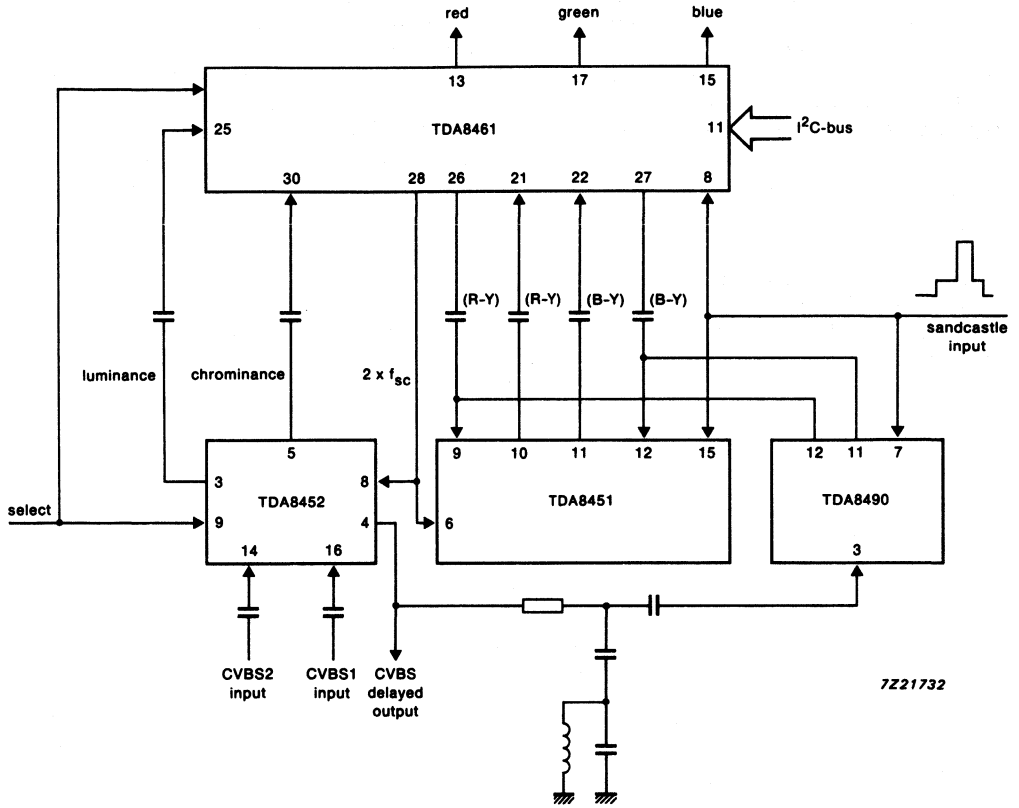


Fig.3 PAL-NTSC-SECAM decoder configuration.

P²CCD FILTER COMBINATION FOR COLOUR DECODERS

GENERAL DESCRIPTION

The TDA8452 is an integrated P²CCD (Profiled Peristaltic Charge Coupled Device) filter combination which has been designed to be used in conjunction with various colour decoder ICs (e.g. TDA8461, TDA8390). The device incorporates a video input switch, a composite video (CVBS) delay line, a luminance delay with chrominance trap, a chrominance band-pass filter and clock drivers for the filters which are driven from an internal voltage controlled oscillator (VCO) locked to the $2 \times f_{sc}$ signal. The $2 \times f_{sc}$ signal is obtained from the decoder IC.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage						
analogue (pin 2)		$V_{p(a)}$	10.8	12.0	13.2	V
digital (pin 12)		$V_{p(d)}$	10.8	12.0	13.2	V
Supply current						
analogue (pin 2)		$I_{p(a)}$	10	18	25	mA
digital (pin 12)		$I_{p(d)}$	20	45	70	mA
CVBS inputs (pins 14 and 16)						
Input signal (peak-to-peak value)		$V_{I(p-p)}$	–	0.7	1.0	V
Luminance output (pin 3)						
output signal (peak-to-peak value)		$V_{3(p-p)}$	–	0.45	–	V
Luminance signal delay						
at 8.87 MHz reference input		t_d	2060	2090	2120	ns
at 7.16 MHz reference input		t_d	2550	2580	2610	ns
Bandwidth	at –3 dB	B	3.7	3.8	–	MHz
Chrominance output (pin 5)						
output signal (peak-to-peak value)		$V_{5(p-p)}$	0.33	0.46	0.66	V
Chrominance filter delay						
at 8.87 MHz reference input		t_d	990	1020	1050	ns
at 7.16 MHz reference input		t_d	1220	1250	1280	ns
Bandwidth (Fig.3)	at –3 dB	B	–	1.1	–	MHz
CVBS output (pin 4)						
output signal (peak-to-peak value)		$V_{4(p-p)}$	–	1.0	–	V
CVBS signal delay						
at 8.87 MHz reference input		t_d	820	850	880	ns
at 7.16 MHz reference input		t_d	1010	1040	1070	ns
Bandwidth (Fig.4)	at –3 dB	B	5.5	6.5	–	MHz
Output resistance		R_O	300	500	800	Ω
Oscillator input signal						
(peak-to-peak value)		$V_{8(p-p)}$	–	> 200	–	mV

PACKAGE OUTLINE

16-lead DIL; plastic with internal heat spreader (SOT38WE2).

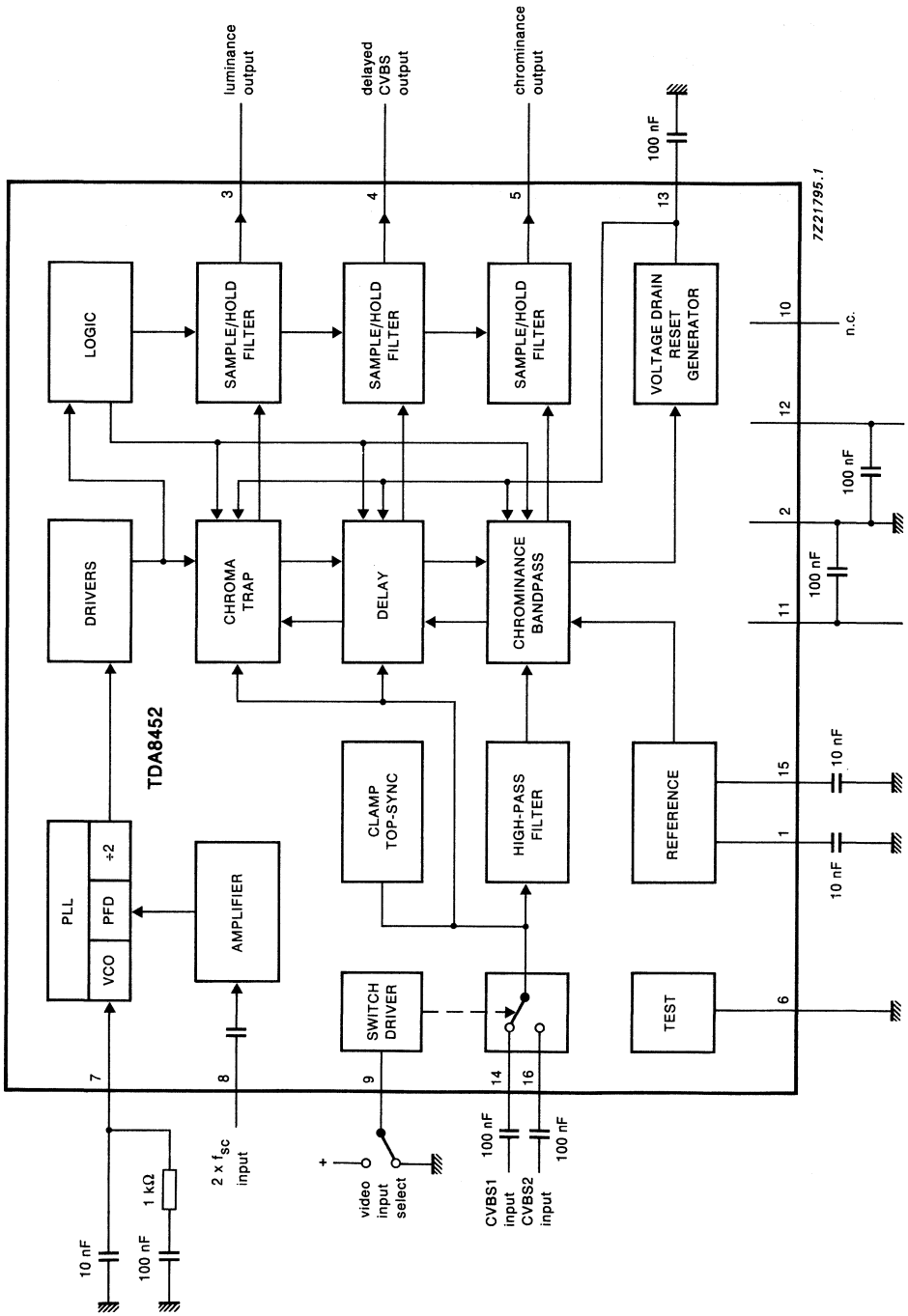


Fig.1 Block diagram.

PINNING

1 Reference decoupling
2 Analogue supply voltage input
3 Luminance output
4 Delayed CVBS output
5 Chrominance output
6 Test pin (to be grounded for normal operation)
7 PLL filter
8 $2 \times f_{sc}$ input
9 CVBS input select
10 Not connected
11 Ground
12 Digital supply voltage input
13 Voltage drain reset generator decoupling
14 CVBS1 input
15 Reference decoupling
16 CVBS2 input

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

The composite video signal (CVBS1 and CVBS2) is applied to pin 14 and/or pin 16. The signal is then routed through three separate paths before being applied to the sample-and-hold filter output stages as follows:

- via a CVBS delay line, the output signal can be used to drive the sync separation circuit, teletext and SECAM decoders etc.
- via a luminance delay line with chrominance trap.
- via a chrominance bandpass filter.

The outputs from the delay lines are applied to the sample-and-hold low-pass filter output stages which are used to reduce the clock signals.
The reference for the PLL is obtained from the decoder IC which derives the 2 x f_{sc} signal from its reference oscillator (the amplitude of this signal may be small, min. 200 mV(p-p)). The VCO operates at 4 x f_{sc} and the delay lines are 4 phase clocked at f_{sc}.
The P^2CCD filter combination requires a supply voltage of 12 V. The output stages require a higher voltage (approximately 14 V). This voltage is generated internally with a decoupling capacitor connected to pin 13. A circuit for the TDA8452 together with PAL decoder (TDA8390) is illustrated in Fig.5.
A circuit for the TDA8452 together with PAL/NTSC decoder (TDA8461) and the SECAM decoder (TDA8490) is illustrated in Fig.6. The TDA8490 can also be used in combination with the TDA8390.
Figure 9 illustrates the luminance and CVBS channel response on T and 2T pulse.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (analogue)		$V_p(a)$	–	13.2	V
Supply voltage (digital)		$V_p(d)$	–	13.2	V
Total power dissipation		P_{tot}	–	1.45	W
Operating ambient temperature range		T_{amb}	−25	+70	°C
Storage temperature range		T_{stg}	−65	+150	°C

THERMAL RESISTANCE

From junction to ambient (in free air)	$R_{th\ j\text{-}a}$		55	K/W

DEVELOPMENT DATA

CHARACTERISTICS

V_p = 12 V; T_{amb} = 25 °C unless otherwise specified (note 1).

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage (pin 2) analogue		$V_p(a)$	10.8	12.0	13.2	V
Supply current (pin 2) analogue		$I_p(a)$	10	18	25	mA
Supply voltage (pin 2) ripple rejection at 100 mVeff	f = 100 Hz	SVRR	–	7	–	dB
Supply voltage (pin 12) digital		$V_p(d)$	10.8	12.0	13.2	V
Supply current (pin 12) digital		$I_p(d)$	20	45	70	mA
Supply voltage (pin 12) ripple rejection at 100 mVeff	f = 100 Hz	SVRR	–	7	–	dB
Total power dissipation		P_{tot}	–	0.76	1.25	W
Composite video inputs (pins 14 and 16)						
AC coupled and clamped to top sync						
Input signal (peak-to-peak value)		$V_{I(p-p)}$	–	0.7	1.0	V
Input current (non-selected input)		I_I	–	–	0.1	μA
Input current during non-clamping period of selected input		I_I	2.0	3.5	5.0	μA
Input capacitance		C_I	–	5	–	pF
Crosstalk between selected/non-selected channels	R_I = 75 Ω					
at f_{sc} = 1.5 MHz		α	60	65	–	dB
at f_{sc} = 5.0 MHz		α	–	50	–	dB
Video switch control (pin 9)						
Video input (pin 14)		V_9	0	–	1.5	V
Video input (pin 16)		V_9	4	–	V_P	V
Oscillator input signal (pin 8)						
Input signal (peak-to-peak value)	2 x f_{sc}	$V_{8(p-p)}$	200	–	–	mV
Input capacitance		C_I	–	6	–	pF
Input resistance		R_I	–	80	–	kΩ

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Luminance signal output (pin 3)						
Output signal (input signal = 0.7 V peak-to-peak value)		$V_{3(p-p)}$	–	0.45	–	V
Black-to-white output signal (CVBS input signal = 0.7 V peak-to-peak value)		$V_{3(p-p)}$	0.23	0.32	0.46	V
Output resistance		R_0	300	500	800	Ω
Output level for top sync		V_3	3.0	–	7.0	V
Luminance output internal load		I_3	0.4	–	1.5	mA
Rest clock signals (RMS value)	note 2					
at 4.43 MHz		$V_{3(rms)}$	–	–	1	mV
at 8.87 MHz		$V_{3(rms)}$	–	–	4	mV
at 17.73 MHz		$V_{3(rms)}$	–	–	12	mV
Signal-to-noise ratio	note 3	S/N	60	65	–	dB
Linearity black-to-white (CVBS input signal = 0.7 V peak-to-peak value)	note 4	$L_{3(p-p)}$	0.95	–	–	
Linearity black-to-white (CVBS input signal = 1.0 V peak-to-peak value)	note 4	$L_{3(p-p)}$	0.94	–	–	
Bandwidth	at −3 dB	B	3.7	3.8	–	MHz
Frequency response with regard to 0 MHz (Fig.2)						
at 2.2 MHz		Δf	−1.0	0.5	2.0	dB
at 3.0 MHz		Δf	−0.5	1.0	2.5	dB
at 3.8 MHz		Δf	−4.0	−2.5	−1.0	dB
at 4.26 MHz		Δf	−18	−15	−12	dB
at 4.43 MHz		Δf	–	−25	−20	dB
at 4.64 MHz		Δf	−18	−15	−12	dB
at 5.5 MHz		Δf	−5.0	−2.5	0	dB
T and 2T response (Fig.7) (CVBS input signal = 0.6 V peak-to-peak value)						
Luminance signal delay						
at 8.87 MHz reference input		t_d	2060	2090	2120	ns
at 7.16 MHz reference input		t_d	2550	2580	2610	ns

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Chrominance signal output (pin 5)						
Output signal (chrominance input signal = 0.465 V peak-to-peak value)		$V_{5(p-p)}$	0.33	0.465	0.66	V
Output resistance		R_0	300	500	800	Ω
DC output level		V_5	3.0	–	7.5	V
Internal load of chrominance output		I_5	0.4	–	1.5	mA
Rest clock signals (RMS value)	note 2					
at 4.43 MHz		$V_{5(rms)}$	–	–	0.2	mV
at 8.87 MHz		$V_{5(rms)}$	–	–	5	mV
at 17.73 MHz		$V_{5(rms)}$	–	–	12	mV
Signal-to-noise ratio	note 3	S/N	60	65	*	dB
Linearity of output signals	note 4					
input = 0.45 V (peak-to-peak value)		$L_{5(p-p)}$	–	0.97	–	
input = 0.65 V (peak-to-peak value)		$L_{5(p-p)}$	–	0.95	–	
Bandwidth (Fig.3)	at –3 dB	B	–	1.1	–	MHz
Frequency response with regard to the top at 4.43 MHz (Fig.3)						
at 0.9 MHz		Δf	–23	–20	–17	dB
at 1.9 MHz		Δf	–40	–35	–30	dB
at 2.5 MHz		Δf	–40	–35	–30	dB
at 3.0 MHz		Δf	–24	–20	–16	dB
at 3.8 MHz		Δf	–3.5	–2.5	–1.5	dB
at 4.93 MHz		Δf	–4.0	–3.0	–2.0	dB
at 5.6 MHz		Δf	–24	–20	–16	dB
Chrominance filter delay						
at 8.87 MHz reference input		t_d	990	1020	1050	ns
at 7.16 MHz reference input		t_d	1220	1250	1280	ns
Delayed signal output (pin 4)						
Output signal (input signal = 0.7 V peak-to-peak value)		$V_{4(p-p)}$	–	1.0	–	V
Black-to-white output signal (CVBS input signal = 0.7 V peak-to-peak value)		$V_{4(p-p)}$	0.49	0.70	0.98	V
Output resistance		R_0	300	500	800	Ω
Internal load of delayed output		I_4	0.4	–	1.5	mA

* Value to be fixed.

parameter	conditions	symbol	min.	typ.	max.	unit
Output sync pulse (input sync pulse = 210 mV peak-to-peak value)		$V_{4(p-p)}$	210	–	–	mV
Output level for top sync		V_4	2.5	–	6.5	V
Rest clock signals (RMS value)	note 4					
at 4.43 MHz		$V_{4(rms)}$	–	–	1	mV
at 8.87 MHz		$V_{4(rms)}$	–	–	5	mV
at 17.73 MHz		$V_{4(rms)}$	–	–	12	mV
Signal-to-noise ratio		S/N	65	70	–	dB
Linearity black to white (CVBS input signal = 0.7 V peak-to-peak value)	note 3	$L_{4(p-p)}$	0.95	–	–	
Linearity black to white (CVBS input signal = 1.0 V peak-to-peak value)	note 3	$L_{4(p-p)}$	0.94	–	–	
Bandwidth (Fig.4)	at −3 dB	B	5.5	6.5	–	MHz
Frequency response with regard to 2.2 MHz (Fig.4)						
at 0.0 MHz		Δf	−2.5	−1.5	−0.5	dB
at 0.9 MHz		Δf	−2	−1	−0	dB
at 3.1 MHz		Δf	0	1.0	1.5	dB
at 5.5 MHz		Δf	−3	−1	+ 0.5	dB
T and 2T response is given in Fig.8 (CVBS input signal = 0.6 V peak-to-peak value)						
CVBS signal delay						
at 8.87 MHz reference input		t_d	820	850	880	ns
at 7.16 MHz reference input		t_d	1010	1040	1070	ns

DEVELOPMENT DATA

Notes to the characteristics

1. Unless otherwise specified all figures are related to a CVBS input signal of 0.7 V (peak-to-peak value); 100% contrast; 75% saturation.
   In this condition the input signal is formed by the following components:
   210 mV(p-p) sync pulse
   490 mV(p-p) black-to-white
   465 mV(p-p) chrominance
2. The sandcastle input is LOW. The rest clock signals are measured with an FET probe (3.5 pF in parallel with a 1 MHz resistor) connected directly to pins 1 and 3, pins 1 and 4 or pins 1 and 5.
3. The signal-to-noise ratio is specified as nominal $V_{out(p-p)}/V_{noise(rms)}$ (0-5 MHz) at a CVBS input signal specified in note 1.
4. The linearity is defined as the amplification at the given input voltage swing, divided by the amplification when the input voltage swing is decreased to 70%.

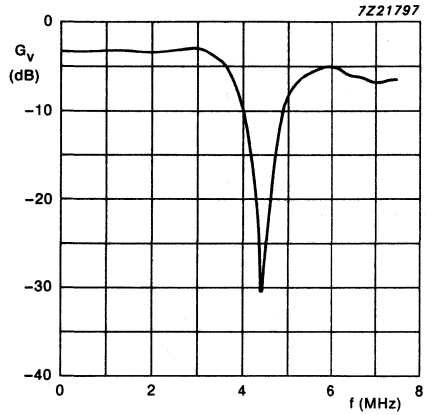


Fig.2 Frequency response of luminance signal.

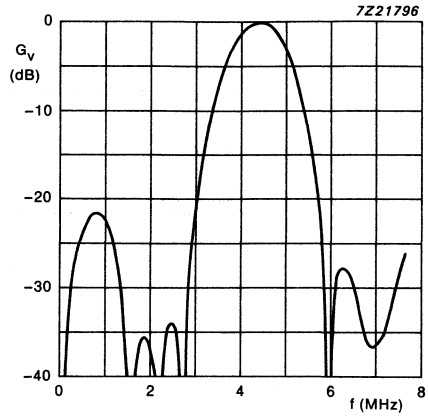


Fig.3 Frequency response of chrominance signal.

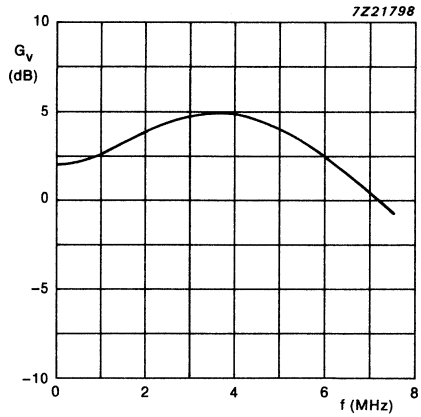


Fig.4 Frequency response of delayed signal.

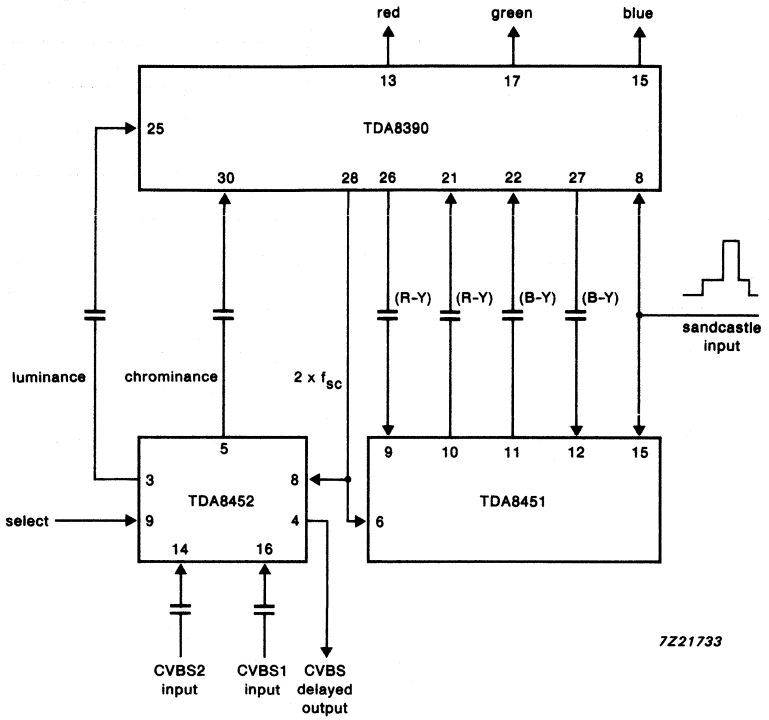


Fig.5 PAL decoder configuration.

DEVELOPMENT DATA

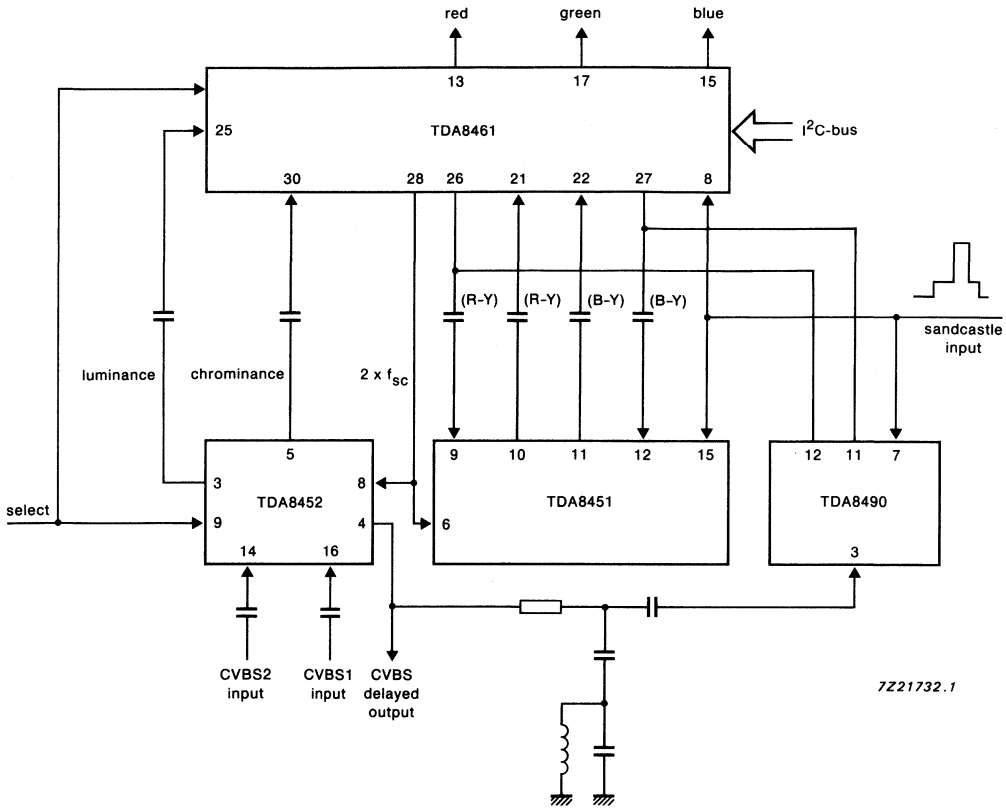


Fig.6 PAL-NTSC-SECAM decoder configuration.

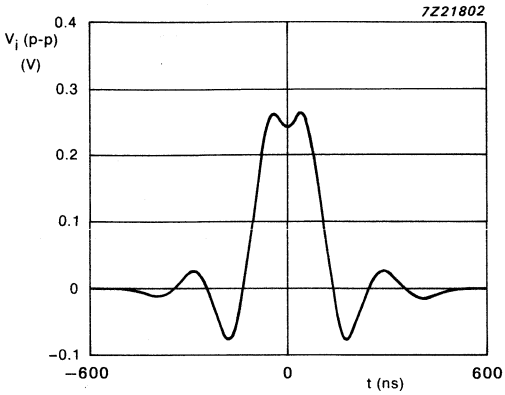


Fig.7(a) Luminance response (T pulse).

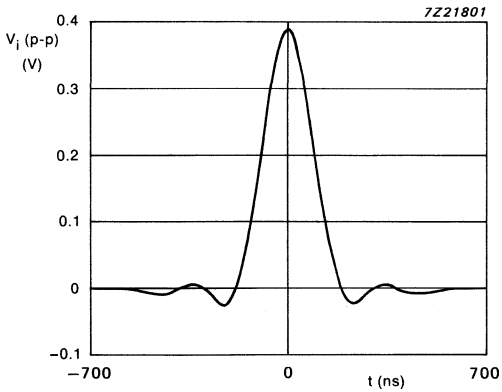


Fig.7(b) Luminance response (2T pulse).

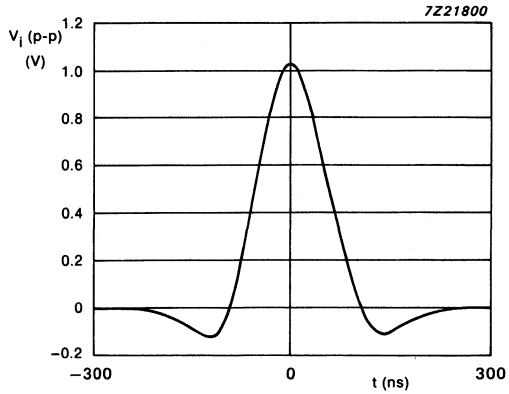


Fig.8(a) CVBS channel response (T pulse).

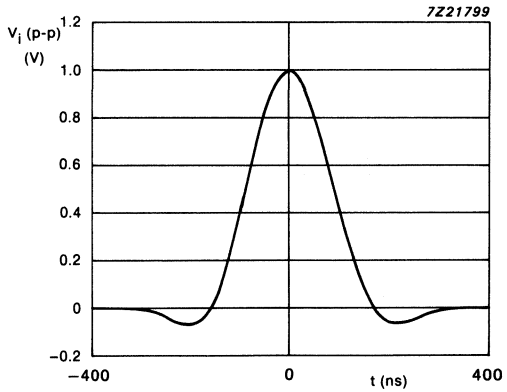


Fig.8(b) CVBS channel response (2T pulse).

PAL/NTSC DECODER WITH I²C BUS CONTROL

GENERAL DESCRIPTION

The TDA8461 is a multistandard colour decoder used in conjunction with delay line TDA8451, filter TDA8452 and SECAM decoder TDA8490. It combines all the functions required for the identification and demodulation of PAL/NTSC signals. The decoder comprises an I²C bus interface used to control the following functions:

- contrast
- saturation
- brightness
- hue, when in the NTSC position
- white point adjustment of the three colours
- peak white limiter adjustment

Via the I²C bus the decoder can be forced into the following modes: PAL, NTSC (4,43 MHz), NTSC (3,58 MHz) and SECAM when applied with the TDA8490.
The bus also indicates, as slave transmitter, the mode of the incoming signal (PAL, NTSC or SECAM).
The decoder contains separate inputs for data insertion, analogue as well as digital, which can be used for text display systems (e.g. channel number display, Teletext, Antiope, etc.).

Features

- I²C bus control
- Integrated filters (TDA8452) and delay lines (TDA8451) used in combination with TDA8461 eliminate the need for wire-wound components and adjustments
- A black-current stabilizer which controls the black currents of the three electron guns to a level low enough to omit the black level adjustment
- Inputs for RGB signals and fast switching
- Contrast and brightness control of inserted RGB signals
- Self-aligned oscillator
- Capacitive coupling of the luminance, colour difference and RGB inputs with black level clamping
- Equal black levels for internal TV and external signals
- Adjustable peak white limiter
- Matrix coefficients selectable for PAL/SECAM and NTSC (correction for FCC primaries)
- 12 MHz bandwidth
- Emitter follower outputs for driving the RGB output stages
- Two sandcastle pulse inputs for maximum design flexibility
- I²C bus on controlled DAC output

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 27)	V_P	10	12	13,2	V
Supply current (pin 27)	I_P	–	110	–	mA

PACKAGE OUTLINE

TDA8461: 40-lead DIL; plastic with internal heat spreader (SOT129).

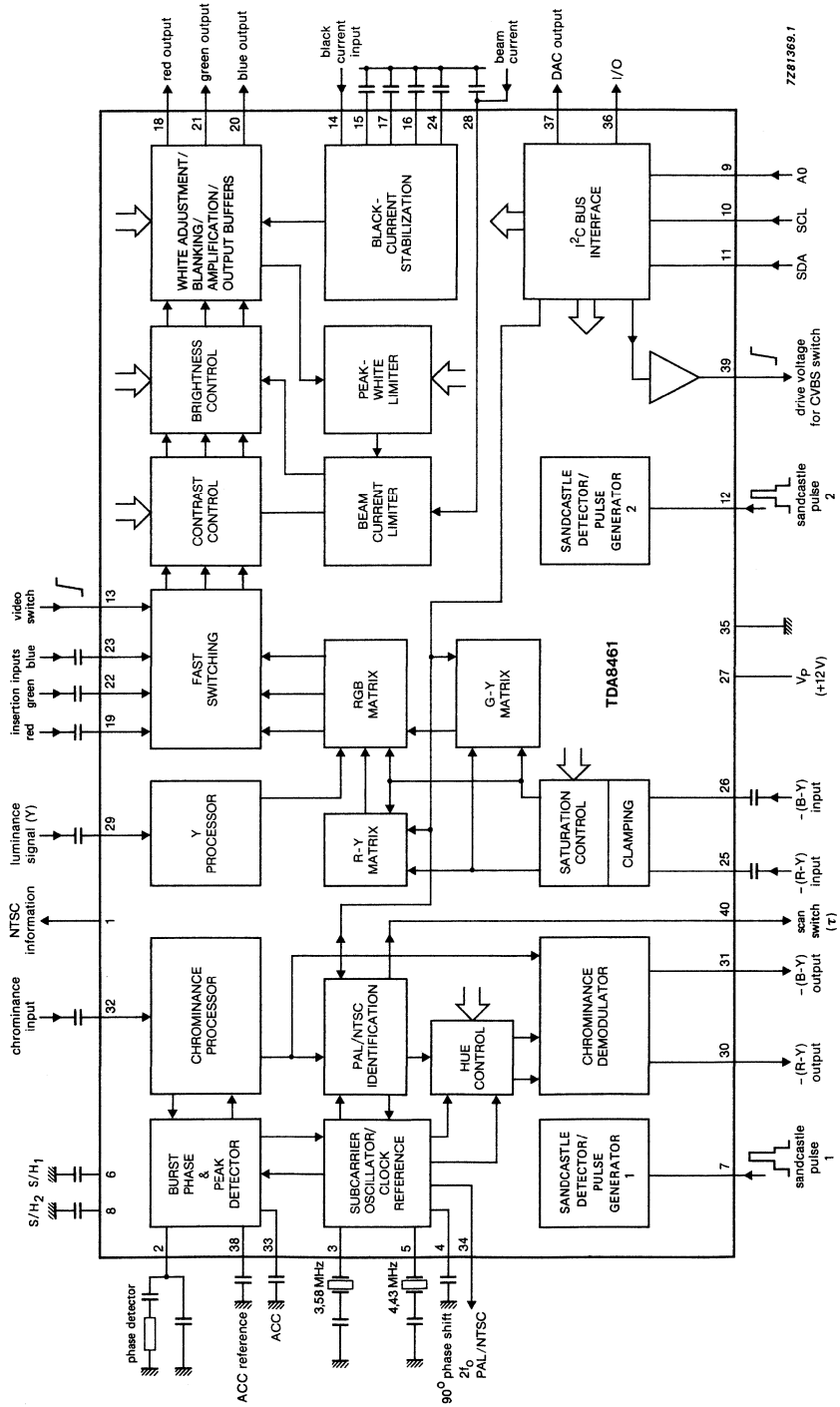


Fig. 1 Block diagram.

DEVELOPMENT DATA

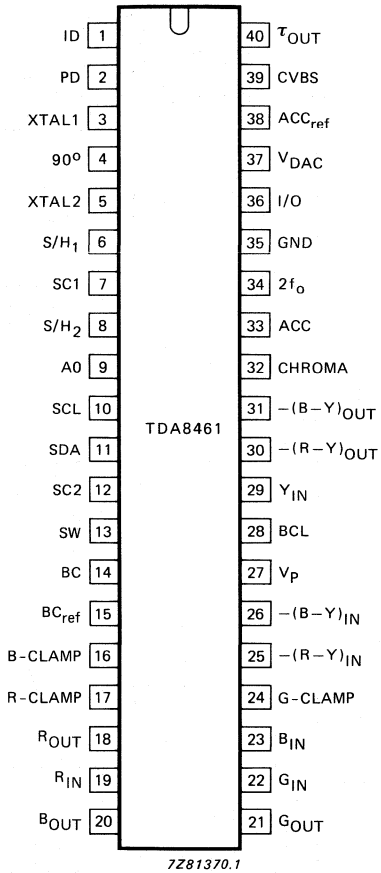


Fig. 2 Pinning diagram.

PIN FUNCTIONS

pin no.	mnemonic	description
1	ID	NTSC 3,58 identification information
2	PD	Phase detector
3	XTAL1	3,58 MHz NTSC reference frequency input
4	90^o	90^o phase shift DC reference
5	XTAL2	4,43 MHz PAL reference frequency input
6	S/H_1	Sample and hold 1 (PAL identification)
7	SC1	Sandcastle pulse input 1
8	S/H_2	Sample and hold 2 (NTSC identification)
9	AO	Programmable slave address pin
10	SCL	I^2C serial clock line
11	SDA	I^2C serial data line
12	SC2	Sandcastle pulse input 2
13	SW	Video switch input
14	BC	Black current input
15	BC_{ref}	Black current reference
16	B-CLAMP	B clamping circuit
17	R-CLAMP	R clamping circuit
18	R_{OUT}	Red signal output
19	R_{IN}	Red insertion input
20	B_{OUT}	Blue signal output
21	G_{OUT}	Green signal output
22	G_{IN}	Green insertion input
23	B_{IN}	Blue insertion input
24	G-CLAMP	G clamping circuit
25	$-(R\text{-}Y)_{IN}$	−(R-Y) colour difference input
26	$-(B\text{-}Y)_{IN}$	−(B-Y) colour difference input

pin no.	mnemonic	description
27	V_P	Positive supply voltage
28	BCL	Beam current limiter input
29	Y_{IN}	Luminance input
30	$-(R\text{-}Y)_{OUT}$	−(R-Y) signal output
31	$-(B\text{-}Y)_{OUT}$	−(B-Y) signal output
32	CHROMA	Chrominance input
33	ACC	Automatic colour control
34	$2f_o$	Frequency doubler output
35	GND	Ground
36	I/O	Input/output interface
37	V_{DAC}	DAC output voltage
38	ACC_{ref}	Automatic colour control reference voltage
39	CVBS	Drive voltage for CVBS switch (TDA8452)
40	τ_{OUT}	Scan switch output

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Colour decoder

The chrominance signal is amplified and is supplied to three detectors; the burst phase detector (ref. sign. R-Y phase), the automatic colour control (ACC) + NTSC synchronous detector (ref. sign. B-Y phase) and the PAL identification detector (ref. sign. ± R-Y phase).

The burst phase detector controls the oscillator which can operate at either 3,58 or 4,43 MHz. The internal switching selects the required crystal. The oscillator is followed by a Miller integrator to obtain the required 90^{o} phase shift and is biased to provide a sine-wave output.
Reference signals obtained from the oscillator and phase shift circuit are then used for the synchronous demodulation of the (B-Y) and (R-Y) signals. The demodulated colour difference signals then have the required amplitude ratio and are fed to the delay line circuit of the TDA8451. If the SECAM decoder TDA8490 is used, then the outputs from this device can be directly connected to the outputs of the TDA8461. The output levels have been chosen so as to give the PAL decoder priority (output level during PAL or NTSC is higher than output level during SECAM reception).

To provide the ACC voltage, the output signal from the ACC and NTSC detector is peak detected and delivered to a sample and hold circuit. The output from the PAL identification detector is also applied to a sample and hold circuit. These two circuits provide the incoming signal identification and the colour killer information.

Signal identification

The decoder scans the various systems sequentially (four fields per system).
As soon as a signal is identified, the scanning stops and the decoder remains locked to that standard until the killer indicates that the signal has disappeared. After this indication, the scanning will resume.
If the TDA8461 is to be used in conjunction with the TDA8490 SECAM decoder, the TDA8461 will be forced into the PAL mode on reception of a SECAM signal. This is because the delay lines for the colour difference signals in the TDA8451 are only operative in this mode.

The scanning system does not remain active during black/white reception as this would cause switching of the filters in the TDA8452. Scanning stops when no ACC voltage is present.

Both TDA8451/2 require a reference signal of $2 \times f_o$. To provide this, the oscillator frequency is internally doubled and is available at pin 34. Depending upon the incoming signal (PAL or NTSC), the DC voltage level on this pin is subject to change. This level change is detected by the TDA8451 so that the delayed signal can be switched OFF for NTSC (3,58 MHz and 4,43 MHz).

When an NTSC signal is identified the hue control circuit is switched-on. Hue control is provided by combining the two quadrature colour reference signals.

Control circuit

The luminance signal is derived from the TDA8452. The control circuit has inputs for luminance and colour difference signals, plus RGB inputs with fast switching. The required luminance signal amplitude is 0,45 V (p-p). After amplification, this signal is supplied to the R, G and B matrix where the colour difference signals are controlled on saturation. The (G-Y) signal is generated after control. The ratio of the colour difference signals which are fed to the RGB matrix is different for both PAL and NTSC signals:

For PAL the normal matrix is followed i.e. (G-Y) = −0,51 (R-Y) −0,19 (B-Y).
For NTSC a new (R-Y) signal is generated consisting of:

$$1{,}57(R\text{-}Y) - 0{,}41(B\text{-}Y).$$

Furthermore, the (G-Y) matrix is changed to −0,43(R-Y) −0,11(B-Y).

The (B-Y) factor remains unchanged, this is to obtain the preferred phase angle and amplitude ratio as normally used for NTSC.

After matrixing, the R, G and B signals are supplied to a switch circuit on which external RGB signals can be chosen. After amplification the RGB signals are controlled for contrast and brightness. The signals are fed to the output via white point adjustment. Typical output signal amplitudes are 4 V black to white (nominal controls). The black level of the three output signals is controlled by a black current stabilization circuit. The black current of the picture tube is obtained in the usual way (see TDA3566).

The TDA8461 has a peak-white limiting circuit. Because the black level at the outputs is dependent upon the black current feedback, the peak-white limiting circuit is adjustable via the I²C bus. Peak white reduces the signal amplitude via contrast. The device has a separate input for average beam current which reduces the signal amplitude via contrast and/or brightness, this is also adjustable via the I²C bus.

DEVELOPMENT DATA

I²C BUS SPECIFICATION

Write

The TDA8461 is controlled via the 2-line I²C bus as specified in the user manual "Single-chip 8-bit microcontrollers". In order to set up the TDA8461, a control message comprising a slave address, a R/W bit, a subaddress byte and one or more data bytes must be written to the device. The control word format is shown in Fig. 3, where AO (pin 9) is a pin programmable slave address bit.

If more than one data byte follows the subaddress, these bytes are stored in the successive registers by the automatic subaddress increment feature.

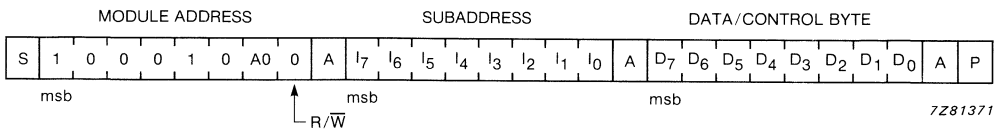


Fig. 3 Control word format for slave receiver.

Note: An acknowledge is only generated when a valid address is received.

I²C BUS SPECIFICATION (continued)

Control

Table 1 shows the bit arrangement and function of each data byte used in the control word.

Table 1 Control data

function	sub-address	data byte							
		D7	D6	D5	D4	D3	D2	D1	D0
brightness	00	X	X	A05	A04	A03	A02	A01	A00
saturation	01	X	X	A15	A14	A13	A12	A11	A10
contrast	02	X	X	A25	A24	A23	A22	A21	A20
hue	03	X	X	A35	A34	A33	A32	A31	A30
decoder control	04	MTRX	CDM2	CDM1	CDM0	CVBSS	RGBS	OFFN	SWOFF
universal DAC, I/O control	08	OUTP	X	A85	A84	A83	A82	A81	A80
peak white limit	09	BLM1	BLM0	A95	A94	A93	A92	A91	A90
red output gain	0A	X	X	AA5	AA4	AA3	AA2	AA1	AA0
green output gain	0B	X	X	AB5	AB4	AB3	AB2	AB1	AB0
blue output gain	0C	X	X	AC5	AC4	AC3	AC2	AC1	AC0

Control bit definition

MTRX control bit:

1	YUV/RGB matrix in PAL mode
0	YUV/RGB matrix in NTSC mode

If colour decoder mode control bits are set to non-forced mode, the YUV/RGB matrix will follow the "own intelligence" PAL or NTSC mode setting.

CDM2 - CDM0: Colour decoder mode bits

CDM2	CDM1	CDM0	function
0	0	0	not forced mode, own intelligence
0	0	1	forced NTSC, 3,58 MHz if a 3,58 MHz crystal is connected to pin 3
0	1	0	forced PAL –B, G, N or M if the correct crystal is connected to pin 5
0	1	1	forced SECAM*
1	0	0	forced NTSC 4,43 MHz mode*
1	0	1	forced PAL –B, G, N or M if the correct crystal is connected to pin 3
1	1	0	no function, reserved
1	1	1	no function, reserved

* If a 4,43 MHz crystal is connected to pin 5.

CVBSS control bit:

0	CVBS output LOW (CVBS1 selected)
1	CVBS output HIGH (CVBS2 selected)

RGBS source select control bit:

0	internal RGB selected
1	external RGB source selected (e.g. from TXT)

OFFN RGB output control bit:

0	RGB outputs are switched off, dark screen
1	RGB outputs are not switched off

SWOFF switch-off phase detector and killer bit:

0	phase detector and killer not switched off
1	phase detector and killer switched off*

OUTP output control bit:

0	output = LOW
1	output = HIGH; input mode

BLM0/BLM1 beam limiting control bits:

BLM1	BLM0	mode
0	0	inactive
0	1	active on contrast
1	0	active on brightness
1	1	active on contrast and brightness

DEVELOPMENT DATA

Read

The status of TDA8461 can also be read. Figure 4 illustrates status read format for the TDA8461 in the slave transmitter mode.
Note: change in direction of read/write bit.

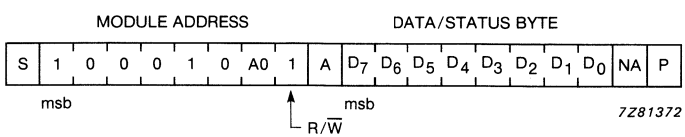


Fig. 4 Status read format slave transmitter.

* Only allowable in forced colour decoding mode.

I²C BUS SPECIFICATION (continued)

The general format of the data byte is shown in Fig. 5.

MSB LSB

PONRES	DECM2	DECM1	DECM0	0	0	0	INP

Fig. 5 Format of data byte.

Bit definition

PONRES power-on reset bit:

A power failure or a power-on reset will set this bit. A succesfull read of the data byte will reset this bit.

DECM2/DECM1/DECM0 colour decoder mode bits:

DECM2	DECM1	DECM0	function
0	0	0	no colour standard identified
0	0	1	NTSC 3,58 MHz
0	1	0	PAL –B, G, N or M*
0	1	0	SECAM
1	0	0	NTSC 4,43 MHz
1	0	1	PAL –B, G, N or M**
1	1	0	unused
1	1	1	unused

INP input function status bit:

0	Input LOW	operates only as input if bit OUTP is logic 1
1	Input HIGH	

Unused status bits are transmitted as logic 0

* Depending upon the crystal connected to pin 5.
** Depending upon the crystal connected to pin 3.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 27)	V_P	–	13,2	V
Total power dissipation (encapsulation)	P_{tot}	–	2,5	W
Storage temperature range	T_{stg}	–25	+ 150	°C
Operating ambient temperature range	T_{amb}	–25	+ 70	°C

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j\text{-}a}$ = 40 K/W

DEVELOPMENT DATA

CHARACTERISTICS

$V_P = V_{27-35} = 12$ V; $T_{amb} = 25$ °C; all voltages referenced to ground unless otherwise specified

parameter	condition	symbol	min.	typ.	max.	unit
Chrominance amplifier (pin 32)						
Input signal amplitude (peak-to-peak value)	note 1		–	465	–	mV
Input signal amplitude	preclipping		–	–	1100	mV
Input resistance (pin 32)		R_I	–	12	–	kΩ
Input capacitance (pin 32)		C_I	–	–	4,0	pF
ACC control range			30	–	–	dB
Min. burst amplitude within control range (peak-to-peak value)			30	–	–	mV
Reference section						
Phase locked loop catching range	note 2	Δf	± 500	–	–	Hz
Phase shift for ± 400 Hz deviation of f_{osc}	note 2	$\Delta\varphi$	–	–	5	deg
Oscillator						
Temperature coefficient of oscillator frequency	note 3	TC_{osc}	–	–2	–	Hz/K
Frequency deviation for a supply voltage change from 10 to 13,2 V		Δf_{osc}	–	40	–	Hz
Input resistance (pin 3)		R_I	–	1500	–	Ω
(pin 5)		R_I	–	650	–	Ω
Input capacitance (pins 3 and 5)		C_I	–	–	6,0	pF
ACC generation/identification	note 4					
Voltage at the PAL identification output (pin 6)						
nominal input signal for PAL		V_6	–	5,0	–	V
nominal input signal for NTSC		V_6	–	3,1	–	V
without burst input		V_6	–	3,1	–	V

parameter	condition	symbol	min.	typ.	max.	unit
Colour-OFF voltage		V_6	–	3,3	–	V
Colour-ON voltage		V_6	–	3,5	–	V
Voltage identification for flip-flop reset		V_6	–	2,8	–	V
Voltage at NTSC identification output (pin 8)						
nominal input signal for PAL		V_8	–	5,3	–	V
nominal input signal for NTSC		V_8	–	5,3	–	V
without burst input		V_8	–	3,1	–	V
Colour-OFF voltage		V_8	–	3,6	–	V
Colour-ON voltage		V_8	–	3,8	–	V
Peak detector voltage (pin 33)						
nominal input signal		V_{33}	–	5,8	–	V
without nominal input signal		V_{33}	–	2,7	–	V
Demodulators						
Output voltage during PAL (R-Y) output (pin 30) (peak-to-peak value)		$V_{30(p-p)}$	0,50	0,62	0,74	V
(B-Y) output (pin 31) (peak-to-peak value)		$V_{31(p-p)}$	0,64	0,80	0,96	V
Output voltage during NTSC (R-Y) output (pin 30) (peak-to-peak value)		$V_{30(p-p)}$	1,00	1,24	1,48	V
(B-Y) output (pin 31) (peak-to-peak value)		$V_{31(p-p)}$	1,28	1,60	1,92	V
Amplification ratio of demodulated signals (B-Y)/(R-Y)		$V_{31,30}$	1,60	1,78	1,96	
Spread of PAL/NTSC signal amplitude ratio	(R-Y) channel		−1	–	1	dB
Frequency response	0 to 1 MHz		–	−3	–	dB
Colour difference output impedance		Z_O	–	100	–	Ω

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	condition	symbol	min.	typ.	max.	unit
Demodulators (continued)						
DC output voltage after signal identification		$V_{31,30}$	–	8,3	–	V
DC output voltage during colour killing		$V_{31,30}$	–	1,3	–	V
Unwanted signals at (R-Y)/(B-Y) outputs	note 5		–	–	*	dB
Residual carrier (peak-to-peak value)						
(R-Y)	4,4 MHz	$V_{30(p\text{-}p)}$	–	–	*	mV
(R-Y)	8,8 MHz + harmonics	$V_{30(p\text{-}p)}$	–	–	*	mV
(B-Y)	4,4 MHz	$V_{31(p\text{-}p)}$	–	–	*	mV
(B-Y)	8,8 MHz + harmonics	$V_{31(p\text{-}p)}$	–	–	*	mV
H/2 ripple voltage at (R-Y) outputs without input signal; (peak-to-peak value)		$V_{30(p\text{-}p)}$	–	–	50	mV
Change in colour difference amplitudes with temperature		$\Delta V/\Delta T$	–	0,1	–	%/K
with supply voltage; (10%)		$\Delta V/\Delta V$	–	–	0,1	dB
Hue control	via I^2C bus					
Phase shift variation		φ	–	0±50	–	deg
		$\Delta\varphi$	–	–	5	deg
Hue control curve	see Fig. 6					
Sandcastle pulse 1 (pin 7)						
Detection level for:						
vertical blanking		V_7	1,0	1,5	2,0	V
horizontal blanking		V_7	3,0	3,5	4,0	V
burst key pulse		V_7	6,5	7,0	2,0	V
Input current (pin 7)						
0,5 to 1,5 V		V_7	–	–	–0,5	mA
1,5 to 7,0 V		V_7	–	–16,0	–	μA
7,0 to 12,0 V		V_7	–	–0,1	–	μA

* Value to be fixed.

DEVELOPMENT DATA

parameter	condition	symbol	min.	typ.	max.	unit
Frequency doubler output (pin 34)						
Output signal voltage; (peak-to-peak value)	PAL/NTSC	$V_{34(p-p)}$	–	350	–	mV
Output impedance		Z_O	–	50	–	Ω
DC output level						
PAL		V_{34}	–	4,9	–	V
NTSC		V_{34}	–	7,0	–	V
NTSC information (pin 1)						
Output voltage level:						
on identification of NTSC 3,58 MHz		V_1	–	8,0	–	V
other modes		V_1	–	2,0	–	V
Output impedance		Z_O	–	–	500	Ω
ACC reference (pin 38)						
DC level		V_{38}	–	7,3	–	V
Scan switch output (pin 40)	open collector					
Clamp scan level		V_{40}	–	0,1	–	V
Input leakage current at signal identification		I_{LI}	–	5,0	–	μA
Luminance input (pin 29)						
Input voltage (peak-to-peak value)	note 6	$V_{29(p-p)}$	–	0,45	–	V
Pre-clipping input voltage		V_{29}	–	–	0,9	V
Input current		I_{29}	–	0,1	1,0	μA
Frequency response of total luminance and amplifier circuits	0 to 12 MHz		–	–3	–	dB
Colour difference input signals						
Input signal amplitude						
(R-Y) (pin 25)		V_{25}	–	0,62	–	V
(B-Y) (pin 26)		V_{26}	–	0,8	–	V
Colour difference input currents (pins 25 and 26)		$I_{25,26}$	–	0,1	1,0	μA

CHARACTERISTICS (continued)

parameter	condition	symbol	min.	typ.	max.	unit
RGB inputs (pins 19, 22 and 23)						
Input signal amplitude (peak-to-peak value)	note 7	$V_{19,22,23(p-p)}$	–	0,7	–	V
Δ Black level	note 8	$\Delta V_{19,22,23}$	–	–	*	V
Frequency response of RGB/Teletext amplifier	0 to 12 MHz		–	–2	–	dB
Delay difference	3 channels	t_d	–	0	–	ns
Input current		$I_{19,22,23}$	–	–	10	μA
Video switching (pin 13)						
Input voltage	no signal insertion	V_{13}	–	–	0,3	V
Input voltage	signal insertion note 9	V_{13}	0,9	–	3,0	V
Delay of switching		t_d	–	–	50	ns
Input resistance		R_{13}	–	10	–	kΩ
Suppression of internal RGB signal	when $V_{13} > 0{,}9$ V, 0 - 5 MHz		46	–	–	dB
Suppression of external RGB signals	when $V_{13} < 0{,}3$ V, 0 - 5 MHz		*	–	–	dB
Sandcastle pulse 2 (pin 12)						
Detection level for:						
vertical blanking		V_{12}	1,0	1,5	2,0	V
horizontal blanking		V_{12}	3,0	3,5	4,0	V
upper part of pulse		V_{12}	6,5	7,0	7,5	V

* Value to be fixed.

DEVELOPMENT DATA

parameter	condition	symbol	min.	typ.	max.	unit
Input current						
0 to 1,5 V		I_{12}	–	–	–0,5	mA
1,5 to 3,5 V		I_{12}	–	–16,0	–	μA
3,5 to 7,0 V		I_{12}	–	–5,0	–	μA
7,0 to 12,0 V		I_{12}	–	–0,1	–	μA
Saturation control	via I²C bus					
Saturation control range		G	50	–	–	dB
Saturation control curve	see Fig. 7					
Contrast control	via I²C bus					
Contrast control range	note 10	G	–	20	–	dB
Tracking of contrast control range between three channels	over 10 dB range		–	–	0,5	dB
Contrast control curve	see Fig. 8					
Brightness control	via I²C bus					
Brightness control voltage	note 14; at nominal white point adjustment		–	2,0	–	V
Brightness control curve	see Fig. 9					
White point adjustment (WPA)	via I²C bus					
Control range		CR	–	8	–	dB
		ΔCR	–	–	1	dB
Peak white limiting (PWL)	via I²C bus					
Control range	nominal WPA		5,0	–	10	V
Colour difference matrices						
PAL mode	(R-Y), (B-Y) not affected					
(G-Y)/(R-Y)			–	–0,51	–	
(G-Y)/(B-Y)			–	–0,19	–	
NTSC mode	(B-Y) not affected					
(R-Y)'/(R-Y)			–	+ 1,57	–	
(R-Y)'/(B-Y)			–	–0,41	–	
(G-Y)/(R-Y)			–	–0,43	–	
(G-Y)/(B-Y)			–	–0,11	–	

CHARACTERISTICS (continued)

parameter	condition	symbol	min.	typ.	max.	unit
RGB amplifiers						
Output signal amplitude (peak-to-peak value)	note 11	$V_{18,20,21}$ (p-p)	–	4,0	–	V
Output signal amplitude for blue channel (peak-to-peak value)	note 12	$V_{20(p-p)}$	–	5,4	–	V
Maximum peak white level		$V_{18,20,21}$ (p-p)	–	10,5	–	V
Available output current		$I_{18,20,21}$	10	–	–	mA
Difference in black level between three channels	note 13; at nominal brightness and nominal WPA	$\Delta V_{18,20,21}$	–	–	10	mV
Delay between leading edges of sandcastle upper part and black level clamping pulse		t_d	–	*	–	μs
Control range of black current stabilization	V_{black} = 3 V; nominal brightness and nominal WPA		–	–	± 2	V
Black level shift with picture content			–	–	40	mV
Output voltage during the 4L pulse after switch-on		$V_{18,20,21}$	7,5	–	–	V
Variation of black level with temperature		$\Delta V/\Delta T$	–	0	–	mV/K
with contrast control	+3 to −17 dB note 14; at nominal saturation and WPA	ΔV	–	–	*	mV

* Value to be fixed.

DEVELOPMENT DATA

parameter	condition	symbol	min.	typ.	max.	unit
Relative spread between the R, G and B output signals			–	–	10	%
Relative black level variation between the three channels during variation of supply voltage (± 10%) at nominal controls	note 14		–	0	*	mV
contrast	(20 dB) at nominal saturation and WPA		–	–	*	mV
saturation	(50 dB) at nominal contrast and WPA		–	–	*	mV
brightness	(± 1 V) at nominal controls		–	–	*	mV
Differential drift of the black level	over range of 40 K; note 14		–	0	20	mV
Blanking level at the RGB outputs			–	1,0	–	V
Difference in blanking level of the three channels			–	0	10	mV
Differential drift of the blanking levels	over range of 40 K		–	0	10	mV
Tracking of output black levels with supply voltage		$\frac{\Delta V_{bl} \times V_p}{V_{bl} \times \Delta V_p}$	0,9	1,0	1,1	
Signal to noise ratio of output signals	note 5	S/N	*	–	–	dB
Residual 4,4 MHz signal at RGB outputs (peak-to-peak value)			–	–	*	mV
Residual 8,8 MHz signal at RGB outputs (peak-to-peak value)			–	–	*	mV
Output impedance		$Z_{18,20,21}$	–	50	–	Ω
Current source of output stage			–	2,5	–	mA

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	condition	symbol	min.	typ.	max.	unit
Black current stabilization						
DC bias voltage (pin 14)		V_{14}	3,5	5,0	7,0	V
Difference between input voltage for black current and leakage current		ΔV	0,35	0,5	0,65	V
Input current during:						
black current		I_{14}	–	–	1,0	μA
scan		I_{14}	–	–	10	mA
Internal limiting level (pin 14)		V_{14}	8,5	9,0	9,5	V
Switching threshold for black current control ON		V_{14}	7,6	8,0	8,4	V
Input resistance during scan (pin 14)		R_{14}	1,0	1,5	2,0	kΩ
DC input current during scan of clamping inputs (pins 24, 16 and 17)		$I_{24,16,17}$	–	–	50	nA
Maximum charge/discharge current during measuring time of clamping pulse (pins 24, 16 and 17)		$I_{c/d}$	0,5	–	–	mA
Beam current limiter (BCL) (pin 28)						
Voltage when BCL or PWL function is inactive	note 15	V_{28}	5,0	–	–	V
Trigger level for BCL or PWL function		V_{28}	–	4,2	–	V
I²C BUS INTERFACE						
I/O interface (pin 36)	note 16					
DAC output (pin 37)						
Control range of output voltage		V_O	0,5	–	10,0	V
Output impedance		Z_O	–	100	–	Ω
Drive output for CVBS switch (pin 39)						
Output voltage LOW		V_{OL}	–	–	1	V
Output voltage HIGH		V_{OH}	10	–	–	V
Output current HIGH	note 17	I_{OH}	3	–	–	mA
Output impedance		Z_O	–	–	300	Ω

Notes to the characteristics

1. Indicated is a signal for a colour bar with 75% saturation (chroma/burst ratio of 2,2 :1).
2. All frequency variations are referred to the 3,58 MHz or 4,43 MHz carrier frequency.
3. The oscillator can run on two frequencies (i.e. when two crystals are connected to the device). Switching between the two reference frequencies is controlled internally or via the I²C bus.
4. The various modes are sequentially scanned (four field periods per mode) until a signal is identified. The voltage levels on the two detection pins in the various modes are given.
5. The ratio between wanted and unwanted signals (e.g. crosstalk, phase errors and noise) is specified as the output signal amplitude (peak-to-peak value at nominal conditions) with respect to the r.m.s. value of the unwanted signal.
6. Signal with negative going sync. Amplitude contains sync pulse amplitude.
7. For a resultant B/W output signal of 4 V, at nominal contrast and nominal white point adjustment.
8. Difference in black level between RGB signals and inserted signals.
9. For normal use, the input voltage should be 3 V maximum. (The range between 4 V and 12 V is used for testing).
10. Nominal contrast is specified as maximum contrast −3 dB. Nominal saturation as maximum saturation −6 dB; nominal white point adjustment is maximum −3 dB.
11. Nominal luminance, contrast and white point adjustment.
12. Nominal contrast, saturation control set and no (R-Y) luminance signal.
13. With respect to the measuring pulse. At nominal brightness the black level of one output is identical to the measuring level.
14. With respect to the measuring pulse.
15. Pin 28 should be externally connected to a high-resistance voltage divider. Pins 13, 19, 22 and 23 when unused, should be connected to ground via a 75 Ω (typ.) resistor.
16. See I²C bus specification.
17. Higher output currents are allowed but this will decrease V_{OH}.

DEVELOPMENT DATA

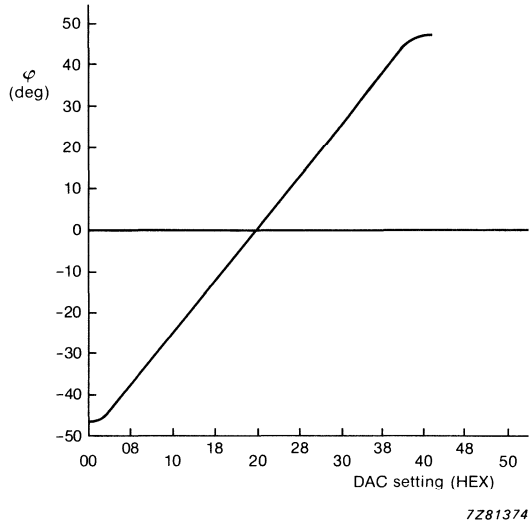


Fig. 6 Typical hue control curve.

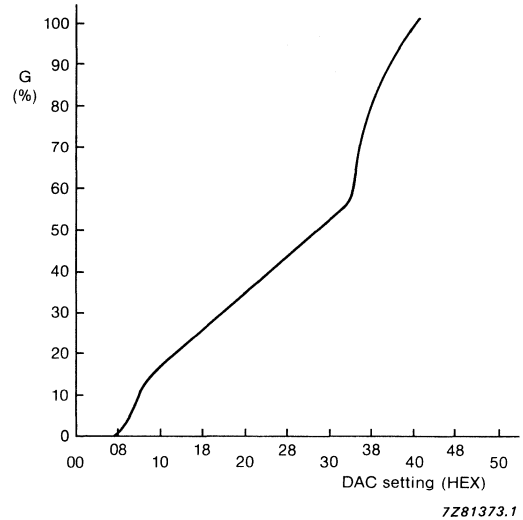


Fig. 7 Typical saturation control curve.

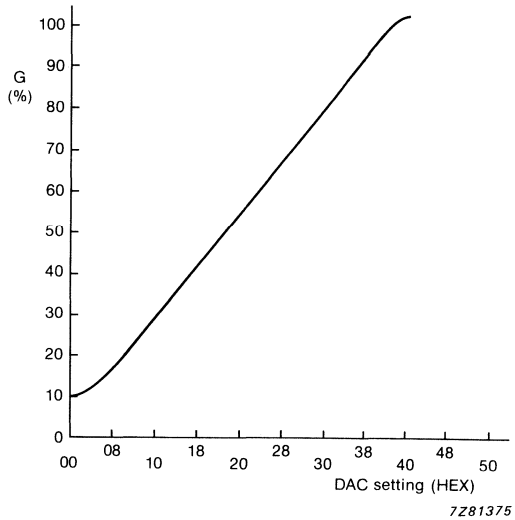


Fig. 8 Typical contrast control curve.

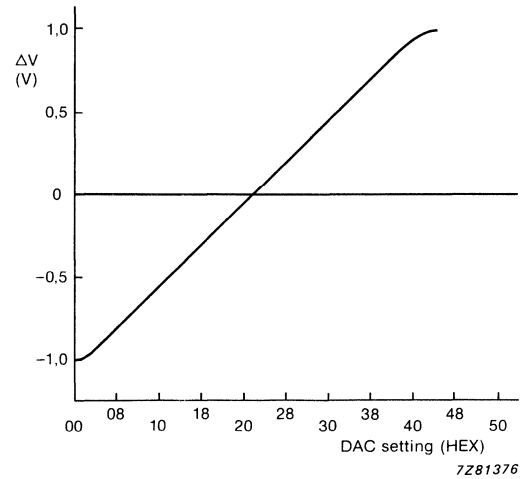


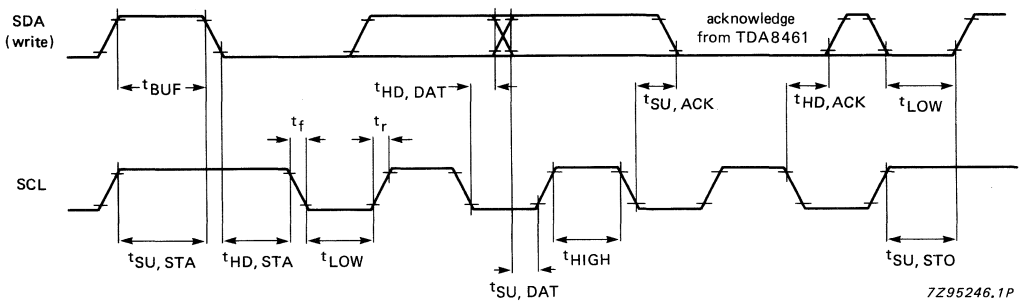
Fig. 9 Difference between black level and measuring level at the RGB outputs (ΔV) as a function of the DAC setting in hexadecimal at nominal WPA setting.

DEVELOPMENT DATA

I²C BUS TIMING (see Fig. 10)

Bus loading conditions: 4 kΩ pull-up resistor to + 5 V; 200 pF capacitor to GND.
All values are referred to V_{IH} = 3 V and V_{IL} = 1,5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4,0	–	–	μs
Start condition set-up time	$t_{SU,STA}$	4,0	–	–	μs
Start condition hold time	$t_{HD,STA}$	4,0	–	–	μs
LOW period SCL, SDA	t_{LOW}	4,0	–	–	μs
HIGH period SCL	t_{HIGH}	4,0	–	–	μs
Rise time SCL, SDA	t_R	–	–	1,0	μs
Fall time SCL, SDA	t_F	–	–	0,30	μs
Data set-up time (write)	$t_{SU,DAT}$	1	–	–	μs
Data hold time (write)	$t_{HD,DAT}$	1	–	–	μs
Acknowledge (from TDA8461) set-up time	$t_{SU,ACK}$	–	–	3,5	μs
Acknowledge (from TDA8461) hold time	$t_{HD,ACK}$	0	–	–	μs
Stop condition set-up time	$t_{SU,STO}$	4,0	–	–	μs



Reference levels are 10 and 90%

Fig. 10 I²C bus timing, TDA8461.

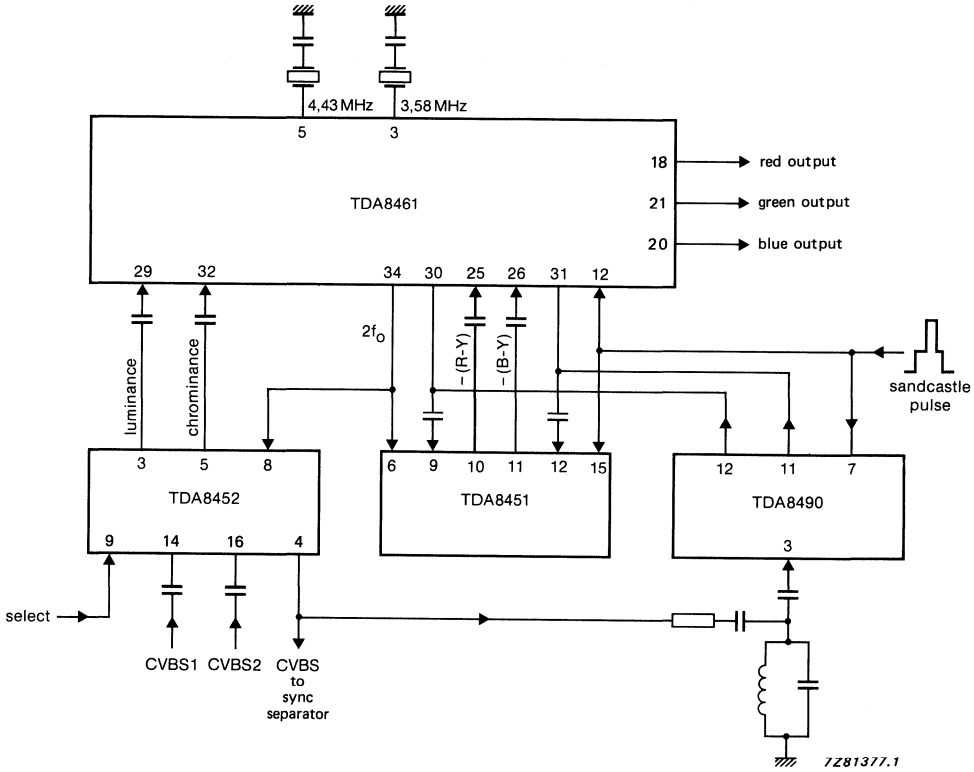


Fig. 11 Application diagram showing the complete multi-standard decoder system.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

SECAM DECODER

GENERAL DESCRIPTION

The TDA8490 is a monolithic integrated SECAM decoder. This circuit is intended to be used in conjunction with TDA8390 or TDA8461 (PAL decoder), TDA8451 (delay) and TDA8452 (filter). In this application the TDA8490 is placed in parallel with the demodulation circuit of the PAL decoder.

Features

- Limiter input for chrominance signal
- SECAM demodulator
- Clamp circuits and de-emphasis for colour difference signals
- Sandcastle pulse detector
- Identification circuit for horizontal and vertical SECAM identification

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		$V_P = V_{9-1}$	10,8	12,0	13,2	V
Supply current		$I_P = I_9$	40	55	70	mA
Chrominance amplifier and demodulator						
Input signal (peak-to-peak value)	SECAM with correct limiting	$V_{3-1(p-p)}$	15	100	300	mV
R-Y and B-Y output						
R-Y output signal amplitude (peak-to-peak value)	pin 12	$V_{12-1(p-p)}$	1,01	1,26	1,51	V
B-Y output signal amplitude (peak-to-peak value)	pin 11	$V_{11-1(p-p)}$	1,28	1,60	1,92	V
Identification						
Input voltage for line identification	pin 4	V_{4-1}	4,1	–	13,2	V
Input voltage for frame identification	pin 4	V_{4-1}	0	–	2,9	V
Switching level for line/frame identification	pin 4	V_{4-1}	3,0	3,5	4,0	V
Sandcastle detector and clamp pulse generator						
Frame blanking detection level		V_{7-1}	1,0	1,5	2,0	V
Line blanking detection level		V_{7-1}	3,0	3,5	4,0	V
Burst gate detection level		V_{7-1}	6,5	7,0	7,5	V

PACKAGE OUTLINE

18-lead DIL; plastic, with internal heat spreader (SOT102).

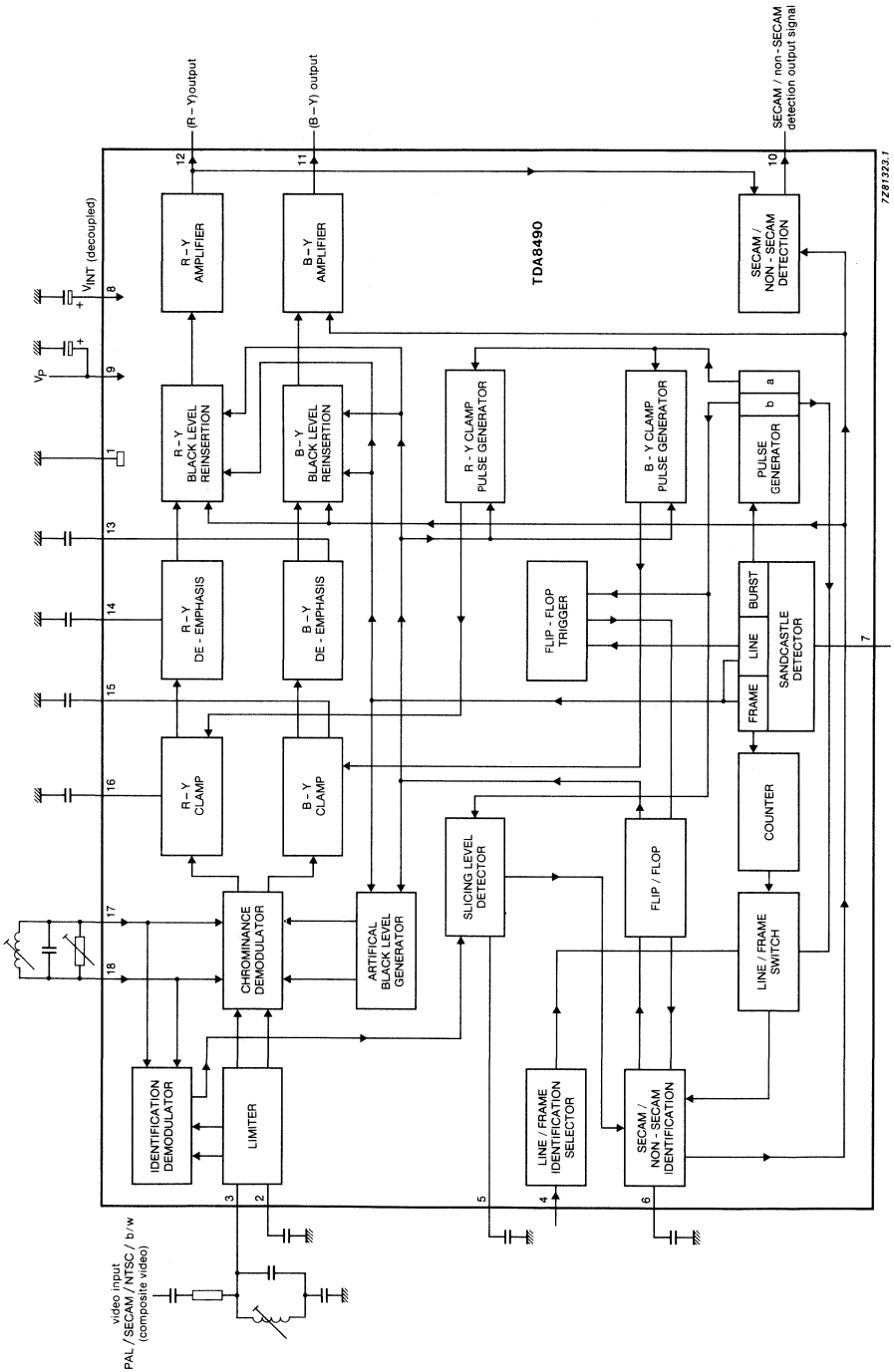


Fig. 1 Block diagram.

PINNING

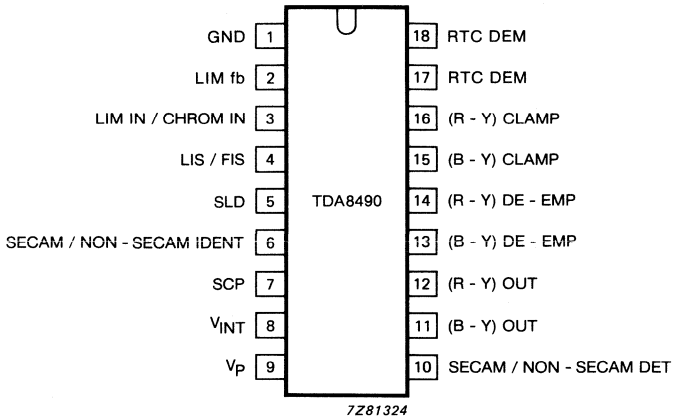


Fig. 2 Pinning diagram.

DEVELOPMENT DATA

1	GND	ground	9	V_P	supply voltage
2	LIM fb	limiter feedback	10	SECAM/NON-SECAM DET	SECAM/non-SECAM detection circuit
3	LIM IN/ CHROM IN	limiter input/ chrominance input	11	(B-Y)OUT	(B-Y) signal output
4	LIS/FIS	line identification selector/ frame identification selector	12	(R-Y)OUT	(R-Y) signal output
			13	(B-Y)DE-EMP	(B-Y) de-emphasis circuit
5	SLD	slicing level detector	14	(R-Y)DE-EMP	(R-Y) de-emphasis circuit
6	SECAM/NON-SECAM IDENT	SECAM/non-SECAM identification circuit	15	(B-Y)CLAMP	(B-Y) clamping circuit
			16	(R-Y)CLAMP	(R-Y) clamping circuit
7	SCP	sandcastle pulse input	17	RTC DEM	reference tuned circuit demodulator
8	V_{INT}	internal supply voltage (decoupled)	18	RTC DEM	reference tuned circuit demodulator

FUNCTIONAL DESCRIPTION

Demodulation

The TDA8490 comprises a chrominance and an identification demodulator, both using the same reference tuned circuit. The identification circuit automatically detects whether the incoming signal at pin 3 (applied via a bandpass filter with a bell-shaped response) is SECAM or non-SECAM (NTSC, PAL or black-and-white).

When the SECAM signal is detected, it is applied to a limiter/amplifier after which it is demodulated. The (R-Y) and (B-Y) signals are applied sequentially, therefore, only one demodulator is required. After demodulation the signals are applied to the (R-Y) and (B-Y) clamp circuits, where the black levels are clamped to the same DC level.

Artificial black levels are inserted during line blanking period. The clamp circuits then react upon these levels instead of the demodulated burst signal (necessary in case there are no line burst signals available). The inserted signals may not be identical to the detected black levels, because of circuitry spread. This can be corrected by detuning the demodulator tuned circuit.

R-Y and B-Y output signals

The R-Y and B-Y signals are available every other line. A new black level is reinserted during blanking and timing b (Fig. 5). If a non-SECAM signal is present the R-Y output will generate a DC level of approximately 3,8 V (the same as the black level generated during normal SECAM condition on both outputs). The B-Y output generates a DC level of approximately 0,8 V in this condition.

SECAM or non-SECAM signals may also be identified by the information at pin 10:

- 2,6 V indicates a SECAM signal.
- 0 V indicates a non-SECAM signal.

The SECAM or non-SECAM signals can be identified by using the (B-Y) demodulator output level at pin 11. Depending on the PAL decoder used in conjunction with this device, the information can be passed to the microcomputer via the I^2C bus.

Priority identification

The two chrominance outputs of TDA8490 are connected to the chrominance outputs of the PAL decoder TDA8461 or TDA8390. The output signal of the TDA8490 and PAL decoder alternately determine the priority of the overall system. In the event of a clash on these outputs, caused by a reflected PAL signal being detected as a SECAM signal by TDA8490, the total system will default to PAL priority.

Identification

The identification circuit compares the voltage difference, which is obtained after demodulation, with the state of the flip-flop. For line identification this comparison occurs during the internally generated pulse 'B' (Fig. 3). Only SECAM signals provide voltage difference from line to line during comparison. If the phase relationship between both the signals is incorrect, the flip-flop will receive an extra input pulse.

The identification (as above) occurs when the line identification system is active. When the frame identification system is switched on (pin 4), the system only compares the demodulator output voltage during a 4-line gate pulse, which is present during frame blanking. The 4-line gate pulse starts 10 burst gate pulses after the start of the vertical blanking part of the sandcastle signal. The operation is identical to the line identification. Timing of the 4-line gate pulse is shown in Fig. 4.

Sandcastle detector

The sandcastle pulse detector requires a 3-level sandcastle pulse. It detects the various blanking and gating pulses and generates the correct drive pulses for the clamping circuits (Fig. 3).

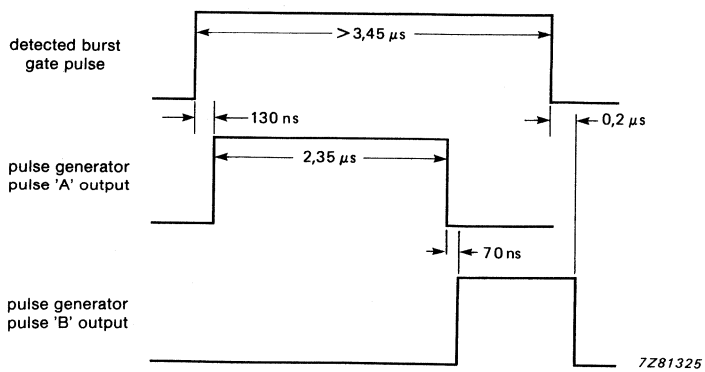


Fig. 3 Burst and derived pulses.

Note

The separated burst pulse is divided into two parts (Fig. 3). Required burst gate pulse: $> 3{,}45\ \mu s$.

Pulse 'A':

- timing R-Y clamp (only present during a red line)
- timing B-Y clamp (only present during a blue line)

Pulse 'B':

- SECAM line identification timing

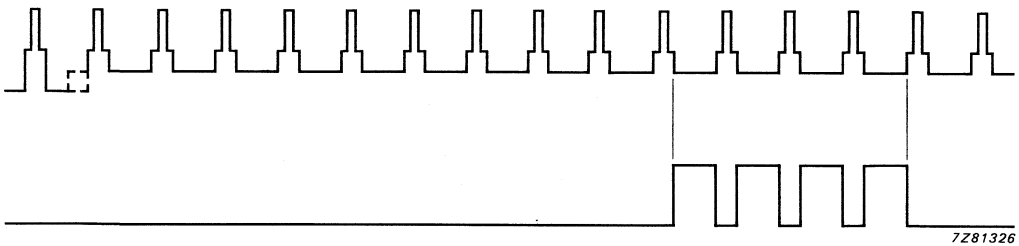


Fig. 4 above: Sandcastle signal during frame period (even and odd).

below: 4-line gate pulse.

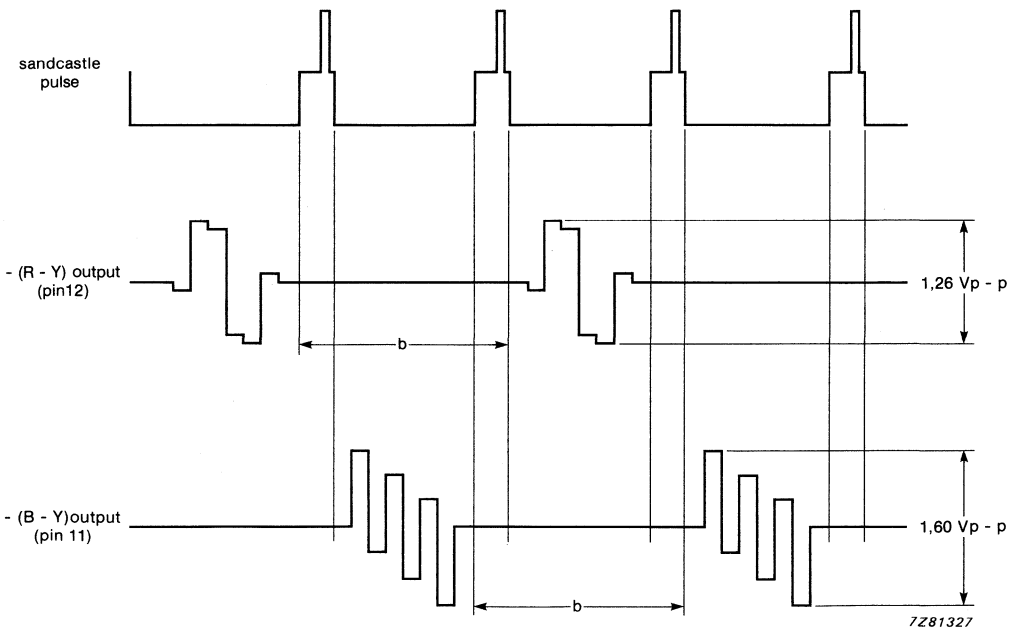


Fig. 5 $-$(R-Y) and $-$(B-Y) output signals compared to the sandcastle input signal.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	pin 9	V_P	–	13,2	V
Total power dissipation		P_{tot}	–	1,7	W
Storage temperature range		T_{stg}	–25	+ 150	°C
Operating ambient temperature range		T_{amb}	–25	+ 65	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		$V_P = V_{9-1}$	10,8	12,0	13,2	V
Supply voltage	decoupled, pin 8	$V_{INT} = V_{8-1}$	10,6	11,8	13,0	V
Supply current		$I_P = I_9$	40	55	70	mA
Total power dissipation		P_{tot}	–	660	840	mW
Thermal resistance from junction to ambient		$R_{th\ j\text{-}a}$	–	50	–	K/W
External capacitance	pin 8	$C_o = C_{8-1}$	–	–	4,7	μF
Chrominance amplifier and demodulator	note 1					
Input signal (peak-to-peak value)	non-SECAM signal	$V_{3-1(p-p)}$	–	–	1,1	V
Input signal (peak-to-peak value)	SECAM signal with correct limiting	$V_{3-1(p-p)}$	15	100	300	mV
Input resistance	pin 3	R_{3-1}	9,5	11,8	14,1	kΩ
Input capacitance	pin 3	C_{3-1}	–	–	5	pF
Input resistance	between pins 17 and 18	R_{17-18}	2,9	3,6	4,3	kΩ
Input capacitance	between pins 17 and 18	C_{17-18}	–	12	–	pF
De-emphasis output resistance	pins 13 and 14	R_{13-1} R_{14-1}	1,45	1,75	2,05	kΩ
Zero point stability of chrominance demodulator	note 2 pins 11 and 12	$f_{11, 12}$	–	5	–	kHz
(B-Y)/(R-Y) gain ratio	note 7		1,38	1,55	1,73	

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
R-Y and B-Y output						
R-Y output signal amplitude (peak-to-peak value)	pin 12	$V_{12-1(p-p)}$	1,01	1,26	1,51	V
B-Y output signal amplitude (peak-to-peak value)	pin 11	$V_{11-1(p-p)}$	1,28	1,60	1,92	V
B-Y output signal level	SECAM		3,5	3,8	4,1	V
B-Y output signal level	non-SECAM		–	0,8	1,1	V
R-Y output signal level			3,5	3,8	4,1	V
R-Y signal linearity	note 3		88	95	102	%
B-Y signal linearity	note 4		85	92	99	%
Inserted black levels (demodulated)	function of temperature, note 6		–	0,22	–	kHz/K
Output impedance	pin 12	$\lvert Z_{12-1}\rvert$	–	30	–	Ω
Output impedance	pin 11	$\lvert Z_{11-1}\rvert$	–	30	–	Ω
Identification	SECAM, non-SECAM					
Input voltage for line identification	pin 4	V_{4-1}	4,1	–	13,2	V
Input voltage for frame identification	pin 4	V_{4-1}	0	–	2,9	V
Switching level for line/frame identification	pin 4	V_{4-1}	3,0	3,5	4,0	V
Input current	pin 4	I_4	–	–5	–25	μA
Voltage at pin 6	during non-SECAM	V_{6-1}	–	10,2	–	V
Voltage at pin 6	during SECAM	V_{6-1}	–	7,7	–	V
Identification level at pin 6		V_{6-1}	10,5	10,8	11,0	V
Internal colour 'OFF' (pin 6)	SECAM to non-SECAM	V_{6-1}	9,7	10,0	10,3	V
Internal colour 'ON' (pin 6)	non-SECAM to SECAM	V_{6-1}	8,9	9,2	9,5	V
Colour 'ON' to colour 'OFF' hysteresis	non-SECAM to SECAM	V_{6-1}	0,5	0,8	1,0	V
Voltage at pin 10	during non-SECAM	V_{10-1}	–	1,6	0,5	V
Voltage at pin 10	during SECAM	V_{10-1}	2,1	2,6	3,1	V
Output impedance at pin 10	during SECAM	$\lvert Z_{10-1}\rvert$	1,35	1,60	1,85	kΩ

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Sandcastle detector and clamp pulse generator	pin 7					
Frame blanking detection level		V_{7-1}	1,0	1,5	2,0	V
Line blanking detection level		V_{7-1}	3,0	3,5	4,0	V
Burst gate detection level		V_{7-1}	6,5	7,0	7,5	V
Input current	V_{7-1} = 0,7 V	I_7	–	–30	–100	μA
Pulse width	see Fig. 3 pulse A		1,85	2,35	2,85	μs
Required pulse width	note 5, see Fig. 3 pulse B		0,6	–	–	μs

Notes to the characteristics

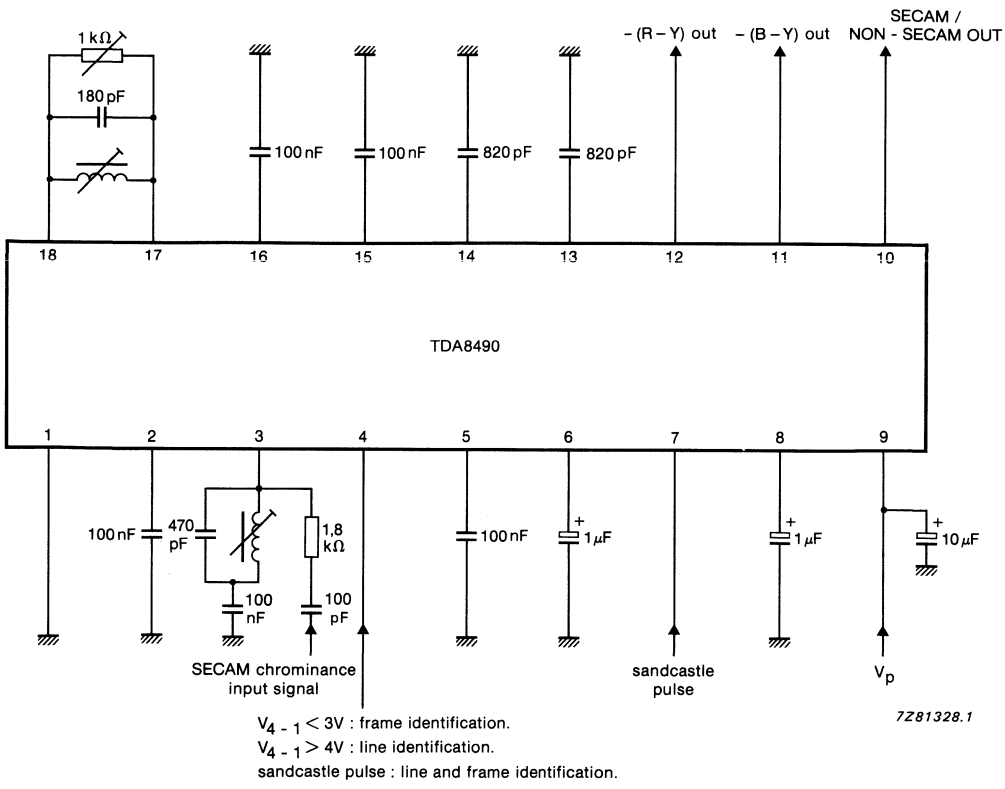
1. For alignment of the reference tuned circuit the input signal on pin 3 must be a SECAM signal at 100 mV(p-p) without deviation during a red and a blue line (black colour information, SECAM). The reference tuned circuit must be aligned to generate a colour output which corresponds to the new reinserted black level information.
2. If the input signal of the limiter is changed from 300 mV(p-p) to 15 mV(p-p), the zero point of the chrominance FM demodulator (f_o is typically 4,33 MHz) will typically shift by 5 kHz.
3. Definition of R-Y linearity = $V_{out\ cyan}/V_{out\ red}$:
   - $f_{nom\ cyan}$ = 4,68 MHz
   - $f_{nom\ red}$ = 4,12 MHz
4. Definition of B-Y linearity = $V_{out\ yellow}/V_{out\ blue}$:
   - $f_{nom\ yellow}$ = 4,02 MHz
   - $f_{nom\ blue}$ = 4,48 MHz
5. The burst gate pulse width must be larger than (2,85 + 0,6)=3,45 μs.
6. Demodulated black level at temperature X = A and at temperature Y = B.
   Artifical black level at temperature X = C and at temperature Y = D.
   Demodulated output signal ($f_o - \Delta f$) at temperature X = E1 and at temperature Y = F1.
   Demodulated output signal ($f_o + \Delta f$) at temperature X = E2 and at temperature Y = F2.

   $$E = \frac{E1 - E2}{2} \text{ and } F = \frac{F1 - F2}{2}$$

   $$\text{specification result} = \frac{(B\text{-}D)/F - (A\text{-}C)/E}{Y\text{-}X} \times \Delta f\ (kHz)/^{o}C)$$

   for B-Y $f_o = f_{ob}$ = 4,25 MHz and Δf = 230 kHz.
   for R-Y $f_o = f_{or}$ = 4,40625 MHz and Δf = 280 kHz.
7. Due to different deviations (230 or 280 kHz) and correction figures (1,9 or 1,5 x) the total B-Y signal path needs a gain, which is 1,55 x higher than the R-Y path.

APPLICATION INFORMATION



$V_{4-1} < 3V$: frame identification.
$V_{4-1} > 4V$: line identification.
sandcastle pulse : line and frame identification.

Fig. 6 Application diagram.

DEVELOPMENT DATA

VIDEO PROCESSOR AND INPUT SELECTOR

GENERAL DESCRIPTION

The TDA9045 is a monolithic integrated circuit for video signal processing and input selection.

FEATURES

- Selection stage for three different inputs
- 4 dB amplifier
- Constant output signal amplifier controlled by synchronizing level and peak white level
- Clamping stage for a constant black level
- Circuit for stopping clamping pulses during the sync pulses
- Emitter follower output stage

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	–	12	–	V
Supply current		I_P	–	60	–	mA
Pre-amplifier						
Composite colour video input signals (peak-to-peak value)		$V_{2, 3, 4-11(p-p)}$	–	–	2	V
AGC amplifier						
Composite video signal (peak-to-peak value)	±6 dB	$V_{12-11(p-p)}$	–	0,4	–	V
Sync level detector						
Threshold voltage for sync level control		V_{9-11}	–	1,8	–	V
Selection						
active input pin 2		V_{1-11}	–	5	–	V
		V_{15-11}	–	5	–	V
active input pin 3		V_{1-11}	0	–	–	V
		V_{15-11}	–	5	–	V
active input pin 4		V_{1-11}	0	–	–	V
		V_{15-11}	0	–	–	V
Not allowed condition		V_{1-11}	–	5	–	V
		V_{15-11}	–	0	–	V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

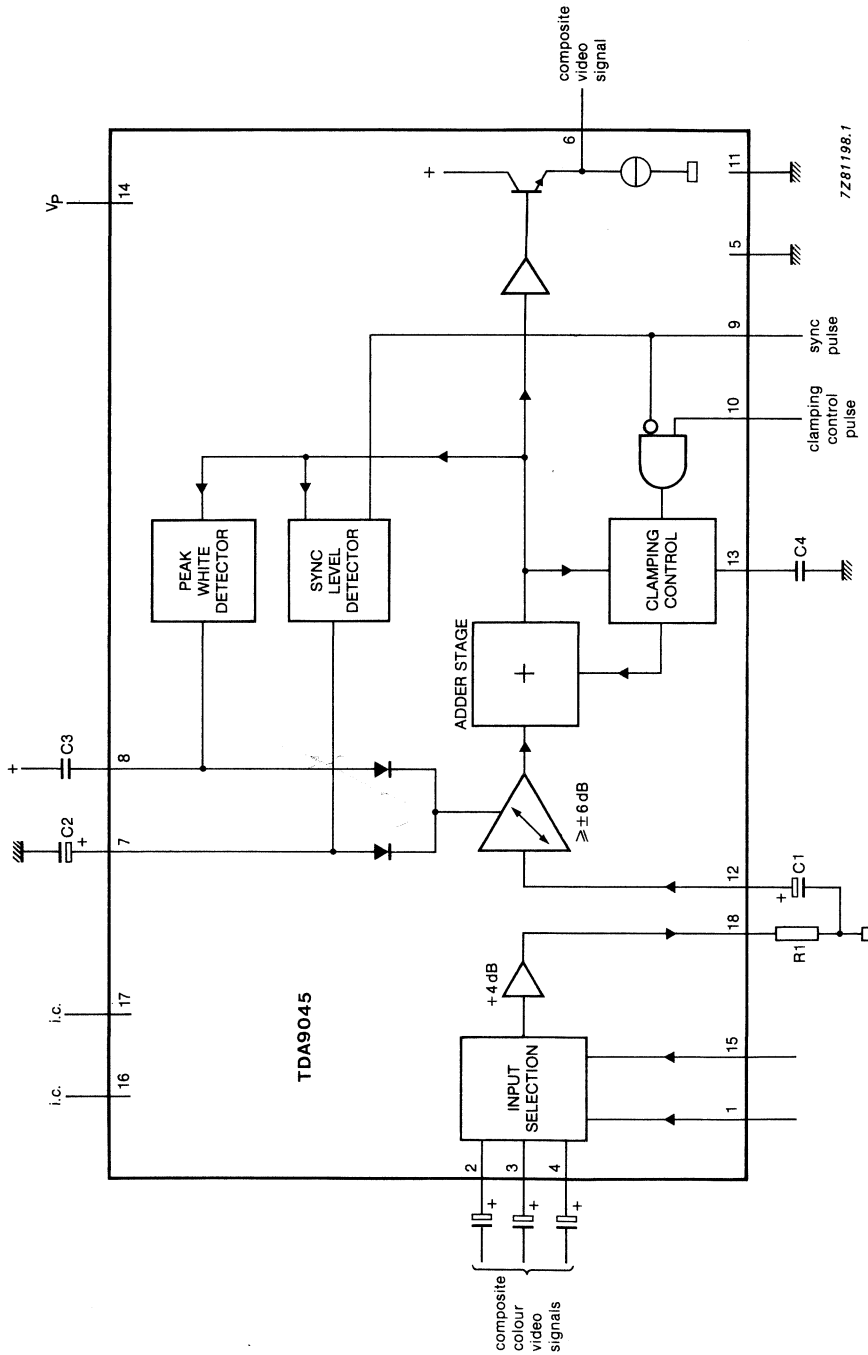


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_P	0	13,2	V
Voltage on pins 9, 10, 12 to pin 11 (GND)		$V_{n\text{-}11}$	0	V_P	V
Voltage readings		$V_{2, 3, 4\text{-}11}$	0	0,8 V_P	V
		$V_{7, 8\text{-}11}$	0,7 V_P	V_P	V
		$V_{13\text{-}11}$	0,25 V_P	V_P	V
		$V_{1, 15\text{-}11}$	0	5,5	V
Current readings		I_6	–	10	mA
		I_{18}	–	20	mA
Total power dissipation		P_{tot}	–	1	W
Storage temperature range		T_{stg}	−25	+150	°C
Operating ambient temperature range		T_{amb}	0	+70	°C

DEVELOPMENT DATA

CHARACTERISTICS

$V_P = V_{14\text{-}11} = 12$ V; trigger pulse width pin 10 = 4 μs; $T_{amb} = 25$ °C; measured in test circuit Fig. 2 unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	9,6	–	13,2	V
Supply current		I_P	–	60	–	mA
Input channel selector						
Input resistance		$R_{1\text{-}11}$	–	7,5	–	kΩ
Selector switching voltage						
select input pin 4		$V_{1\text{-}11}$	0	–	1	V
		$V_{15\text{-}11}$	0	–	1	V
select input pin 3		$V_{1\text{-}11}$	0	–	1	V
		$V_{15\text{-}11}$	2,5	5	5,5	V
select input pin 2		$V_{1\text{-}11}$	2,5	5	5,5	V
		$V_{15\text{-}11}$	2,5	5	5,5	V

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Pre-amplifier						
Composite colour video input signals (peak-to-peak value)		$V_{2,3,4\text{-}11(p\text{-}p)}$	–	1	2,0	V
Input resistance		$R_{2,3,4\text{-}11}$	–	10	–	kΩ
Input capacity		$C_{2,3,4\text{-}11}$	–	10	–	pF
Amplification		$A_{18\text{-}2,3,4}$	–	4	–	dB
DC output voltage		$V_{18\text{-}11}$	–	5,8	6,4	V
Frequency response	0 to 7 MHz		–	–	±2	dB
Signal suppression at output	pin 18 with no input		50	–	–	dB
AGC amplifier						
Input voltage composite video signal (peak-to-peak value)	± 6 dB	$V_{2,3,4\text{-}11(p\text{-}p)}$	–	0,4	–	V
Input resistance		$R_{12\text{-}11}$	–	10	–	kΩ
Input capacity		$C_{12\text{-}11}$	–	10	–	pF
Frequency response	0 to 7 MHz		–	–	±2	dB
Peak white and sync pulse level detectors						
capacitor current charging current		$-I_8$	–	15	–	mA
discharging current		I_8	–	0,8	–	μA
charging current		$-I_7$	–	0,3	–	mA
discharging current		I_7	–	0,3	–	mA
Threshold voltage for sync level controls		$V_{9\text{-}11}$	1	1,8	2,4	V
Input current		$-I_{9\text{-}11}$	–	–	50	μA
Clamping control triggering and sync pulse regeneration						
Threshold voltage for clamping control ON	$V_{9\text{-}11}$ = 0 V	$V_{10\text{-}11}$	1	1,8	2,4	V
Input current		$-I_{10\text{-}11}$	–	–	50	μA
Charging current		$-I_{13}$	–	0,3	–	mA
Discharging current		I_{13}	–	0,3	–	mA
Black level voltage		$V_{6\text{-}11}$	5,2	5,6	6	V
Controlled output signal (peak-to-peak value)		$V_{6\text{-}11(p\text{-}p)}$	3,7	3,9	4,1	V

DEVELOPMENT DATA

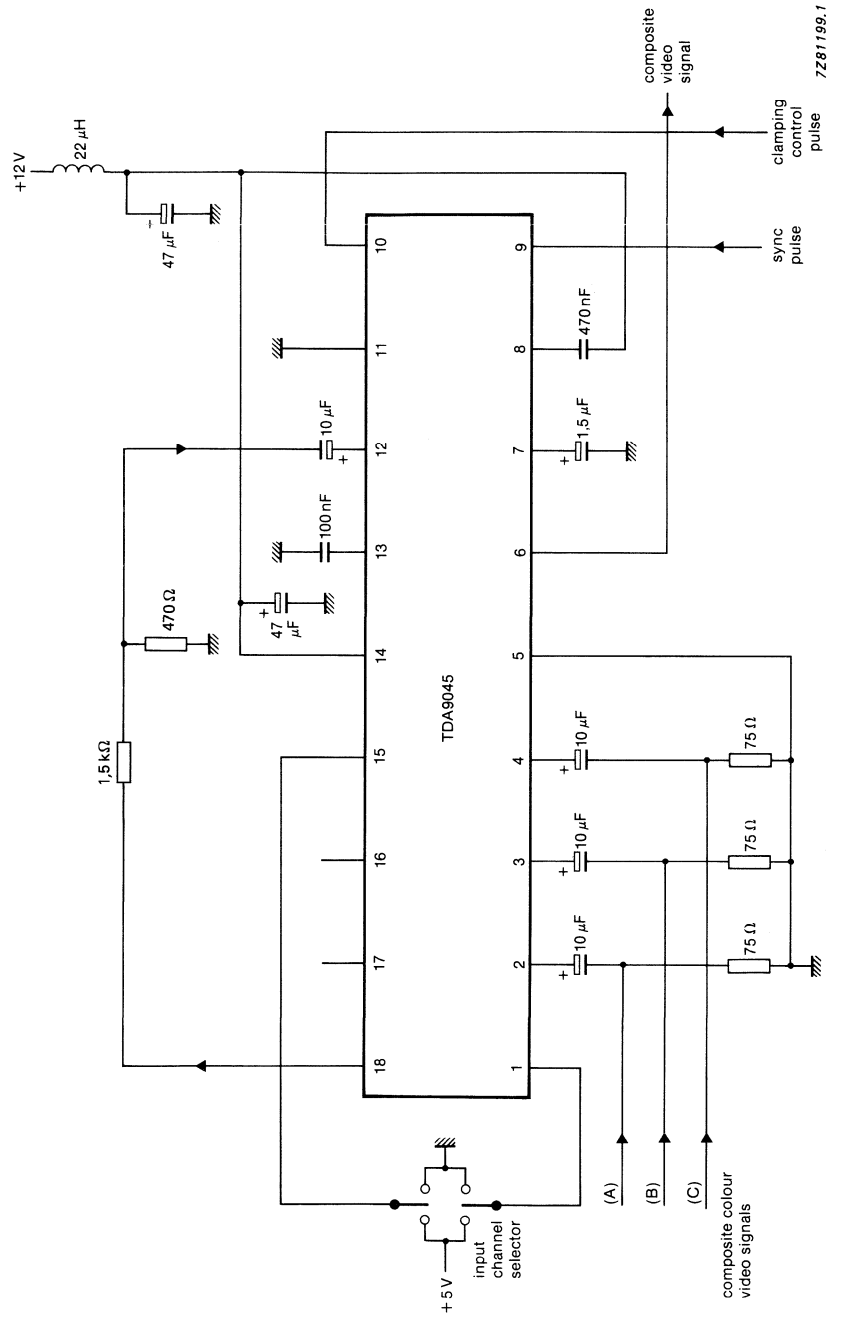


Fig. 2 Application diagram; also used as test circuit.

VIDEO CONTROL COMBINATION CIRCUIT

WITH AUTOMATIC CUT-OFF CONTROL

GENERAL DESCRIPTION

The TDA9080 is an integrated circuit which performs video control functions in a PAL/SECAM decoder.

The required input signals are: luminance and negative colour difference −(R−Y) and −(B−Y), and a 2-level sandcastle pulse for control purposes. Linear RGB signals can be inserted from an external source. RGB output signals are available for driving the video output stages. This circuit provides automatic cut-off control of the picture tube.

Features

- Capacitive coupling of the colour difference and luminance input signals with black level clamping in the input stages
- Linear saturation control acting on the colour difference signals
- (G−Y) and RGB matrix
- Linear transmission of inserted signals
- Equal black levels for inserted and matrixed signals
- 3 identical channels for the RGB signals
- Linear contrast and brightness controls, operating on both the inserted and matrixed RGB signals
- Peak beam current limiting input
- Clamping, horizontal and vertical blanking of the three input signals controlled by a 2-level sandcastle pulse
- 3 DC gain controls for the RGB output signals (white point adjustment)
- Emitter-follower outputs for driving the RGB output stages
- Input for automatic cut-off control with compensation for leakage current of the picture tube

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 6)		$V_P = V_{6-24}$	–	12	–	V
Supply current		$I_P = I_6$	–	100	–	mA
Composite video input signal (peak-to-peak value)		$V_{15-24(p-p)}$	–	0.45	–	V
Colour difference input signals (peak-to-peak value)						
–(B–Y)		$V_{18-24(p-p)}$	–	1.33	–	V
–(R–Y)		$V_{17-24(p-p)}$	–	1.05	–	V
Inserted RGB signals (black-to-white value)		$V_{12,13,14-24}$	–	1.0	–	V
Two-level sandcastle pulse		V_{10-24}	–	2.5	–	V
			–	4.5	–	V
Control voltage ranges						
brightness		V_{20-24}	1.0	–	3.0	V
contrast		V_{19-24}	2.0	–	4.3	V
saturation		V_{16-24}	2.0	–	4.3	V

DEVELOPMENT DATA

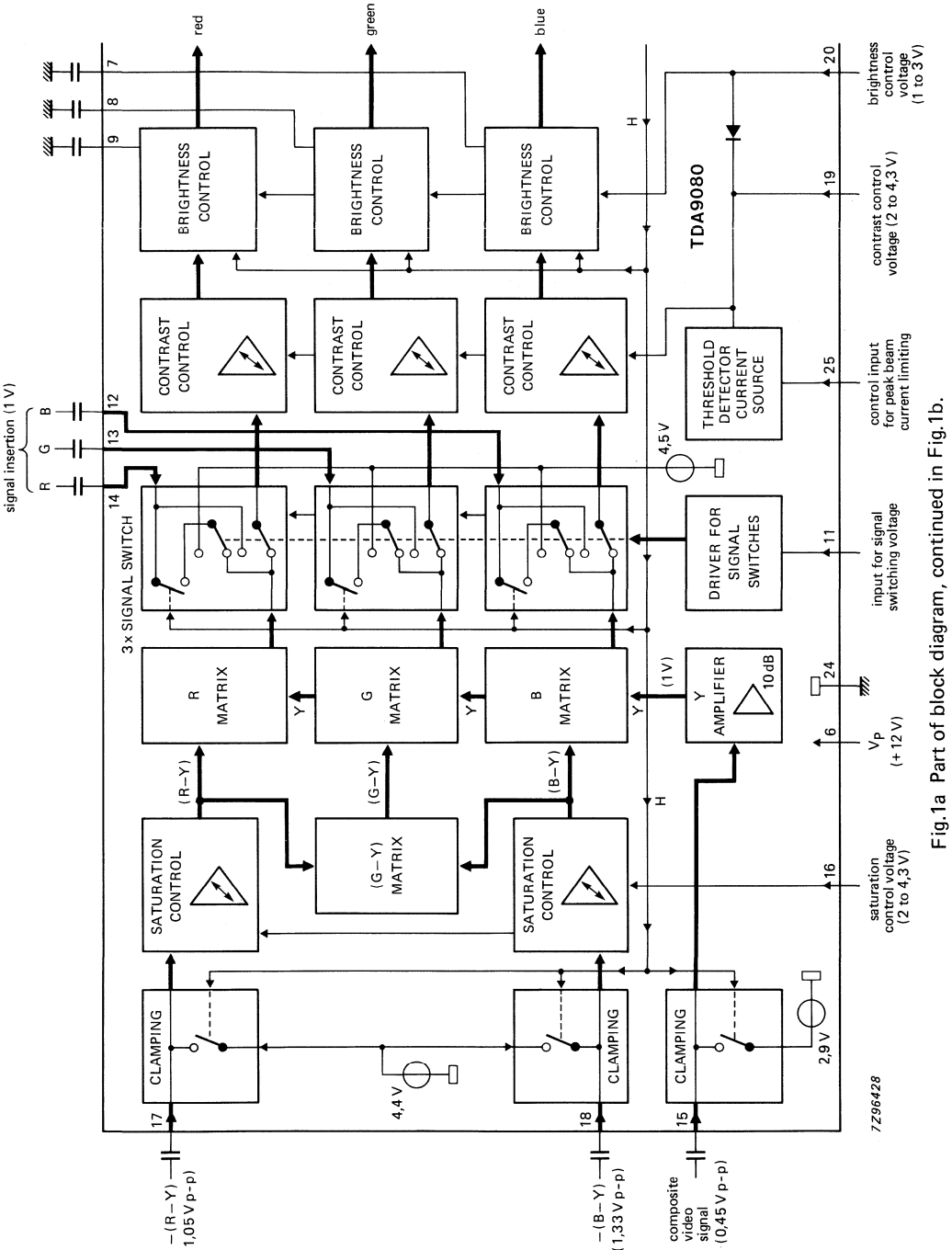


Fig.1a Part of block diagram, continued in Fig.1b.

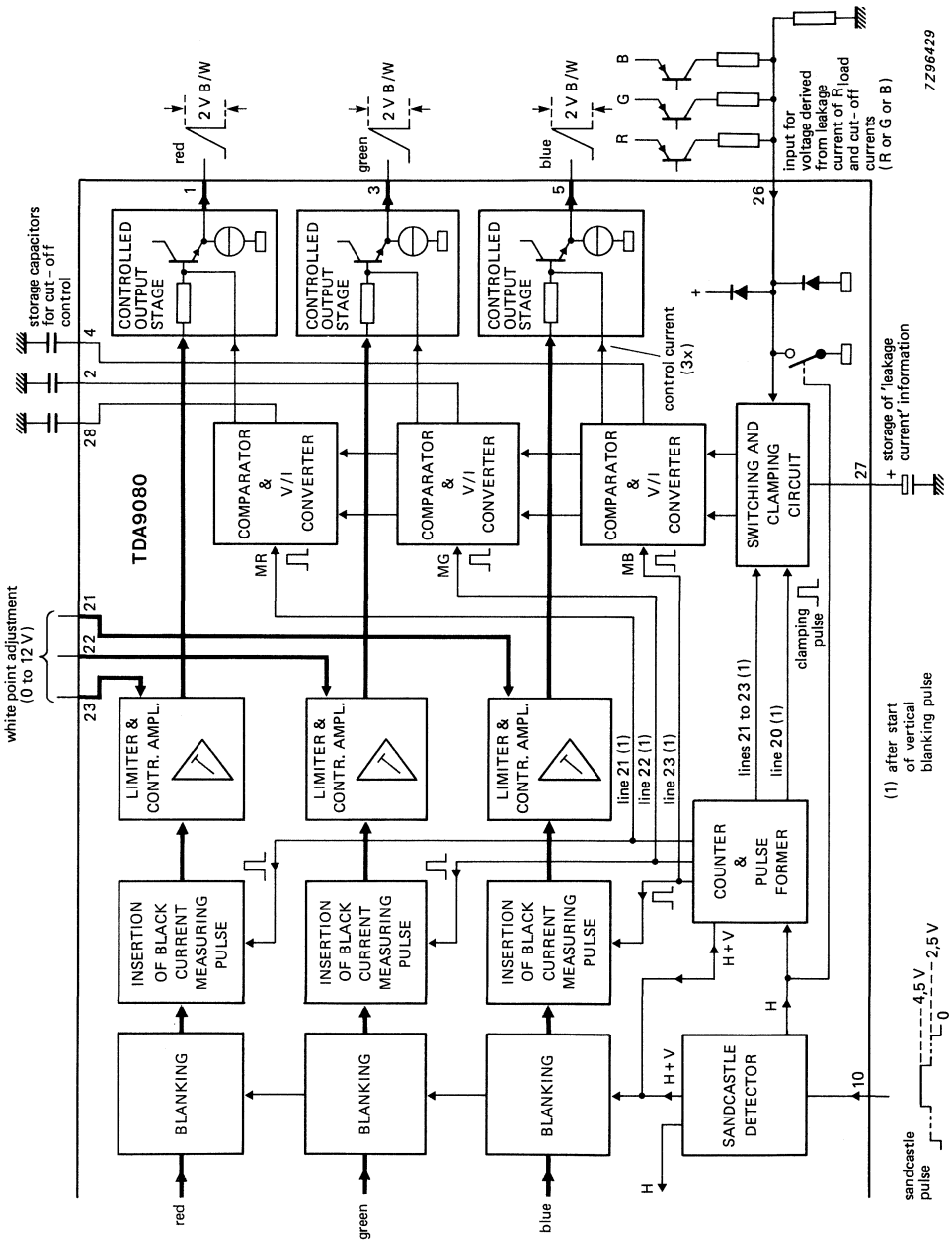


Fig.1b Part of block diagram, continued from Fig.1a.

DEVELOPMENT DATA

PINNING

pin	description
1	red output
2	green storage capacitor for cut-off control
3	green output
4	blue storage capacitor for cut-off control
5	blue output
6	positive supply voltage (+12 V)
7	blue storage for brightness
8	green storage for brightness
9	red storage for brightness
10	sandcastle pulse input
11	fast switch for RGB inputs
12	blue input (external signal)
13	green input (external signal)
14	red input (external signal)
15	luminance input
16	saturation control input
17	−(R−Y) colour difference input
18	−(B−Y) colour difference input
19	contrast control input
20	brightness control input
21	white point adjustment, blue
22	white point adjustment, green
23	white point adjustment, red
24	ground (0 V)
25	control input for peak beam current limiting
26	automatic cut-off control input
27	storage capacitor for leakage current
28	red storage capacitor for cut-off control

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 6)	$V_P = V_{6-24}$	–	13.2	V
Voltage ranges				
at pins 10, 21, 22, 23, 25, 26	V_{n-24}	0	V_P	V
at pin 11	V_{11-24}	−0.5	3.0	V
at pins 16, 19, 20	$V_{16,19,20-24}$	0	0.5V_P	V
at pins 1, 2, 3, 4, 5, 7, 8, 9, 12, 13, 14, 15, 17, 18, 27, 28	no external DC voltage			
Currents				
at pins 1, 3, 5	$-I_{1,3,5}$	–	3	mA
at pin 19	I_{19}	–	10	mA
at pin 20	I_{20}	–	5	mA
at pin 25	$-I_{25}$	–	5	mA
Total power dissipation	P_{tot}	–	1.7	W
Storage temperature range	T_{stg}	−25	+150	°C
Operating ambient temperature range	T_{amb}	0	+70	°C

CHARACTERISTICS

$V_P = V_{6-24} = 12.0$ V; $V_{12,13,14(p-p)} = 1.0$ V; $V_{15-24(p-p)} = 0.45$ V; $V_{17-24(p-p)} = 1.05$ V; $V_{18-24(p-p)} = 1.33$ V; $T_{amb} = 25\ ^{o}C$; measured in Fig. 2; nominal settings of brightness, contrast, saturation and white point adjustment; all voltages are referred to pin 24; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply (pin 6)						
Supply voltage		$V_P = V_6$	10.8	12.0	13.2	V
Supply current		I_P	–	100	130*	mA
Colour difference inputs (pins 17, 18)						
–(R–Y) input signal (pin 17) (peak-to-peak value)	for saturated colour bar with 75% of maximum amplitude	$V_{17(p-p)}$	–	1.05	1.48	V
–(B–Y) input signal (pin 18) (peak-to-peak value)	for saturated colour bar with 75% of maximum amplitude	$V_{18(p-p)}$	–	1.33	1.88	V
Input current during scanning		$I_{17,18}$	–	–	1.0	μA
Input resistance		$R_{17,18-24}$	1.0	–	–	MΩ
Internal DC voltage due to clamping	note 1	$V_{17,18}$	3.8	4.4	4.8	V
Saturation control (pin 16)						
Control voltage for maximum saturation	note 1	V_{16}	4.0	4.2	4.4	V
Control voltage for nominal saturation	6 dB below max. note 1	V_{16}	2.9	3.1	3.3	V
Control voltage for –26 dB saturation referred to maximum	note 1	V_{16}	1.9	2.1	2.3	V
Minimum saturation	$V_{16} = 1.8$ V	d	46	50	–	dB
Input current		I_{16}	–	–	20	μA
(G–Y) matrix						
Matrixed according to the equation $V_{(G-Y)} = -0{,}51\ V_{(R-Y)} - 0{,}19\ V_{(B-Y)}$						
Luminance input (pin 15)						
Composite video input signal (peak-to-peak value)		$V_{15(p-p)}$	–	450	630	mV
Input resistance		R_{15-24}	100	–	–	kΩ
Input capacitance		C_{15-24}	–	–	5	pF

* $<$ 115 mA after warm-up

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Luminance input (continued)						
Input current during scanning		I_{15}	–	–	1	μA
Linearity	nominal settings	m	0.85	–	–	
Internal DC voltage due to clamping	note 1	V_{15}	2.5	2.9	3.3	V
RGB channels						
Signal switching input (pin 11)						
Normal state; no insertion		V_{11}	0	–	0.4	V
Level for insertion-on		V_{11}	0.9	–	3.0	V
Input capacitance		$C_{11\text{-}24}$	–	–	10	pF
Input current	V_{11} = 0 to 3 V	I_{11}	−100	–	+450	μA
Signal insertion (pins 12, 13, 14)						
External RGB input signals (black-to-white value)		$V_{12,13,14}$	–	1.0	1.4	V
Input current during scanning		$I_{12,13,14}$	–	–	1.0	μA
Internal DC voltage due to clamping	notes 1, 2	$V_{12,13,14}$	4.0	4.5	5.0	V
Contrast control (pin 19)	note 1					
Control voltage for maximum contrast		V_{19}	4.0	4.2	4.4	V
Control voltage for nominal contrast	3 dB below max.	V_{19}	3.4	3.6	3.8	V
Control voltage for −10 dB below max.		V_{19}	2.6	2.8	3.0	V
Minimum contrast referred to max.	V_{19} = 2 V	d	18	21	29	dB
Input current	$V_{25} > 6$ V	I_{19}	–	–	2	μA
Difference between RGB channels	contrast −10 dB below max.		–	–	0.6	dB
Peak beam current limiting (pin 25)						
Internal DC bias voltage	note 1	V_{25}	5.3	5.5	5.7	V
Input resistance		$R_{25\text{-}24}$	–	10	–	kΩ
Input current at contrast control input	V_{25} = 4.5 V	I_{19}	10	20	34	mA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Brightness control (pin 20)	note 1					
Control voltage range		V_{20}	1	–	3	V
Input current		$-I_{20}$	–	–	10	μA
Change of black level in the control range related to the luminance signal (black/white)	ΔV_{20} = 1 V		–	±50	–	%
Tracking			95	–	–	%
Internal signal limiting (RGB)						
Signal limiting referred to nominal luminance and nominal black level						
black			–	–25	–	%
white			115	120	125	%
White point adjustment (pins 21, 22, 23)	note 1					
AC voltage gain	note 3					
$V_{21,22,23}$ = 5.5 V		G_V	–	100	–	%
$V_{21,22,23}$ = 0 V		G_V	–35	–40	–	%
$V_{21,22,23}$ = 12 V		G_V	+35	+40	–	%
Input resistance		$R_{21,22,23\text{-}24}$	–	20	–	kΩ
RGB outputs (emitter follower) (pins 1, 3, 5)						
Output voltage; black-to-white positive		$V_{1,3,5}$	1.5	2.0	2.5	V
Black level without automatic cut-off control	note 1; $V_{28,2,4}$ = 10 V	$V_{1,3,5}$	6.1	6.9	7.7	V
Difference in black level between RGB channels due to variation of contrast control		$\Delta V_{1,3,5}$	–	–	10	mV
Cut-off control range	note 1	$V_{1,3,5}$	4.0	4.6	–	V
Internal current source		$I_{1,3,5}$	2.0	3.0	–	mA

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Automatic cut-off control (pin 26)	notes 1, 4					
Input voltage range		V_{26}	0	–	6.5	V
Voltage difference between cut-off current measurement (note 5) and leakage current measurement (note 6)		V_{26}	0.5	0.64	0.72	V
Input pin 26 switches to ground during horizontal flyback						
Gain data	at nominal brightness, contrast, saturation and white point settings					
Voltage gain with respect to luminance input (pin 15)		$G_{1,3,5\text{-}15}$	14	16	18	dB
Frequency response of luminance path	0 to 10 MHz	$d_{1,3,5\text{-}15}$	–	–	3	dB
Voltage gain with respect to colour difference inputs (pins 17 and 18)		$G_{5\text{-}18}$ $G_{1\text{-}17}$	3	6	9	dB
Frequency response of colour difference paths	0 to 4 MHz	$d_{5\text{-}18}$ $d_{1\text{-}17}$	–	–	3	dB
Voltage gain with respect to inserted signals		$G_{1\text{-}14}$ $G_{3\text{-}13}$ $G_{5\text{-}12}$	4	6	8	dB
Frequency response of inserted signal paths	0 to 10 MHz	$d_{1\text{-}14}$ $d_{3\text{-}13}$ $d_{5\text{-}12}$	–	–	3	dB
Rise and fall times of RGB output signals (pins 1, 3, 5)		t_r, t_f	–	40	–	ns
Difference in transit times between R, G and B channels		$\Delta t_{1,3,5}$	–	0	15	ns
Delay time between signal switching and signal insertion		t_d	–25	–	+25	ns
Difference in gain between normal mode and signal insertion mode		$\Delta G_{1,3,5}$	–	–	10	%

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Sandcastle pulse detector (pin 10)	note 7					
Levels for separating the following pulses:						
horizontal and vertical blanking pulses	note 8	V_{10}	1.0	1.5	2.0	V
required pulses (H + V)		V_{10}	2.1	2.5	2.9	V
horizontal pulses		V_{10}	3.0	3.5	4.0	V
required pulses (H)		V_{10}	4.1	–	5.0	V
no keying		V_{10}	–	–	1.0	V
Input current		$-I_{10}$	–	–	110	μA

Notes to the characteristics

1. Values are proportional to the supply voltage.
2. When $V_{11\text{-}24} < 0.4$ V during clamping time – the black levels of the inserted RGB signals are clamped on the black levels of the internal RGB signals.

   When $V_{11\text{-}24} > 0.9$ V during clamping time – the black levels of the inserted RGB signals are clamped on an internal DC voltage (correct clamping of the external RGB signals is possible only when they are synchronous with the sandcastle pulse).
3. When pins 21, 22 and 23 are not connected, an internal bias voltage of 5.5 V is supplied.
4. Automatic cut-off control measurement occurs in the following lines after start of the vertical blanking pulse:

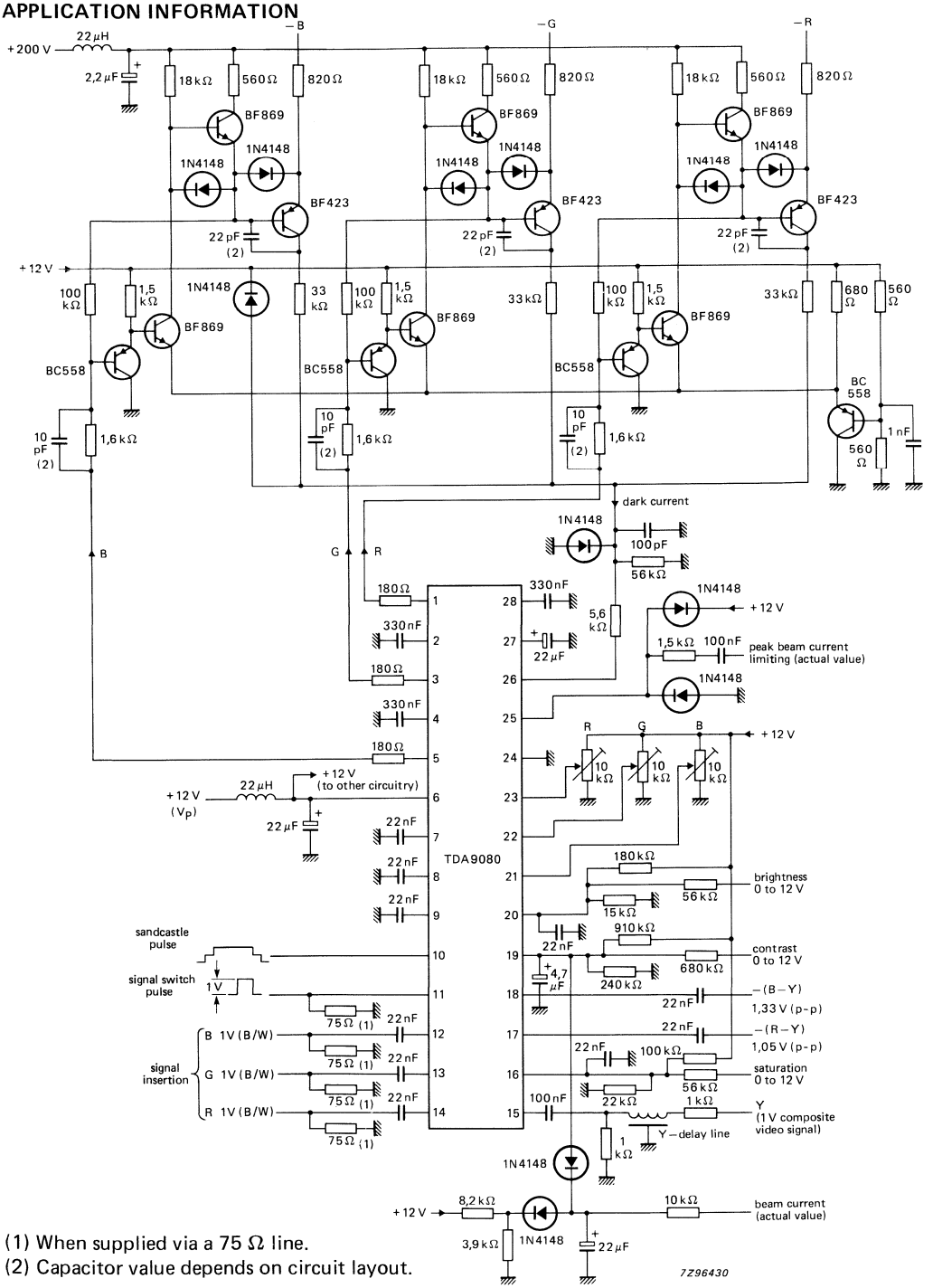
   line 20: measurement of leakage current (R + G + B)
   line 21: measurement of red cut-off current
   line 22: measurement of green cut-off current
   line 23: measurement of blue cut-off current
5. Black level of the measured channel is nominal; the other two channels are blanked to ultra-black.
6. All three channels blanked to ultra-black.

   The cut-off control cycle occurs when the vertical blanking part of the sandcastle pulse contains more than 3 line pulses.

   The internal blanking continues until the end of the last measured line.

   The vertical blanking pulse is not allowed to contain more than 34 line pulses, otherwise another control cycle begins.
7. The sandcastle pulse is compared with two internal thresholds (proportional to Vp) and the given levels separate the various pulses.
8. Blanked to ultra-black (–25%).

APPLICATION INFORMATION



(1) When supplied via a 75 Ω line.
(2) Capacitor value depends on circuit layout.

Fig.2 Typical application circuit diagram using the TDA9080.

DEVELOPMENT DATA

CONTROL CIRCUIT FOR SMPS

GENERAL DESCRIPTION

The TEA1039 is a bipolar integrated circuit intended for the control of a switched-mode power supply. Together with an external error amplifier and a voltage regulator (e.g. a regulator diode) it forms a complete control system. The circuit is capable of directly driving the SMPS power transistor in small SMPS systems.

Features

- Suited for frequency and duty factor regulation.
- Suited for flyback converters and forward converters.
- Wide frequency range.
- Adjustable input sensitivity.
- Adjustable minimum frequency or maximum duty factor limit.
- Adjustable overcurrent protection limit.
- Supply voltage out-of-range protection.
- Slow-start facility.

QUICK REFERENCE DATA

Supply voltage	V_{CC}	nom.	14 V
Supply current	I_{CC}	max.	13 mA
Output pulse repetition frequency range	f_o	1 Hz to	100 kHz
Output current LOW	I_{OL}	max.	1 A
Operating ambient temperature range	T_{amb}	−25 to +	125 °C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

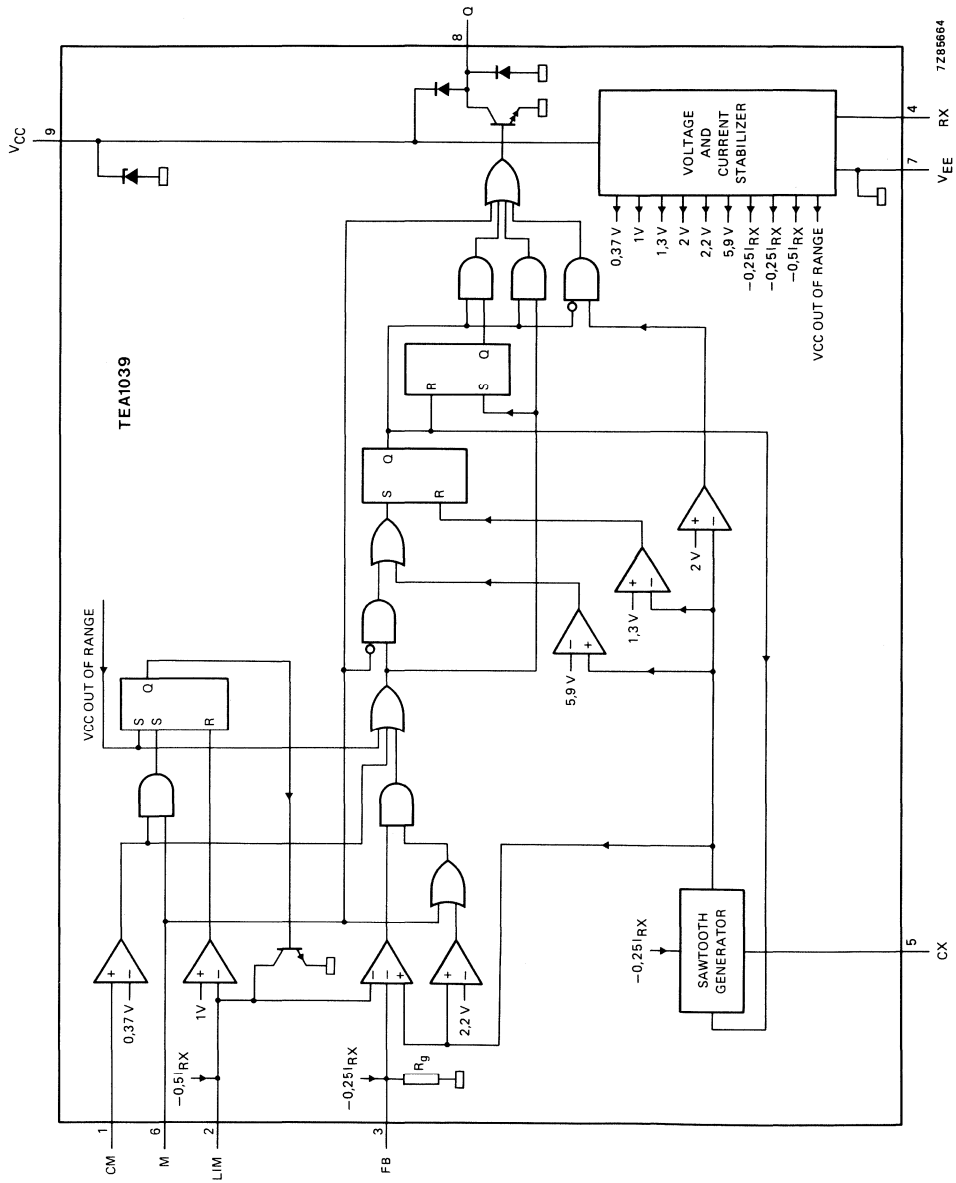


Fig. 1 Block diagram.

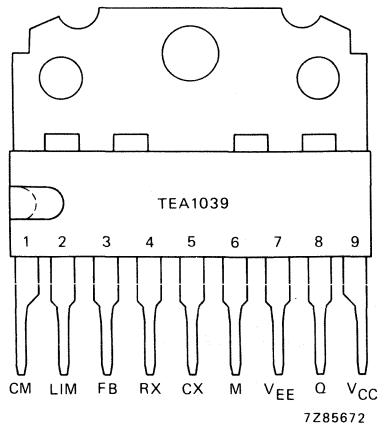


Fig. 2 Pinning diagram.

PINNING

1	CM	overcurrent protection input
2	LIM	limit setting input
3	FB	feedback input
4	RX	external resistor connection
5	CX	external capacitor connection
6	M	mode input
7	V_{EE}	common
8	Q	output
9	V_{CC}	positive supply connection

FUNCTIONAL DESCRIPTION

The TEA1039 produces pulses to drive the transistor in a switched-mode power supply. These pulses may be varied either in frequency (frequency regulation mode) or in width (duty factor regulation mode).

The usual arrangement is such that the transistor in the SMPS is ON when the output of the TEA1039 is HIGH, i.e. when the open-collector output transistor is OFF. The duty factor of the SMPS is the time that the output of the TEA1039 is HIGH divided by the pulse repetition time.

Supply V_{CC} (pin 9)

The circuit is usually supplied from the SMPS that it regulates. It may be supplied either from its primary d.c. voltage or from its output voltage. In the latter case an auxiliary starting supply is necessary.

The circuit has an internal V_{CC} out-of-range protection. In the frequency regulation mode the oscillator is stopped; in the duty factor regulation mode the duty factor is made zero. When the supply voltage returns within its range, the circuit is started with the slow-start procedure.

When the circuit is supplied from the SMPS itself, the out-of-range protection also provides an effective protection against any interruption in the feedback loop.

Mode input M (pin 6)

The circuit works in the frequency regulation mode when the mode input M is connected to ground (V_{EE}, pin 7). In this mode the circuit produces output pulses of a constant width but with a variable pulse repetition time.

The circuit works in the duty factor regulation mode when the mode input M is left open. In this mode the circuit produces output pulses with a variable width but with a constant pulse repetition time.

FUNCTIONAL DESCRIPTION (continued)

Oscillator resistor and capacitor connections RX and CX (pins 4 and 5)

The output pulse repetition frequency is set by an oscillator whose frequency is determined by an external capacitor C5 connected between the CX connection (pin 5) and ground (V_{EE}, pin 7), and an external resistor R_4 connected between the RX connection (pin 4) and ground. The capacitor C5 is charged by an internal current source, whose current level is determined by the resistor R4. In the frequency regulation mode these two external components determine the minimum frequency; in the duty factor regulation mode they determine the working frequency (see Fig. 4). The output pulse repetition frequency varies less than 1% with the supply voltage over the supply voltage range.

In the frequency regulation mode the output is LOW from the start of the cycle until the voltage on the capacitor reaches 2 V. The capacitor is further charged until its voltage reaches the voltage on either the feedback input FB or the limit setting input LIM, provided it has exceeded 2,2 V. As soon as the capacitor voltage reaches 5,9 V the capacitor is discharged rapidly to 1,3 V and a new cycle is initiated (see Figs 5 and 6).

For voltages on the FB and LIM inputs lower than 2,2 V, the capacitor is charged until this voltage is reached; this sets an internal maximum frequency limit.

In the duty factor regulation mode the capacitor is charged from 1,3 V to 5,9 V and discharged again at a constant rate. The output is HIGH until the voltage on the capacitor exceeds the voltage on the feedback input FB; it becomes HIGH again after discharge of the capacitor (see Figs 7 and 8). An internal maximum limit is set to the duty factor of the SMPS by the discharging time of the capacitor.

Feedback input FB (pin 3)

The feedback input compares the input current with an internal current source whose current level is set by the external resistor R4. In the frequency regulation mode, the higher the voltage on the FB input, the longer the external capacitor C5 is charged, and the lower the frequency will be. In the duty factor regulation mode external capacitor C5 is charged and discharged at a constant rate, the voltage on the FB input now determines the moment that the output will become LOW. The higher the voltage on the FB input, the longer the output remains HIGH, and the higher the duty factor of the SMPS.

Limit setting input LIM (pin 2)

In the frequency regulation mode this input sets the minimum frequency, in the duty factor regulation mode it sets the maximum duty factor of the SMPS. The limit is set by an external resistor R2 connected from the LIM input to ground (pin 7) and by an internal current source, whose current level is determined by external resistor R4.

A slow-start procedure is obtained by connecting a capacitor between the LIM input and ground. In the frequency regulation mode the frequency slowly decreases from f_{max} to the working frequency. In the duty factor regulation mode the duty factor slowly increases from zero to the working duty factor.

Overcurrent protection input CM (pin 1)

A voltage on the CM input exceeding 0,37 V causes an immediate termination of the output pulse. In the duty factor regulation mode the circuit starts again with the slow-start procedure.

Output Q (pin 8)

The output is an open-collector n-p-n transistor, only capable of sinking current. It requires an external resistor to drive an n-p-n transistor in the SMPS (see Figs 9 and 10).

The output is protected by two diodes, one to ground and one to the supply.

At high output currents the dissipation in the output transistor may necessitate a heatsink. See the power derating curve (Fig. 3).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range, voltage source	V_{CC}	−0,3 to +20	V
Supply current range, current source	I_{CC}	−30 to +30	mA
Input voltage range, all inputs	V_I	−0,3 to +6	V
Input current range, all inputs	I_I	−5 to +5	mA
Output voltage range	V_{8-7}	−0,3 to +20	V
Output current range			
output transistor ON	I_8	0 to 1	A
output transistor OFF	I_8	−100 to + 50	mA
Storage temperature range	T_{stg}	−55 to +150	°C
Operating ambient temperature range (see Fig. 3)	T_{amb}	−25 to +125	°C
Power dissipation (see Fig. 3)	P_{tot}	max. 2	W

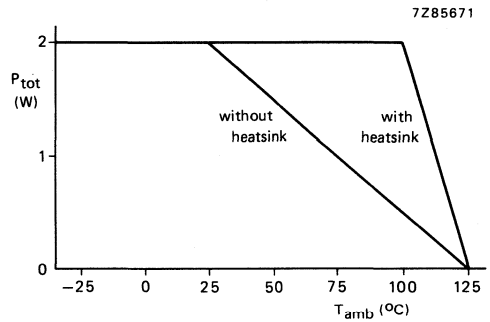


Fig. 3 Power derating curve.

CHARACTERISTICS

V_{CC} = 14 V; T_{amb} = 25 °C unless otherwise specified

	symbol	min.	typ.	max.	unit
Supply V_{CC} (pin 9)					
Supply voltage, operating	V_{CC}	11	14	20	V
Supply current					
at V_{CC} = 11 V	I_{CC}	–	7,5	11	mA
at V_{CC} = 20 V	I_{CC}	–	9	12	mA
variation with temperature	$\frac{\Delta I_{CC}/I_{CC}}{\Delta T}$	–	–0,3	–	%/K
Supply voltage, internally limited					
at I_{CC} = 30 mA	V_{CC}	23,5	–	28,5	V
variation with temperature	$\Delta V_{CC}/\Delta T$	–	18	–	mV/K
Low supply threshold voltage	V_{CCmin}	9	10	11	V
variation with temperature	$\Delta V_{CC}/\Delta T$	–	–5	–	mV/K
High supply threshold voltage	V_{CCmax}	21	23	24,6	V
variation with temperature	$\Delta V_{CC}/\Delta T$	–	10	–	mV/K
Feedback input FB (pin 3)					
Input voltage for duty factor = 0; M input open	V_{3-7}	0	–	0,3	V
Internal reference current	$-I_{FB}$	–	0,5 I_{RX}	–	mA
Internal resistor R_g	R_g	–	130	–	kΩ
Limit setting input LIM (pin 2)					
Threshold voltage	V_{2-7}	–	1	–	V
Internal reference current	$-I_{LIM}$	–	0,25 I_{RX}	–	mA
Overcurrent protection input CM (pin 1)					
Threshold voltage	V_{1-7}	300	370	420	mV
variation with temperature	$\Delta V_{1-7}/\Delta T$	–	0,2	–	mV/K
Propagation delay, CM input to output	t_{PHL}	–	500	–	ns

	symbol	min.	typ.	max.	unit
Oscillator connections RX and CX (pins 4 and 5)					
Voltage at RX connection at $-I_4$ = 0,15 to 1 mA	V_{4-7}	6,2	7,2	8,1	V
variation with temperature	$\Delta V_{4-7}/\Delta T$	–	2,1	–	mV/K
Lower sawtooth level	V_{LS}	–	1,3	–	V
Threshold voltage for output H to L transition in F mode	V_{FT}	–	2	–	V
Threshold voltage for maximum frequency in F mode	V_{FM}	–	2,2	–	V
Higher sawtooth level	V_{HS}	–	5,9	–	V
Internal capacitor charging current, CX connection	$-I_{CX}$	–	0,25 I_{RX}	–	mA
Oscillator frequency (output pulse repetition frequency)	f_o	1	–	10^5	Hz
Minimum frequency in F mode, initial deviation	$\Delta f/f$	−10	–	10	%
variation with temperature	$\frac{\Delta f/f}{\Delta T}$	–	0,034	–	%/K
Maximum frequency in F mode, initial deviation	$\Delta f/f$	−20	–	+20	%
variation with temperature	$\frac{\Delta f/f}{\Delta T}$	–	−0,16	–	%/K
Output LOW time in F mode, initial deviation	$\Delta t/t$	−25	–	+25	%
variation with temperature	$\frac{\Delta t/t}{\Delta T}$	–	0,2	–	%/K
Pulse repetition frequency in D mode, initial deviation	$\Delta f/f$	−10	–	10	%
variation with temperature	$\frac{\Delta f/f}{\Delta T}$	–	0,034	–	%/K
Minimum output LOW time in D mode at C_5 = 3,6 nF	t_{OLmin}	–	1	–	μs
variation with temperature	$\frac{\Delta t/t}{\Delta T}$	–	0,2	–	%/K
Output Q (pin 8)					
Output voltage LOW at I_8 = 100 mA	V_{8-7}	–	0,8	1,2	V
variation with temperature	$\Delta V_{8-7}/\Delta T$	–	1,5	–	mV/K
Output voltage LOW at I_8 = 1 A	V_{8-7}	–	1,7	2,1	V
variation with temperature	$\Delta V_{8-7}/\Delta T$	–	−1,4	–	mV/K

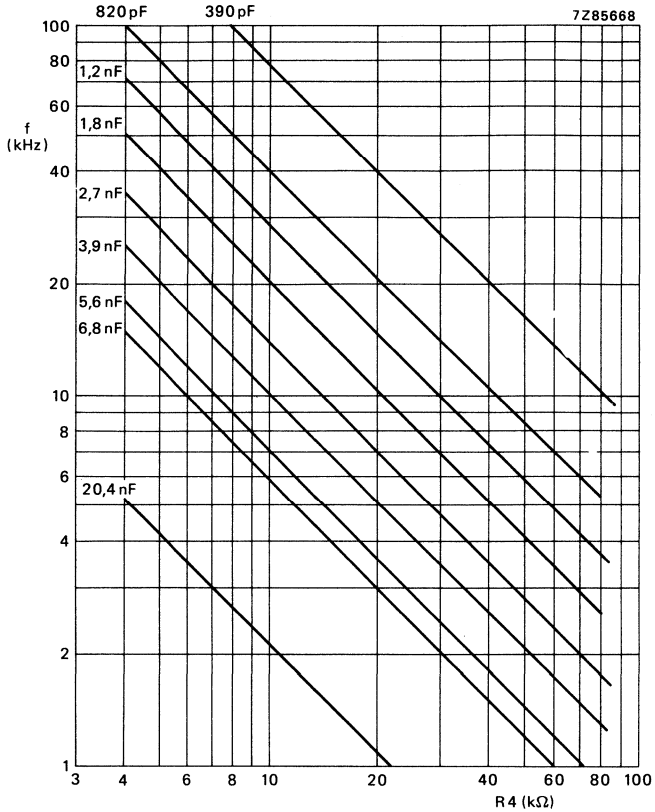


Fig. 4 Minimum pulse repetition frequency in the frequency regulation mode, and working pulse repetition frequency in the duty factor regulation mode, as a function of external resistor R4 connected between RX and ground with external capacitor C5 connected between CX and ground as a parameter.

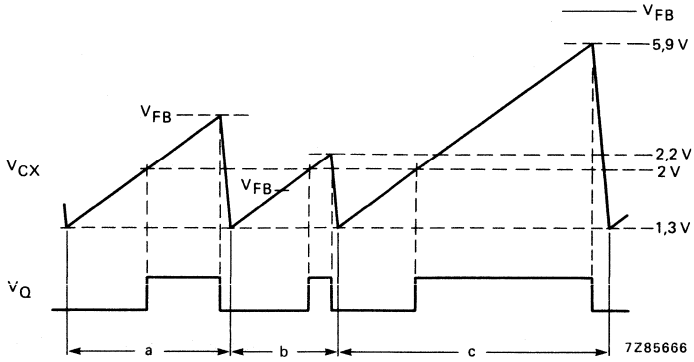


Fig. 5 Timing diagram for the frequency regulation mode showing the voltage on external capacitor C5 connected between CX and ground and the output voltage as a function of time for three combinations of input signals. *a:* The voltages on inputs FB or LIM are between 2,2 V and 5,9 V. The circuit is in its normal regulation mode. *b:* The voltage on input FB or input LIM is lower than 2,2 V. The circuit works at its maximum frequency. *c:* The voltages on inputs FB and LIM are higher than 5,9 V. The circuit works at its minimum frequency.

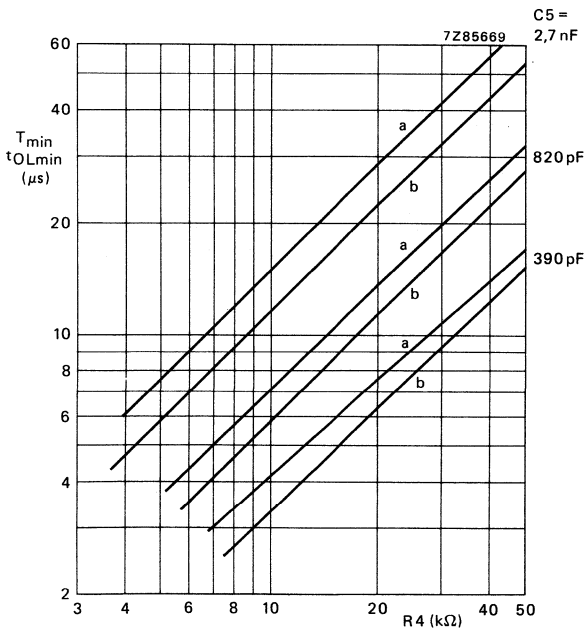


Fig. 6 Minimum output pulse repetition time T_{min} (curves a) and minimum output LOW time t_{OLmin} (curves b) in the frequency regulation mode as a function of external resistor R4 connected between RX and ground with external capacitor C5 connected between CX and ground as a parameter.

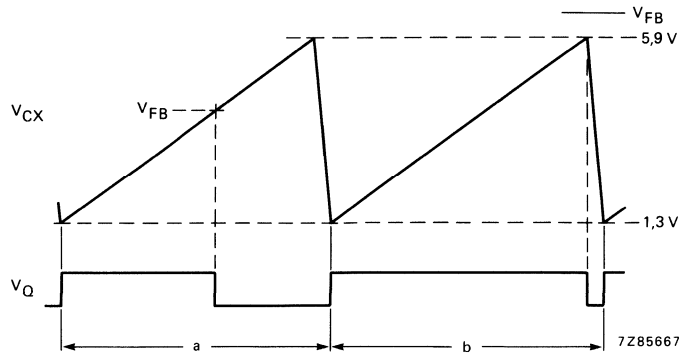


Fig. 7 Timing diagram for the duty factor regulation mode showing the voltage on external capacitor C5 connected between CX and ground and the output voltage as a function of time for two combinations of input signals. *a:* The voltages on inputs FB or LIM are below 5,9 V. The circuit is in its normal regulation range. *b:* The voltages on inputs FB and LIM are higher than 5,9 V. The circuit produces its minimum output LOW time, giving the maximum duty factor of the SMPS.

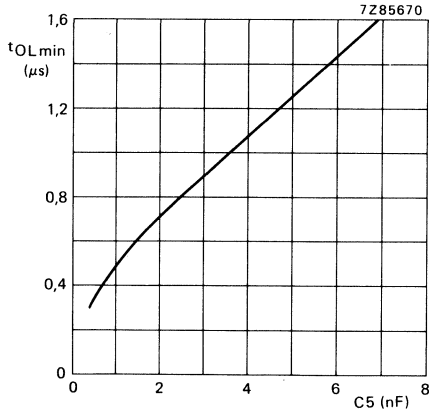


Fig. 8 Minimum output LOW time t_{OLmin} in the duty factor regulation mode as a function of external capacitor C5 connected between CX and ground. In this mode the minimum output LOW time is independent of R4 for values of R4 between 4 kΩ and 80 kΩ.

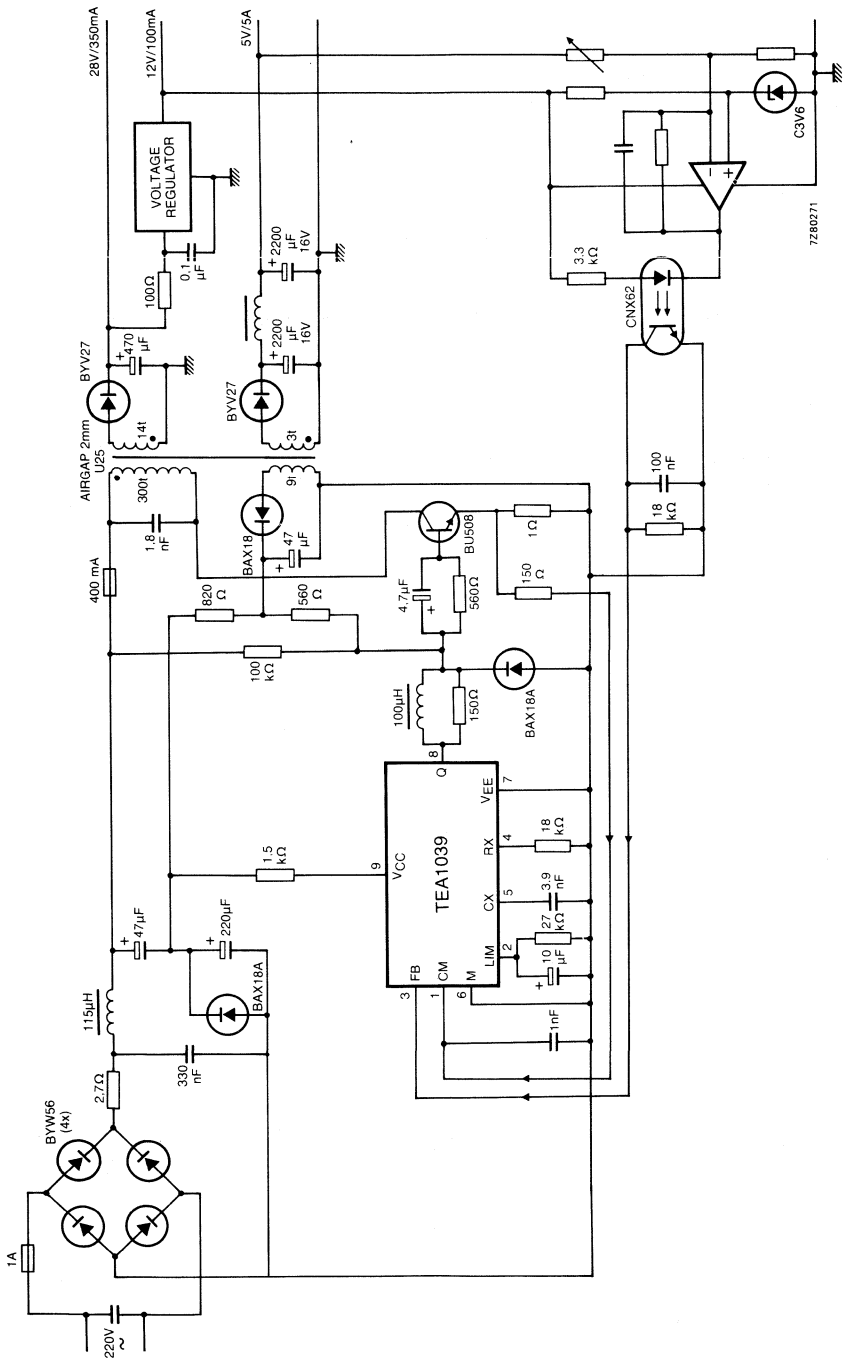


Fig. 9 Typical application of the TEA1039 in a variable-frequency flyback converter switched-mode power supply. An optocoupler CNX62 is used for voltage separation.

APPLICATION INFORMATION SUPPLIED ON REQUEST

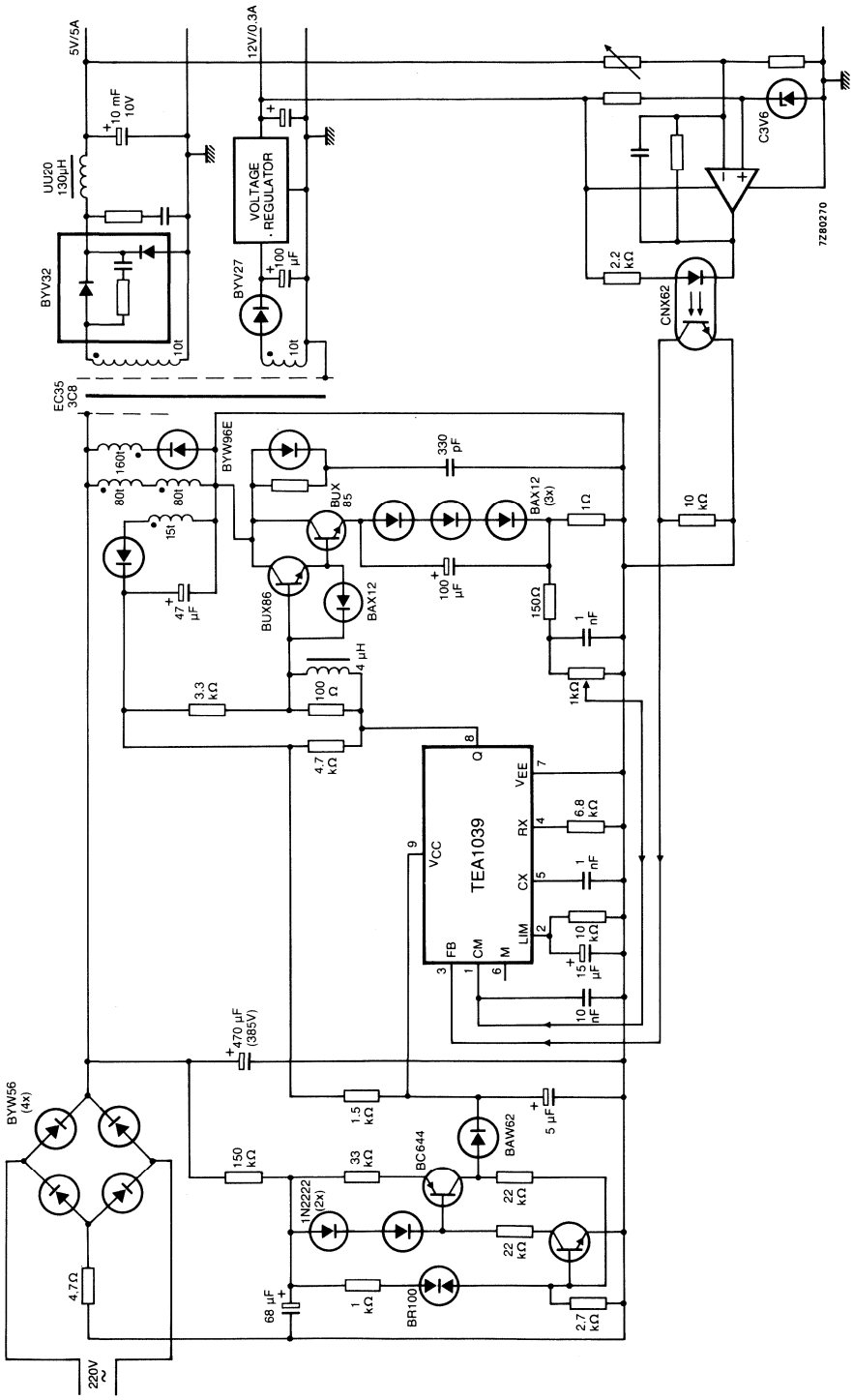


Fig. 10 Typical application of the TEA1039 in a fixed-frequency, variable duty factor forward converter switched-mode power supply. An optocoupler CNX62 is used for voltage separation.

APPLICATION INFORMATION SUPPLIED ON REQUEST

PAL/NTSC COLOUR ENCODER

GENERAL DESCRIPTION

The TEA2000 is a monolithic integrated circuit, which encodes colour information and provides composite video output for driving a VHF or UHF modulator.

Features

- European PAL and American NTSC/M standard selectable
- Internal generation of burst timing and PAL-switch-function
- 6 bit binary TTL compatible input provides 64 different colours
- TTL compatible colour blanking input
- TTL compatible sync input

QUICK REFERENCE DATA

Supply voltage	$V_{11\text{-}9}$	typ.	12 V
Supply current at $V_{11\text{-}9}$ = 12 V	I_{11}	typ.	55 mA
Input voltage pins 1,2,3,4,5,14,16,17,18	V_{IL}	max.	0,8 V
	V_{IH}	min.	2,0 V
Composite video output (sync tip to white)	$V_{6\text{-}9(p\text{-}p)}$	typ.	2,0 V
Operating temperature range	T_{amb}		0 to + 70 °C

PACKAGE OUTLINE

18-lead DIL; plastic with internal heat spreader (SOT102).

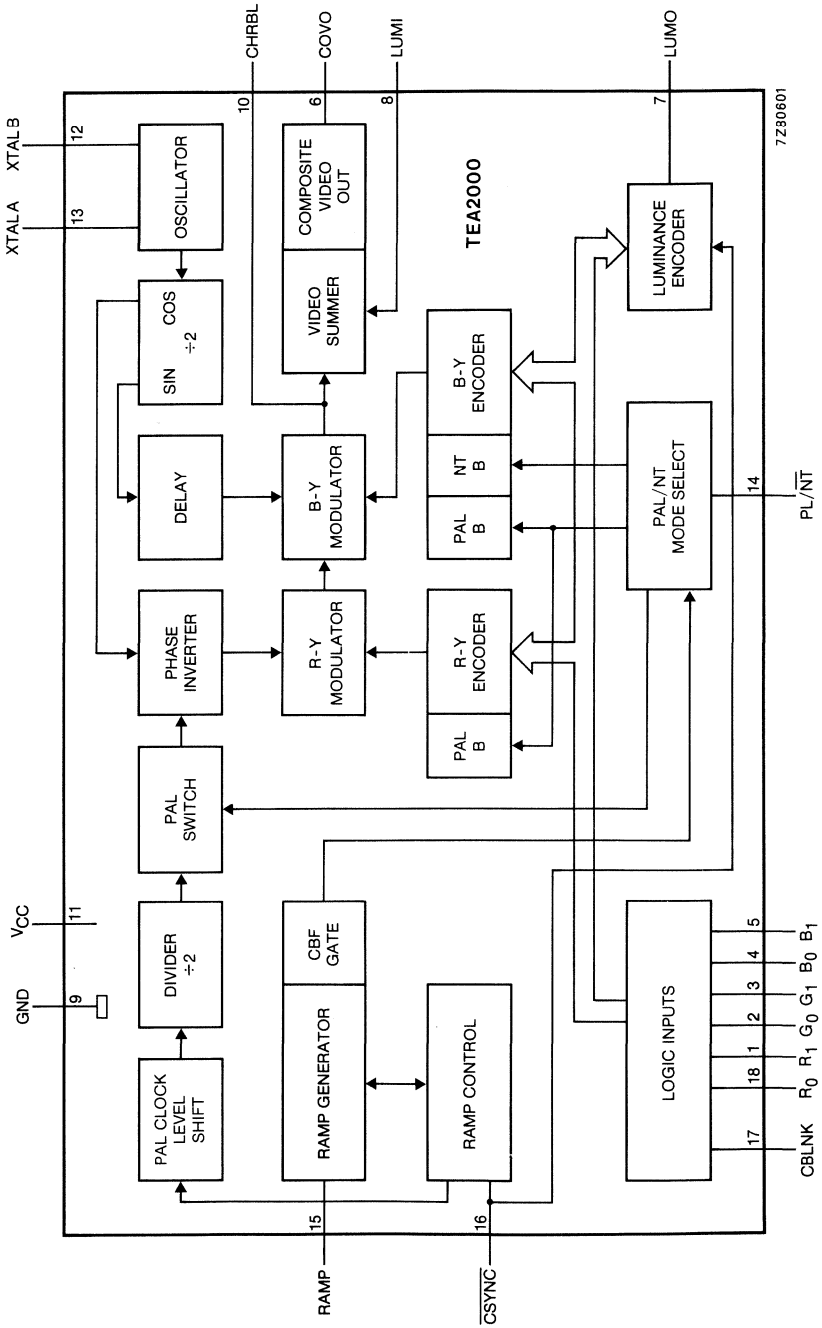


Fig. 1 Block diagram.

PINNING

1. Red 1 binary input
2. Green 0 binary input
3. Green 1 binary input
4. Blue 0 binary input
5. Blue 1 binary input
6. Composite video output
7. Luminance output to delay line
8. Luminance input from delay line
9. Ground 0 volt
10. Chrominance band limiting
11. Supply voltage
12. } Oscillator inputs { 7,16 MHz crystal for NTSC
13. } { 8,86 MHz crystal for PAL
14. PAL/NTSC switch
15. Ramp
16. Composite sync input ($\overline{\text{CSYNC}}$)
17. Composite blanking input (CBLNK)
18. Red 0 binary input

FUNCTIONAL DESCRIPTION

The TEA2000 PAL/NTSC colour encoder and video summer integrated circuit has an internal oscillator from which the (R-Y) and (B-Y) waveforms are generated. The TEA2000 accepts timing signals (composite sync, composite blanking) and a 6 bit binary coded input giving colour information. The inputs are organized as 2 bits per primary colour and gamma correction is applied to the resultant luminance and chrominance levels. Each of the equally spaced intensity levels (for each primary colour) is combined with those of the other primary colours. This produces 64 output colours comprising a wide range of saturated and desaturated colours, black, white and two levels of grey. The resultant output is a composite video signal compatible with the PAL and NTSC/M standards.

PIN DESCRIPTION

R0, R1, G0, G1, B0, B1, pins 18, 1,2,3,4 and 5.
These are the red, green and blue logic inputs. 2 bits per primary colour. These inputs are TTL compatible.

$\overline{\text{CSYNC}}$, pin 16.

Composite sync input requiring a negative logic signal, TTL compatible. For PAL operation the field sync must include line sync information.

XTALA, XTALB, pins 12 and 13.

Oscillator inputs. A crystal in series with a trimmer capacitor is connected between pins 12 and 13. The output of the oscillator is divided to provide the four subcarrier phases required in the encoder. The crystal frequencies are:

PAL mode 8,867238 MHz
NTSC mode 7,15909 MHz

LUMO, LUMI, pins 7 and 8.

Luminance output and input. The combined luminance and sync signal appearing at pin 7 must be d.c. coupled to pin 8 via an appropriate luminance delay line or resistor network. Resistors must have a tolerence of ± 5%, or better, as they affect the d.c. level at COVO, pin 6.

CHRBL, pin 10.

Chrominance filtering can be accomplished by connecting a chrominance frequency tuned filter (4,43 MHz or 3,57 MHZ), via a blocking capacitor to pin 10. This point is the chrominance summing junction and has a nominal internal impedance of 1,5 kΩ. If a filter is used at this point then the delay caused to the chrominance signal should be compensated by an appropriate luminance delay line.

COVO, pin 6.

Composite video output is internally buffered giving a nominal output voltage swing of 2 V sync-white and a nominal sync 5 V level.

PL/$\overline{\text{NT}}$, pin 14.

PAL/NTSC, select input selects PAL mode when HIGH and NTSC mode when LOW. This input is TTL compatable. An internal pull-up resistor selects PAL if the pin is not connected.

RAMP, pin 15.

Ramp timing component connection. A capacitor and resistor connected to pin 15 provide timing information for the colour burst and for PAL phase switching. Alternative components may be used to optimise for NTSC operation.

V_{CC}, pin 11.

12 volt supply.

GND, pin 9.

Ground connection, zero volts.

CBLNK, pin 17.

Blanking input when high, switches off colour inputs. CBLNK must be high during sync and colour burst unless colour inputs are all low at this time. This input is TTL compatible.

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Supply voltage V_{11-9}	max.	13,2	V
Voltages, pin 1,2,3,4,5,14,16,17,18	max.	V_{11-9}	V
Storage temperature		−20 to +125	°C
Operating ambient temperature		0 to + 70	°C

CHARACTERISTICS

V_{11-9} = 12 V; T_{amb} = 25 °C; measured in Fig. 3 unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_{11-9}	10,8	12	13,2	V
Supply current V_{11-9} = 12 V	I_{11}	–	55	–	mA
Oscillator stability, pins 12 and 13					
Crystal type 4322 143 04051					
V_P = 10,8 to 12 V		–	+50	–	Hz
V_P = 12 to 13,2 V		–	–50	–	Hz
Digital inputs					
$\overline{CSYNC}$, CBLNK, PL/$\overline{NT}$ pins 16,17,14 R0,R1,G0,G1,B0,B1 pins 18,1,2,3,4,5					
V_{IN} (LOW)	V_{IL}	–0,5	–	0,8	V
V_{IN} (HIGH)	V_{IH}	2	–	V_{11-9}	V
Input capacitance	C_i	–	–	10	pF
Input rise and fall times $\overline{CSYNC}$, CBLNK, R0,R1,G0,G1,B0,B1 pins 16,17,18,1,2,3,4,5	t_r,t_f	–	–	200	ns
Input current d.c. for V_{IN} = 0 V	I_{IL}	–	–	–100	μA
Input current d.c. for V_{IN} = 2 V	I_{IH}	–	–	20	μA
PL/$\overline{NT}$, pin 14					
Input current d.c. for V_{IN} = 0 V	I_{IL}	–	–	–500	μA
Input current d.c. for V_{IN} = 2 V	I_{IH}	–	–	–200	μA
Composite video output, pin 6					
Output amplitude (sync tip-white)	$V_{6-9\ (p-p)}$	–	2	–	V
Sync tip level	V_{6-9}	–	5	–	V
Output load resistor	R_{6-9}	0,47	1	–	kΩ
Variation of output amplitude T_{amb} = 0 to +70 °C	$V_{(p-p)}$	–	–	tbf	%
Over supply range V_{11-9} = 10,8 to 13,2 V	ΔV	–	–	tbf	%
Output impedance (with 1 kΩ load)	R_L	–	15	–	Ω
Residual chrominance on white	ΔV_{rms}	–	30	–	mV
Tolerance on luminance amplitude	ΔV	–	10	–	%
Tolerance on chrominance amplitude	ΔV	–	10	–	%
Tolerance on chrominance phase	ΔΩ	–	tbf	–	%
Chrominance band limiting, pin 10					
Internal resistance	R_{10-11}	–	1,5	–	kΩ
Luminance delay, pins 7 and 8					
Nominal series resistor (±5%)	R_S	–	1,2	–	kΩ
Nominal load resistor at luminance input (±5%)	R_L	–	1	–	kΩ
Ramp timing, pin 15 (see Fig. 4)					
With external RC circuit R = 36 kΩ; C = 330 pF (note 1)					
Start of burst from line sync	t_b	–	5,7	–	μs
Burst width	t_w	–	2,5	–	μs
Threshold for seperation of equalizing pulses and sync pulses	t	36	44	56	μs

Note: 1. A figure of 5 pF is assumed for external capacitance. This figure includes temperature dependence of the components.

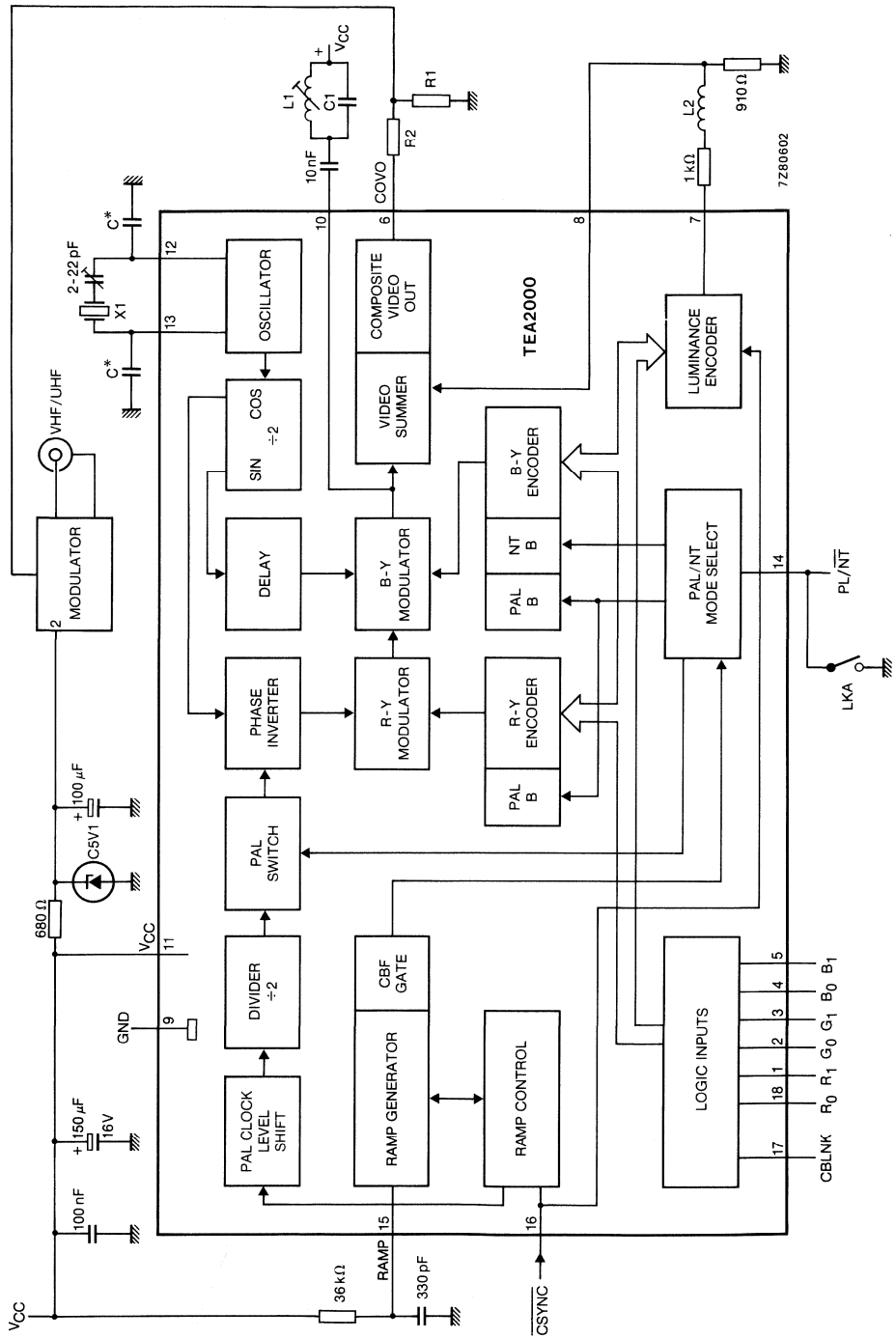


Fig. 2 Internal circuit details and typical external connections.

X1 (PAL) = 8,867238 MHz
X1 (NTSC) = 7,159100 MHz
C* = 5,6 pF only for mask version 1

COMPONENT	PAL	NTSC
L1	15 μH	18 μH
C1	82 pF	100 pF
L2	DL270	DL330
R1	430 Ω	510 Ω
R2	510 Ω	750 Ω
M1	UM1233	UM1622
LKA	o/c	made

Component list for Fig. 2.

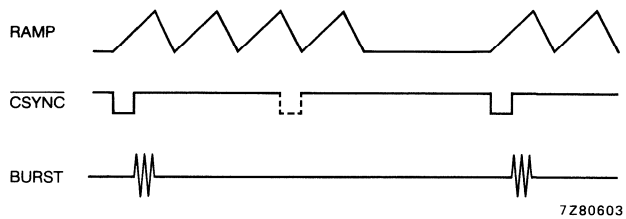


Fig. 3 Ramp timing.

1.3 GHz I²C-BUS CONTROLLED FREQUENCY SYNTHESIZER

GENERAL DESCRIPTION

The TSA5510 is a bipolar single-chip frequency synthesizer. It performs all the tuning functions of a phase-locked loop (PLL) television tuning system. The IC is designed for application in all types of television receivers.

Control data is entered via the I²C-bus; five serial bytes are required to address the device, select the oscillator frequency, program the 8 output ports and set the programmable current amplifier (charge pump) current. Three of these ports can also be used as general purpose I/O ports.

Digital information concerning these ports can be read out of the TSA5510 on the serial data line (SDA), one status byte, during a READ operation.

A flag is set when the PLL is "in-lock" and read during a READ operation. The TSA5510 has one fixed I²C-bus address and 3 programmable addresses, programmed by applying a specific voltage on Port 3.

The phase comparator operates at a frequency of 7.8125 kHz when a 4 MHz crystal is used.

Features

- Complete 1.3 GHz single-chip system
- Low power: 5 V at 35 mA
- I²C-bus programming
- In-lock flag
- Variable capacitor drive disable
- Low radiation
- Address selection for Picture-in Picture Controller (PIPCO), Direct Broadcast Satellite tuner (DBS), etc.
- 8 controllable outputs, 3 bidirectional
- Power-down flag

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 14)		V_{CC}	4.5	5.0	5.5	V
Supply current		I_{CC}	25	35	50	mA
Input frequency range		f_i	64	–	1300	MHz
Input voltage (RMS value)	f_i = 80 - 150 MHz	$V_{i(rms)}$	12/–25	–	300/2.6	mV/dBm
	f_i = 150 - 1000 MHz	$V_{i(rms)}$	9/–28	–	300/2.6	mV/dBm
	f_i = 1 - 1.3 GHz	$V_{i(rms)}$	40/–15	–	300/2.6	mV/dBm
Oscillator frequency	C_{series} = 27 pF	f_{OSC}	–	4	–	MHz
Output current						
open-collector		I_{OL}	–	–	10	mA
current limited		I_{OL}	–	1	–	mA
Operating ambient temperature range		T_{amb}	–10	–	+ 80	°C
Storage temperature range		T_{stg}	–40	0	+ 125	°C
Thermal resistance		$R_{th\ j\text{-}a}$	–	70	80	K/W

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

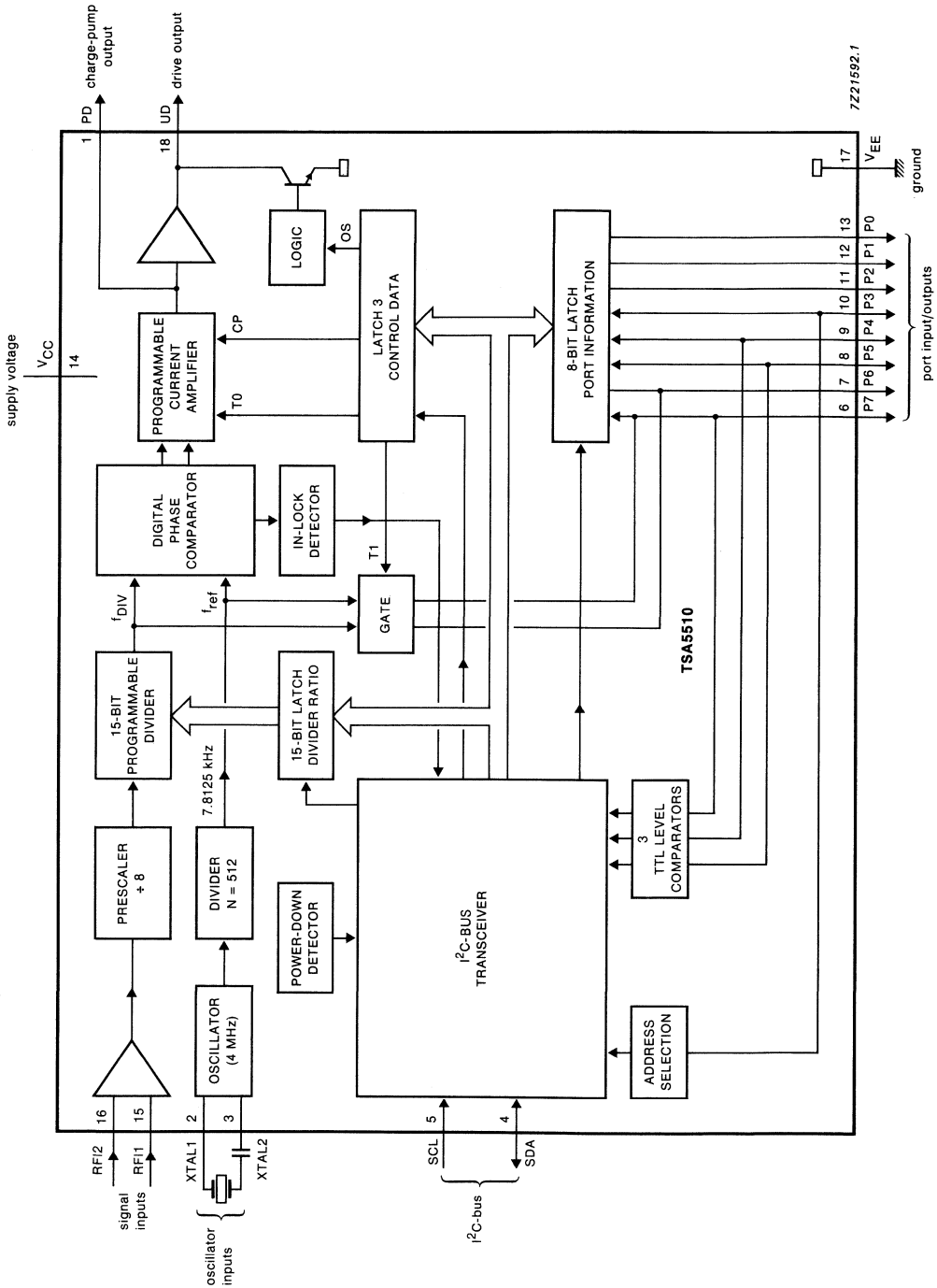


Fig. 1 Block diagram.

PINNING

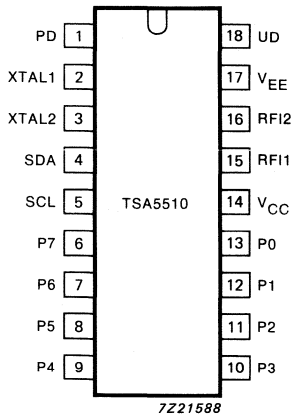


Fig. 2 Pinning diagram.

1	PD	charge-pump output	
2	XTAL1	crystal oscillator input 1	
3	XTAL2	crystal oscillator input 2	
4	SDA	serial data input/output	I²C-bus
5	SCL	serial clock input	I²C-bus
6	P7	port 7 I/O (general purpose)	
7	P6	port 6 output	
8	P5	port 5 I/O (general purpose)	
9	P4	port 4 I/O (general purpose)	
10	P3	port 3 I/O for address selection	
11	P2	port 2 output	
12	P1	port 1 output	
13	P0	port 0 output	
14	V_{CC}	positive supply voltage	
15	RFI1	UHF/VHF signal input 1	
16	RFI2	UHF/VHF signal input 2	
17	V_{EE}	ground	
18	UD	operational amplifier drive output	

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

The TSA5510 is controlled via the 2-wire I²C-bus. For programming there is one 7-bit module address and a R/$\overline{W}$ bit for selecting READ or WRITE mode.

WRITE mode: R/$\overline{W}$ = 0 (see Table 1)

After the address transmission (first byte), data bytes can be sent to the device. Four data bytes are required to fully program the TSA5510. The bus transceiver has an auto-increment facility which permits the programming of the TSA5510 within one single transmission (address + 4 data bytes).

The TSA5510 can also be partially programmed on the condition that the first data byte following the address is byte 2 or byte 4. The meaning of the bits in the data byte is explained in Table 1. The first bit of the first data byte transmitted indicates whether frequency data (first bit = 0) or charge-pump and ports information (first bit = 1) will follow. Until an I²C-bus STOP condition is sent by the controller, additional data bytes can be entered without the need to re-address the device. This allows a smooth frequency sweep for fine tuning or AFC purpose. At power-on ports are set to a high impedance state.

The 7.8125 kHz reference frequency is obtained by dividing the output of the 4 MHz oscillator by 512. As the input of the UHF/VHF signal is first divided by 8 the minimum step is 62.5 kHz.

FUNCTIONAL DESCRIPTION (continued)

READ mode: R/$\overline{W}$ = 1 (see Table 2)

Data can be read from the TSA5510 by setting the R/$\overline{W}$ bit to 1. After the slave address has been recognized, the TSA5510 generates an acknowledge pulse and the first data byte (status word) is transferred on the SDA line (MSB first). Data is valid on the SDA line during a high position of the SCL clock signal.

A second data byte can be read out of the TSA5510 if the processor generates an acknowledge on the SDA line. If no acknowledge is generated, end of transmission will occur. The TSA5510 will then release the data line to allow the processor to generate a STOP condition.

When ports P3 to P5 and P7 are used as inputs, they must be programmed in their high-impedance state.

The power-on reset (POR) flag is set to logic 1 when V_{CC} drops below 3 V and at power-on. It is reset when an end of data is detected by the TSA5510 (end of READ sequence).

A control of the loop is made possible with the in-lock flag FL which indicates (FL = 1) when the loop is phase-locked.

Bits I0, I1 and I2 represent the status of the I/O ports P4, P5 and P7 respectively. A logic 0 indicates a low level and a logic 1 indicates a high level (TTL levels).

Address selection (see Table 3)

The module address contains programmable address bits (MA0 and MA1) which offer together with the I/O port P3 the possibility of having up to 3 synthesizers in one system. The relationship between bits MA0 and MA1 and the input voltage on I/O port P3 is given in Table 3.

Table 1 Write data format

	MSB							LSB		
address	1	1	0	0	0	MA1	MA0	0*	A	byte 1
programmable divider	0	N14	N13	N12	N11	N10	N9	N8	A	byte 2
programmable divider	N7	N6	N5	N4	N3	N2	N1	N0	A	byte 3
charge-pump and test bits	1	CP	T1	T0	1	1	1	OS	A	byte 4
I/O port control bits	P7	P6	P5	P4	P3	P2	P1	P0	A	byte 5

* R/W bit = 0 for WRITE mode;
R/W bit = 1 for READ mode.

Where

A is the acknowledge bit.
N14 to N0 are the programmable divider bits;
$N = N14 \times 2^{14} + N13 \times 2^{13} + \ldots + N1 \times 2 + N0$.
CP is the charge-pump current;
CP = 0 : 50 μA
CP = 1 : 220 μA.
P3 to P0 = 1 : limited current output is active.
P7 to P4 = 1 : open-collector output is active.
P7 to P0 = 0 : outputs are in high-impedance state.
T1, T0, OS = 0, 0, 0 : normal operation.
T1 = 1, P6 = f_{ref}, P7 = f_{DIV}.
T0 = 1 : 3-state charge pump.
OS = 1 : operational amplifier output is switched off (variable capacitor drive is disabled).

Table 2 Read data format

	MSB								LSB	
address	1	1	0	0	0	MA1	MA0	1*	A	byte 1
status byte	POR	FL	I2	I1	I0	X	X	X	A	byte 2

Where

POR is the power-on reset flag;
POR = 1 : on power-on.
FL is the in-lock flag;
FL = 1 : loop is phase-locked.
I2, I1, I0 : digital information for I/O ports P4, P5 and P7 respectively.
X = don't care

Table 3 Address selection

MA1	MA0	voltage input on P3
0	0	0 to 0.1 V_{CC}
0	1	always valid
1	0	0.4 to 0.6 V_{CC}
1	1	0.9 V_{CC} to 13.5 V

* R/$\overline{W}$ bit = 0 for WRITE mode;
R/$\overline{W}$ bit = 1 for READ mode.

DEVELOPMENT DATA

ELECTROSTATIC DISCHARGE PROTECTION

Inputs and outputs have electrostatic discharge protection in accordance with specification MIL-STD-883C, class A

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 14)	V_{CC}	−0.3	+ 6.0	V
Charge-pump output voltage (pin 1)	$V_{1\text{-}17}$	−0.3	V_{CC}	V
Crystal oscillator input voltage (pin 2)	$V_{2\text{-}17}$	−0.3	V_{CC}	V
Serial data input/output voltage (pin 4)	$V_{4\text{-}17}$	−0.3	+ 6.0	V
Serial clock input voltage (pin 5)	$V_{5\text{-}17}$	−0.3	+ 6.0	V
Ports P7 and P5 to P3 input/output voltage (pins 6 and 8 to 10)	$V_{I/O}$	−0.3	+ 16.0	V
Ports P6 and P2 to P0 output voltage (pins 7 and 11 to 13)	V_O	−0.3	+ 16.0	V
UHF/VHF signal input voltage (pin 15)	$V_{15\text{-}17}$	−0.3	+ 2.5	V
UHF/VHF signal input voltage (pin 16)	$V_{16\text{-}17}$	−0.3	+ 2.5	V
Drive output voltage (pin 18)	$V_{18\text{-}17}$	−0.3	V_{CC}	V
Output current				
output ports (open collector)	I_{OL}	−1	+ 15	mA
serial data output (open collector)	I_{OL}	−1	+ 5	mA
Storage temperature range	T_{stg}	−40	+ 125	°C
Operating ambient temperature range	T_{amb}	−10	+ 80	°C
Junction temperature	T_j	–	+ 125	°C
Short-circuit time	t_{sc}	–	10	s

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j\text{-}a(max)} = 80$ K/W

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

DEVELOPMENT DATA

CHARACTERISTICS

V_{CC} = 5 V; V_{EE} = 0 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_{CC}	4.5	5.0	5.5	V
Supply current		I_{CC}	25	35	50	mA
Input frequency range		f_i	64	–	1300	MHz
Programmable divider		N_n	256	–	32767	bits
Oscillator frequency	C_{series} = 27 pF	f_{OSC}	–	4	–	MHz
Prescaler						
Input sensitivity	see Fig. 3					
Input voltage	V_{CC} = 5 V ± 10%; T_{amb} = −10 to 80 °C					
(RMS value)						
	f_i = 80 to 150 MHz	$V_{i(rms)}$	12/−25	–	300/2.6	mV/dBm
	f_i = 150 to 1000 MHz	$V_{i(rms)}$	9/−28	–	300/2.6	mV/dBm
	f_i = 1 to 1.3 GHz	$V_{i(rms)}$	40/−15	–	300/2.6	mV/dBm
Input impedance	see Fig. 4					
		R_i	–	50	–	Ω
		C_i	–	2	–	pF
Output ports						
Ports P0 to P3	current limited					
Leakage current	V_{10-13} = 13.5 V	I_{LO}	–	–	10	μA
Sink current	V_{10-13} = 12 V	I_{sink}	0.7	1.0	1.5	mA
Ports P4 to P7*	open-collector					
Leakage current	V_{6-9} = 13.5 V	I_{LO}	–	–	10	μA
Output voltage LOW	I_{6-9} = 10 mA**	V_{OL}	–	–	0.7	V

* When the port is active, the collector voltage may not exceed 6 V.

** Measured with a single open-collector port active.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Input ports						
Port P3						
Input current LOW	V_{IL} = 0 V	I_{IL}	−10	–	–	μA
Input current HIGH	V_{IH} = 13.5 V	I_{IH}	–	–	10	μA
Ports P4, P5, P7						
Input voltage LOW		V_{IL}	–	–	0.8	V
Input voltage HIGH		V_{IH}	2.7	–	–	V
Input current LOW	V_{IL} = 0 V	I_{IL}	−10	–	–	μA
Input current HIGH	V_{IH} = 13.5 V	I_{IH}	–	–	10	μA
Inputs						
SCL, SDA						
Input voltage LOW		V_{IL}	–	–	1.5	V
Input voltage HIGH		V_{IH}	3.0	–	5.5	V
Input current LOW	V_{CC} = 5 V; V_{IL} = 0 V	I_{IL}	−10	–	–	μA
Input current HIGH	V_{CC} = 0 V; V_{IH} = 5 V	I_{IH}	–	–	10	μA
	V_{CC} = 5 V; V_{IH} = 5 V	I_{IH}	–	–	10	μA
Outputs						
SDA	open-collector					
Leakage current	V_4 = 5.5 V	I_{LO}	–	–	10	μA
Output voltage LOW	I_4 = 3 mA	V_{OL}	–	–	0.4	V
PD						
Output current LOW	bit CP = logic 0	$\|I_{OL}\|$	22	50	75	μA
Output current HIGH	bit CP = logic 1	$\|I_{OH}\|$	90	220	300	μA
Output voltage LOW	in-lock	V_{OL}	1.5	–	2.5	V
UD (test mode)	bit T0 = logic 1					
Output current	V_{18} = 0.8 V; I_1 = 90 μA	I_{18}	500	–	–	μA
Output voltage	V_1 = 0 V	V_{18}	–	–	100	mV
Output voltage when switched off	bits T0, OS = logic 1; V_1 = 2 V	V_{18}	–	–	200	mV

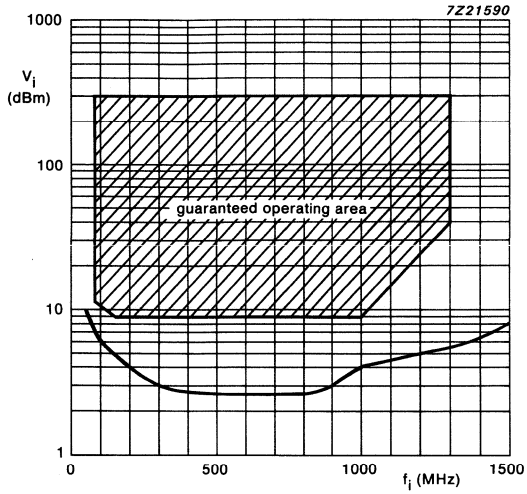


Fig. 3 Prescaler typical input sensitivity curve: V_{CC} = 4.5 to 5.5 V; T_{amb} = −10 to + 80 °C.

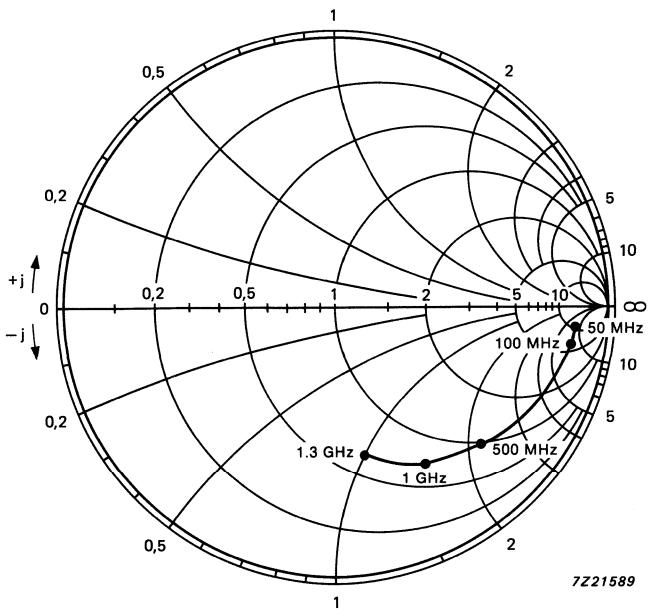


Fig. 4 Prescaler Smith chart of typical input impedance: V_{CC} = 5 V; reference value = 50 Ω.

DEVELOPMENT DATA

APPLICATION INFORMATION

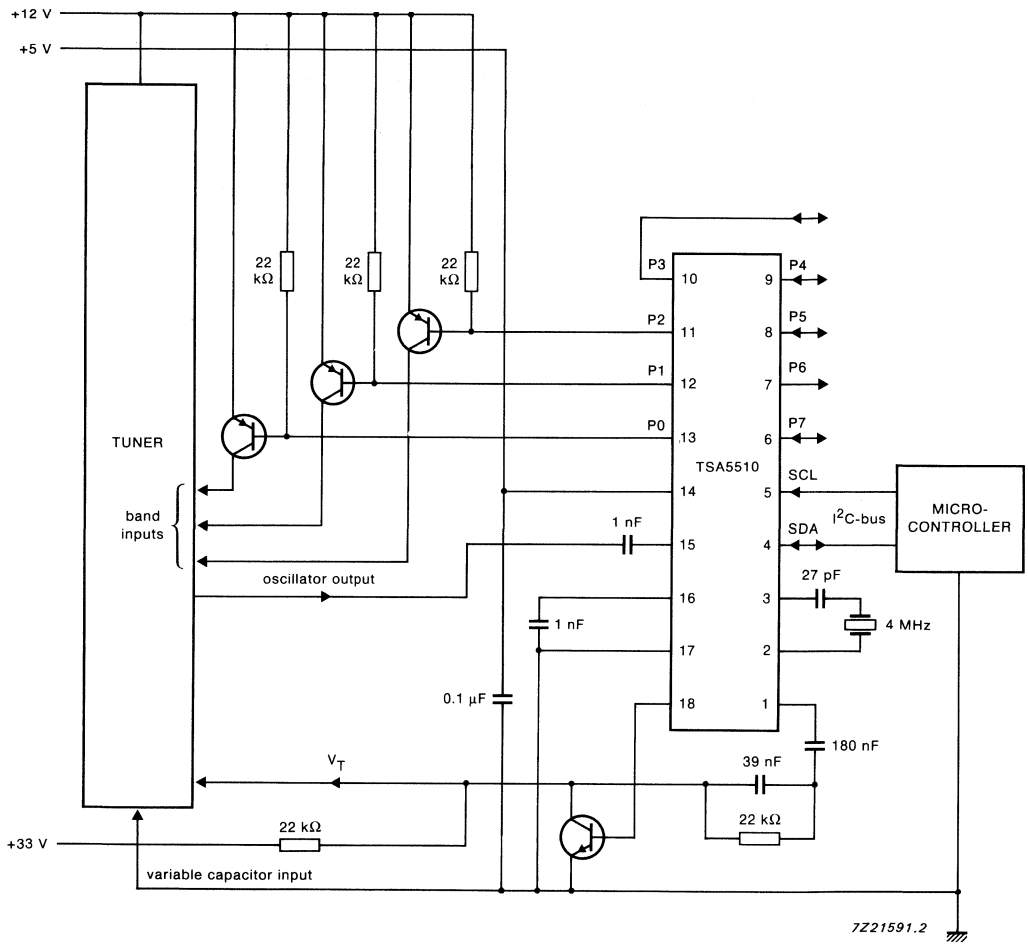


Fig. 5 Typical application diagram.

1.3 GHz I²C-BUS CONTROLLED FREQUENCY SYNTHESIZER

GENERAL DESCRIPTION

The TSA5510T is a bipolar single-chip frequency synthesizer. It performs all the tuning functions of a phase-locked loop (PLL) television tuning system. The IC is designed for application in all types of television receivers.

Control data is entered via the I²C-bus; five serial bytes are required to address the device, select the oscillator frequency, program the output ports and set the programmable current amplifier (charge pump) current. Three of these ports can also be used as general purpose I/O ports.

Digital information concerning these ports can be read from the TSA5510T on the serial data line (SDA), one status byte, during a READ operation.

A flag is set when the PLL is "in-lock" and read during a READ operation.

The TSA5510T has one fixed I²C-bus address and 3 programmable addresses, which can be programmed by applying a specific voltage to Port 3.

The phase comparator operates at a frequency of 7.8125 kHz when a 4 MHz crystal is used.

Features

- Complete 1.3 GHz single-chip system
- Low power: 5 V at 35 mA
- I²C-bus programming
- In-lock flag
- Variable capacitor drive disable
- Low radiation
- Address selection for Picture-in Picture Controller (PIPCO), Direct Broadcast Satellite tuner (DBS), etc.
- 5 controllable outputs, 3 bidirectional
- Power-down flag

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 14)		V_{CC}	4.5	5.0	5.5	V
Supply current		I_{CC}	25	35	50	mA
Input frequency range		f_i	64	–	1300	MHz
Input voltage (RMS value)	f_i = 80 - 150 MHz	$V_{i(rms)}$	12/–25	–	300/2.6	mV/dBm
	f_i = 150 - 1000 MHz	$V_{i(rms)}$	9/–28	–	300/2.6	mV/dBm
	f_i = 1 - 1.3 GHz	$V_{i(rms)}$	40/–15	–	300/2.6	mV/dBm
Oscillator frequency	C_{series} = 27 pF	f_{OSC}	–	4	–	MHz
Output current						
open-collector		I_{OL}	–	–	10	mA
current limited		I_{OL}	–	1	–	mA
Operating ambient temperature range		T_{amb}	–10	–	+ 80	°C
Storage temperature range		T_{stg}	–40	0	+ 125	°C
Thermal resistance		$R_{th\ j\text{-}a}$	–	–	110	K/W

PACKAGE OUTLINE

16-lead mini-pack; plastic (SO16; SOT109A).

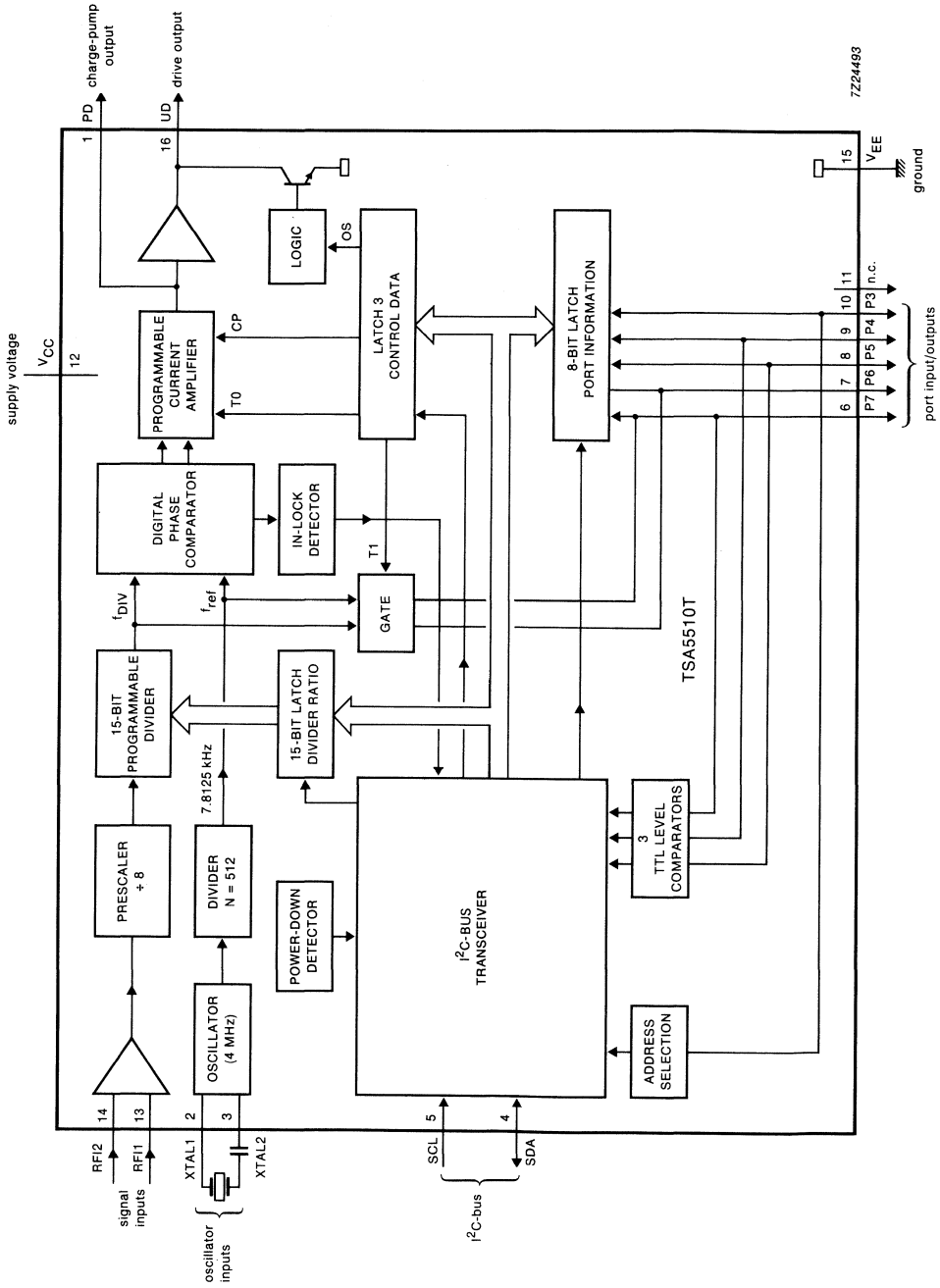


Fig.1 Block diagram.

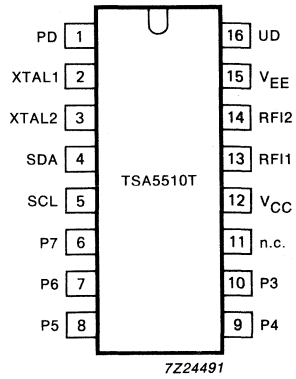


Fig.2 Pinning diagram.

PINNING

1	PD	charge-pump output	
2	XTAL1	crystal oscillator input 1	
3	XTAL2	crystal oscillator input 2	
4	SDA	serial data input/output	I²C-bus
5	SCL	serial clock input	I²C-bus
6	P7	port 7 I/O (general purpose)	
7	P6	port 6 output	
8	P5	port 5 I/O (general purpose)	
9	P4	port 4 I/O (general purpose)	
10	P3	port 3 I/O for address selection	
11	n.c.	not connected	
12	V_{CC}	positive supply voltage	
13	RFI1	UHF/VHF signal input 1	
14	RFI2	UHF/VHF signal input 2	
15	V_{EE}	ground	
16	UD	operational amplifier drive output	

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

The TSA5510T is controlled via the 2-wire I²C-bus. For programming there is one 7-bit module address and a R/$\overline{W}$ bit for selecting READ or WRITE mode.

WRITE mode: R/$\overline{W}$ = 0 (see Table 1)

After the address transmission (first byte), data bytes can be sent to the device. Four data bytes are required to fully program the TSA5510T. The bus transceiver has an auto-increment facility which permits the programming of the TSA5510T within one single transmission (address + 4 data bytes).

The TSA5510T can also be partially programmed on the condition that the first data byte following the address is byte 2 or byte 4. The meaning of the bits in the data byte is explained in Table 1. The first bit of the first data byte transmitted indicates whether frequency data (first bit = 0) or charge-pump and ports information (first bit = 1) will follow. Until an I²C-bus STOP condition is sent by the controller, additional data bytes can be entered without the need to re-address the device. This allows a smooth frequency sweep for fine tuning or AFC purpose. At power-on, ports are set to a high impedance state.

The 7.8125 kHz reference frequency is obtained by dividing the output of the 4 MHz oscillator by 512. As the input of the UHF/VHF signal is first divided by 8 the minimum step is 62.5 kHz.

FUNCTIONAL DESCRIPTION (continued)

READ mode: R/$\overline{W}$ = 1 (see Table 2)

Data can be read from the TSA5510T by setting the R/$\overline{W}$ bit to 1. After the slave address has been recognized, the TSA5510T generates an acknowledge pulse and the first data byte (status word) is transferred on the SDA line (MSB first). Data is valid on the SDA line when the SCL clock signal is HIGH.

A second data byte can be read from the TSA5510T if the processor generates an acknowledge on the SDA line. If no acknowledge is generated, end of transmission will occur. The TSA5510T will then release the data line to allow the processor to generate a STOP condition.

When ports P3 to P5 and P7 are used as inputs, they must be programmed in their high-impedance state.

The power-on reset (POR) flag is set to logic 1 when V_{CC} drops below 3 V and at power-on. It is reset when an end of data is detected by the TSA5510T (end of READ sequence).

Control of the loop is made possible with the in-lock flag FL which indicates (FL = 1) when the loop is phase-locked.

Bits I0, I1 and I2 represent the status of the I/O ports P4, P5 and P7 respectively. A logic 0 indicates a low level and a logic 1 indicates a high level (TTL levels).

Address selection (see Table 3)

The module address contains programmable address bits (MA0 and MA1) which offer, together with the I/O port P3, the possibility of having up to 3 synthesizers in one system. The relationship between bits MA0 and MA1 and the input voltage on I/O port P3 is given in Table 3.

Table 1 Write data format

	MSB							LSB		
address	1	1	0	0	0	MA1	MA0	0*	A	byte 1
programmable divider	0	N14	N13	N12	N11	N10	N9	N8	A	byte 2
programmable divider	N7	N6	N5	N4	N3	N2	N1	N0	A	byte 3
charge-pump and test bits	1	CP	T1	T0	1	1	1	OS	A	byte 4
I/O port control bits	P7	P6	P5	P4	P3	–	–	–	A	byte 5

* R/$\overline{W}$ bit = 0 for WRITE mode;
R/$\overline{W}$ bit = 1 for READ mode.

Where

A is the acknowledge bit.
N14 to N0 are the programmable divider bits;
$N = N14 \times 2^{14} + N13 \times 2^{13} + \ldots + N1 \times 2 + N0$.
CP is the charge-pump current; CP = 0 : 50 μA; CP = 1 : 220 μA
P3 = 1 : limited current output is active.
P7 to P4 = 1 : open-collector output is active.
P7 to P3 = 0 : output is in high-impedance state.
T1, T0, OS = 0, 0, 0 : normal operation.
T1 = 1, P6 = f_{ref}, P7 = f_{DIV}.
T0 = 1 : 3-state charge pump.
OS = 1 : operational amplifier output is switched off (variable capacitor drive is disabled).

Table 2 Read data format

	MSB								LSB	
address	1	1	0	0	0	MA1	MA0	1*	A	byte 1
status byte	POR	FL	I2	I1	I0	X	X	X	A	byte 2

Where

POR is the power-on reset flag;
POR = 1 : on power-on.
FL is the in-lock flag;
FL = 1 : loop is phase-locked.
I2, I1, I0 : digital information for I/O ports P7, P5 and P4 respectively.
X = don't care.

Table 3 Address selection

MA1	MA0	voltage input on P3
0	0	0 to 0.1 V_{CC}
0	1	always valid
1	0	0.4 to 0.6 V_{CC}
1	1	0.9 V_{CC} to 13.5 V

* R/$\overline{W}$ bit = 0 for WRITE mode;
R/$\overline{W}$ bit = 1 for READ mode.

ELECTROSTATIC DISCHARGE PROTECTION

Inputs and outputs have electrostatic discharge protection in accordance with specification MIL-STD-883C, class A.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 12)	V_{CC}	−0.3	+ 6.0	V
Charge-pump output voltage (pin 1)	$V_{1\text{-}15}$	−0.3	V_{CC}	V
Crystal oscillator input voltage (pin 2)	$V_{2\text{-}15}$	−0.3	V_{CC}	V
Serial data input/output voltage (pin 4)	$V_{4\text{-}15}$	−0.3	+ 6.0	V
Serial clock input voltage (pin 5)	$V_{5\text{-}15}$	−0.3	+ 6.0	V
Ports P7 and P5 to P3 input/output voltage (pins 6 and 8 to 10)	$V_{I/O}$	−0.3	+ 16.0	V
Ports P6 output voltage (pin 7)	V_O	−0.3	+ 16.0	V
UHF/VHF signal input voltage (pin 13)	$V_{13\text{-}15}$	−0.3	+ 2.5	V
UHF/VHF signal input voltage (pin 14)	$V_{14\text{-}15}$	−0.3	+ 2.5	V
Drive output voltage (pin 16)	$V_{16\text{-}15}$	−0.3	V_{CC}	V
Output current				
output ports (open collector)	I_{OL}	−1	+ 15	mA
serial data output (open collector)	I_{OL}	−1	+ 5	mA
Storage temperature range	T_{stg}	−40	+ 125	°C
Operating ambient temperature range	T_{amb}	−10	+ 80	°C
Junction temperature	T_j	−	+ 125	°C
Short-circuit time	t_{sc}	−	10	s

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j\text{-}a(max)}$ = 110 K/W

DEVELOPMENT DATA

CHARACTERISTICS

V_{CC} = 5 V; V_{EE} = 0 V; T_{amb} = 25 °C; unless otherwise specified

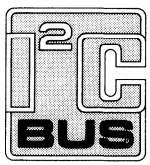
parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_{CC}	4.5	5.0	5.5	V
Supply current		I_{CC}	25	35	50	mA
Input frequency range		f_i	64	–	1300	MHz
Programmable divider		N_n	256	–	32767	bits
Oscillator frequency	C_{series} = 27 pF	f_{OSC}	–	4	–	MHz
Prescaler						
Input sensitivity	see Fig.3					
Input voltage	V_{CC} = 5 V ± 10%; T_{amb} = −10 to 80 °C					
(RMS value)						
	f_i = 80 to 150 MHz	$V_{i(rms)}$	12/−25	–	300/2.6	mV/dBm
	f_i = 150 to 1000 MHz	$V_{i(rms)}$	9/−28	–	300/2.6	mV/dBm
	f_i = 1 to 1.3 GHz	$V_{i(rms)}$	40/−15	–	300/2.6	mV/dBm
Input impedance	see Fig.4					
		R_i	–	50	–	Ω
		C_i	–	2	–	pF
Output ports						
Port P3	current limited					
Leakage current		I_{LO}	–	–	10	μA
Sink current		I_{sink}	0.7	1.0	1.5	mA
Ports P4 to P7*	open-collector					
Leakage current	V_{6-9} = 13.5 V	I_{LO}	–	–	10	μA
Output voltage LOW	I_{6-9} = 10 mA**	V_{OL}	–	–	0.7	V
Input ports						
Port P3						
Input current LOW	V_{IL} = 0 V	I_{IL}	−10	–	–	μA
Input current HIGH	V_{IH} = 13.5 V	I_{IH}	–	–	10	μA
Ports P4, P5, P7						
Input voltage LOW		V_{IL}	–	–	0.8	V
Input voltage HIGH		V_{IH}	2.7	–	–	V
Input current LOW	V_{IL} = 0 V	I_{IL}	−10	–	–	μA
Input current HIGH	V_{IH} = 13.5 V	I_{IH}	–	–	10	μA

* When the port is active, the collector voltage may not exceed 6 V.

** Measured with a single open-collector port active.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs						
SCL, SDA						
Input voltage LOW		V_{IL}	–	–	1.5	V
Input voltage HIGH		V_{IH}	3.0	–	5.5	V
Input current LOW	V_{CC} = 5 V; V_{IL} = 0 V	I_{IL}	−10	–	–	μA
Input current HIGH						
	V_{CC} = 0 V; V_{IH} = 5 V	I_{IH}	–	–	10	μA
	V_{CC} = 5 V; V_{IH} = 5 V	I_{IH}	–	–	10	μA
Outputs						
SDA	open-collector					
Leakage current	V_4 = 5.5 V	I_{LO}	–	–	10	μA
Output voltage LOW	I_4 = 3 mA	V_{OL}	–	–	0.4	V
PD						
Output current LOW	bit CP = logic 0	$\|I_{OL}\|$	22	50	75	μA
Output current HIGH	bit CP = logic 1	$\|I_{OH}\|$	90	220	300	μA
Output voltage LOW	in-lock	V_{OL}	1.5	–	2.5	V
UD (test mode)	bit T0 = logic 1					
Output current	V_{16} = 0.8 V; I_1 = 90 μA	I_{16}	500	–	–	μA
Output voltage	V_1 = 0 V	V_{16}	–	–	100	mV
Output voltage when switched off	bits T0, OS = logic 1; V_1 = 2 V	V_{16}	–	–	200	mV



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

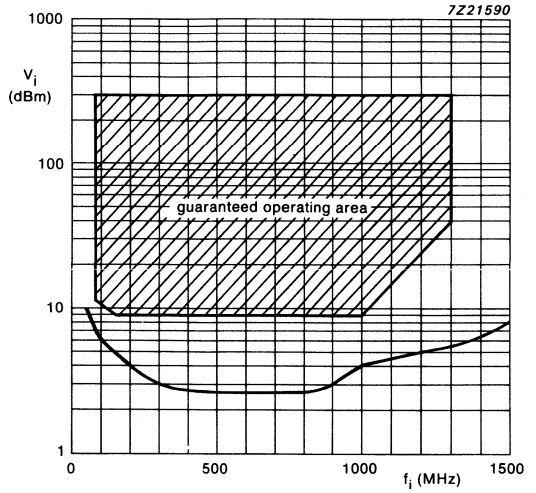


Fig. 3 Prescaler typical input sensitivity curve: V_{CC} = 4.5 to 5.5 V; T_{amb} = −10 to + 80 °C.

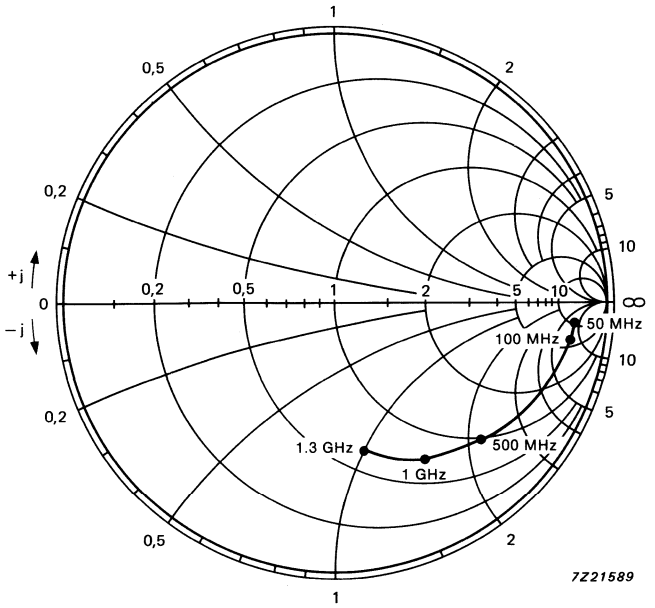


Fig. 4 Prescaler Smith chart of typical input impedance: V_{CC} = 5 V; reference value = 50 Ω.

DEVELOPMENT DATA

APPLICATION INFORMATION

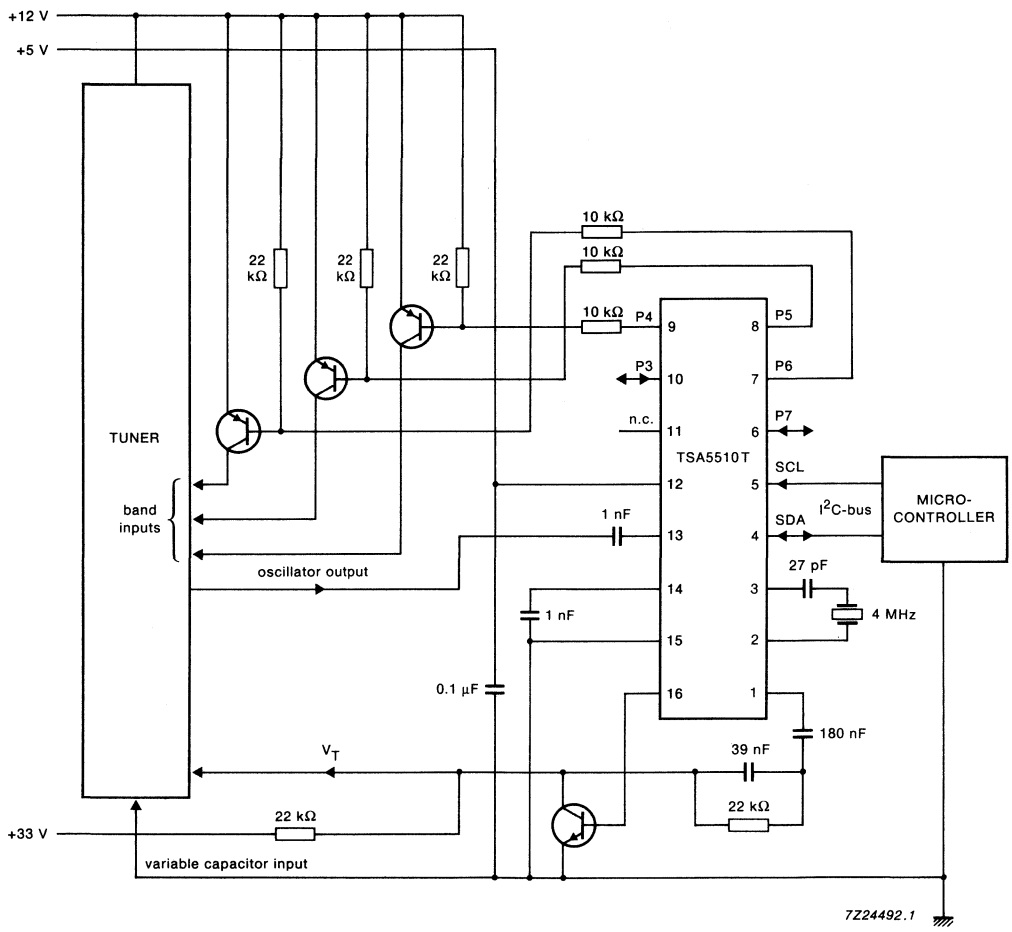


Fig.5 Typical application diagram.

μA733/733C
Differential Video Amplifier

Product Specification

DESCRIPTION

The 733 is a monolithic differential input, differential output, wide-band video amplifier. It offers fixed gains of 10, 100, or 400 without external components, and adjustable gains from 10 to 400 by the use of an external resistor. No external frequency compensation components are required for any gain option. Gain stability, wide bandwidth, and low phase distortion are obtained through use of the classic series-shunt feedback from the emitter-follower outputs to the inputs of the second stage. The emitter-follower outputs provide low output impedance, and enable the device to drive capacitive loads. The 733 is intended for use as a high-performance video and pulse amplifier in communications, magnetic memories, display and video recorder systems.

FEATURES

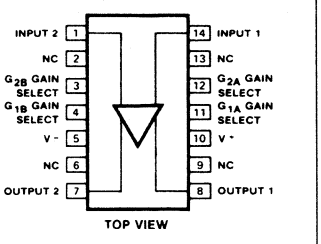
- **120MHz bandwidth**
- **250kΩ input resistance**
- **Selectable gains of 10, 100, and 400**
- **No frequency compensation required**
- **MIL-STD-883A, B, C available**

APPLICATIONS

- **Video amplifier**
- **Pulse amplifier in communications**
- **Magnetic memories**
- **Video recorder systems**

PIN CONFIGURATION

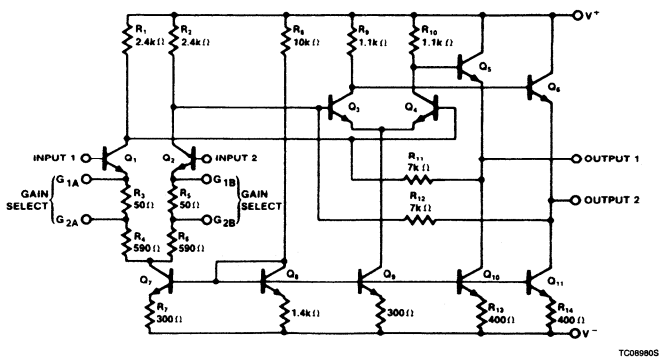
F, N Packages



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE	ORDER CODE
14-Pin Ceramic DIP	−55°C to +125°C	μA733F
14-Pin Plastic DIP	−55°C to +125°C	μA733N
14-Pin Plastic DIP	0 to +70°C	μA733CN
14-Pin Ceramic DIP	0 to +70°C	μA733CF

CIRCUIT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DIFF}	Differential input voltage	±5	V
V_{CM}	Common-mode input voltage	±6	V
V_{CC}	Supply voltage	±8	V
I_{OUT}	Output current	10	mA
T_J	Junction temperature	+150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range μA733C μA733	 0 to +70 −55 to +125	 °C °C
$P_{D\ MAX}$	Maximum power dissipation, 25°C ambient temperature (still-air)[1] F package N package	 1190 1420	 mW mW

NOTE:
1. The following derating factors should be applied above 25°C:
   F package at 9.5mW/°C
   N package at 11.4mW/°C.

DC ELECTRICAL CHARACTERISTICS

T_A = +25°C, V_S = ±6V, V_{CM} = 0, unless otherwise specified. Recommended operating supply voltages V_S = ±6.0V.

SYMBOL	PARAMETER	TEST CONDITIONS	μA733C			μA733			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Differential voltage gain Gain 1[2] Gain 2[2] Gain 3[3]	R_l = 2kΩ, V_{OUT} = $3V_{P-P}$	 250 80 8	 400 100 10	 600 120 12	 300 90 9	 400 100 10	 500 110 11	 V/V V/V V/V
BW	Bandwidth Gain 1[1] Gain 2[2] Gain 3[3]			 40 90 120			 40 90 120		 MHz MHz MHz
t_R	Rise time Gain 1[1] Gain 2[2] Gain 3[3]	V_{OUT} = $1V_{P-P}$		 10.5 4.5 2.5	 12 		 10.5 4.5 2.5	 10 	 ns ns ns
t_{PD}	Propagation delay Gain 1[1] Gain 2[2] Gain 3[3]	V_{OUT} = $1V_{P-P}$		 7.5 6.0 3.6	 10 		 7.5 6.0 3.6	 10 	 ns ns ns
R_{IN}	Input resistance Gain 1[2] Gain 2[2] Gain 3[3]		 10 	 4.0 30 250	 	 20 	 4.0 30 250	 	 kΩ kΩ kΩ
	Input capacitance[2]	Gain 2		2.0			2.0		pF
I_{OS}	Input offset current			0.4	5.0		0.4	3.0	μA
I_{BIAS}	Input bias current			9.0	30		9.0	20	μA
V_{NOISE}	Input noise voltage	BW = 1kHz to 10MHz		12			12		μV_{RMS}
V_{IN}	Input voltage range		±1.0			±1.0			V
CMRR	Common-mode rejection ratio Gain 2 Gain 2	 V_{CM} = ±1V, f ≤ 100kHz V_{CM} = ±1V, f = 5MHz	 60 	 86 60	 	 60 	 86 60	 	 dB dB
SVRR	Supply voltage rejection ratio Gain 2	ΔV_S = ±0.5V	50	70		50	70		dB

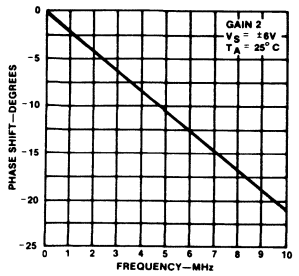
DC ELECTRICAL CHARACTERISTICS (Continued) $T_A = +25°C$, $V_S = \pm 6V$, $V_{CM} = 0$, unless otherwise specified. Recommended operating supply voltages $V_S = \pm 6.0V$.

SYMBOL	PARAMETER	TEST CONDITIONS	μA733C			μA733			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Output offset voltage Gain 1[1] Gain 2 and 3[2, 3]	$R_L = \infty$		0.6 0.35	1.5 1.5		0.6 0.35	1.5 1.0	V V
V_{CM}	Output common-mode voltage	$R_L = \infty$	2.4	2.9	3.4	2.4	2.9	3.4	V
	Output voltage swing, differential	$R_L = 2k\Omega$	3.0	4.0		3.0	4.0		V_{P-P}
I_{SINK}	Output sink current		2.5	3.6		2.5	3.6		mA
R_{OUT}	Output resistance			20			20		Ω
I_{CC}	Power supply current	$R_L = \infty$		18	24		18	24	mA
THE FOLLOWING SPECIFICATIONS APPLY OVER TEMPERATURE			**0°C ≤ T_A ≤ 70°C**			**−55°C ≤ T_A ≤ 125°C**			
	Differential voltage gain Gain 1[1] Gain 2[2] Gain[3]	$R_l = 2k\Omega$, $V_{OUT} = 3V_{P-P}$	 250 80 8		 600 120 12	 200 80 8		 600 120 12	 V/V V/V V/V
R_{IN}	Input resistance Gain 2[2]		 8			 8			 kΩ
I_{OS}	Input offset current				6			5	μA
I_{BIAS}	Input bias current				40			40	μA
V_{IN}	Input voltage range		±1.0			±1.0			V
CMRR	Common-mode rejection ratio Gain 2	$V_{CM} = \pm V$, $F \leq 100kHz$	50			50			dB
SVRR	Supply voltage rejection ratio Gain 2	$\Delta V_S = \pm 0.5V$	50			50			dB
V_{OS}	Output offset voltage Gain 1[1] Gain 2 and 3[2, 3]	$R_L = \infty$			 1.5 1.5			 1.5 1.2	 V V
V_{DIFF}	Output voltage swing, differential	$R_L = 2k\Omega$	2.8			2.5			V_{P-P}
I_{SINK}	Output sink current		2.5			2.2			mA
I_{CC}	Power supply current	$R_L \pm \infty$			27			27	mA

NOTES:
1. Gain select pins G_{1A} and G_{1B} connected together.
2. Gain select pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.

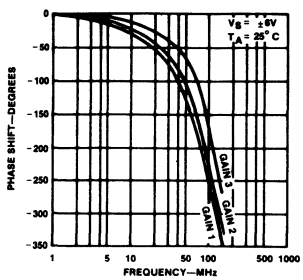
TYPICAL PERFORMANCE CHARACTERISTICS

Phase Shift as a Function of Frequency



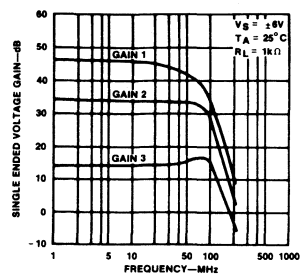
OP05620S

Phase Shift as a Function of Frequency



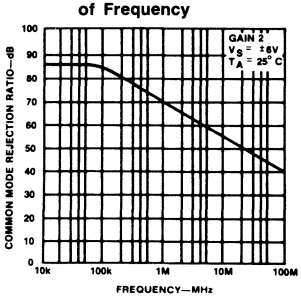
OP05630S

Voltage Gain as a Function of Frequency



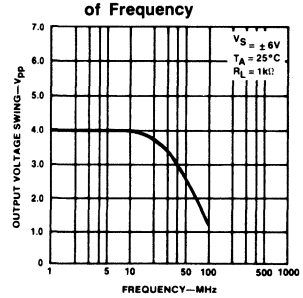
OP05640S

Common Mode Rejection Ratio as a Function of Frequency



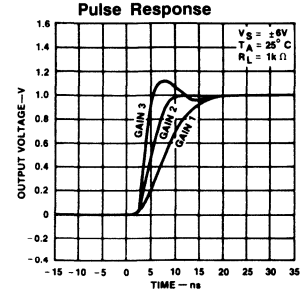
OP05650S

Output Voltage Swing as a Function of Frequency



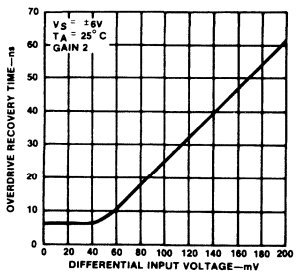
OP05660S

Pulse Response



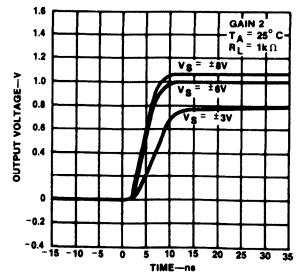
OP05670S

Differential Overdrive Recovery Time



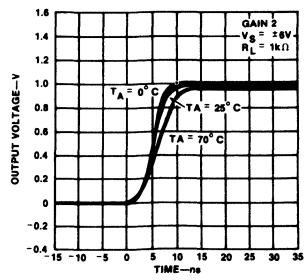
OP05680S

Pulse Response as a Function of Supply Voltage



OP05690S

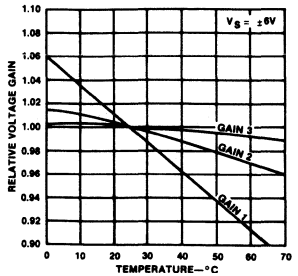
Pulse Response as a Function of Temperature



OP05700S

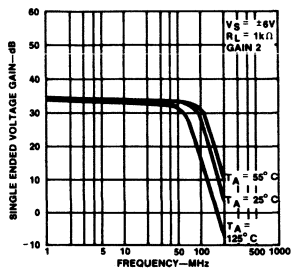
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Voltage Gain as a Function of Temperature



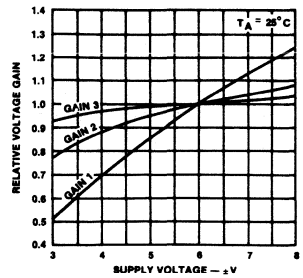
OP05710S

Gain vs Frequency as a Function of Temperature



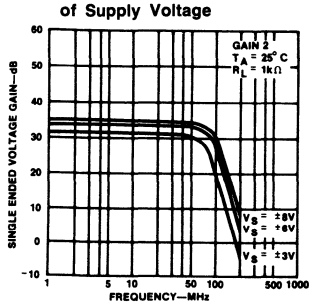
OP05720S

Voltage Gain as a Function of Supply Voltage



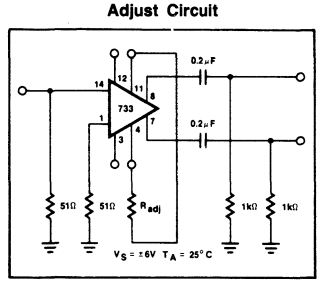
OP05730S

Gain vs Frequency as a Function of Supply Voltage



OP05740S

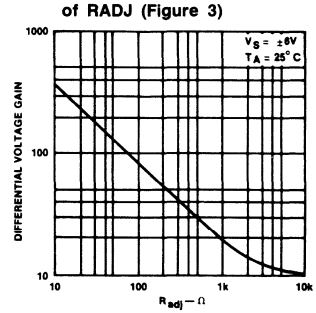
Voltage Gain Adjust Circuit



(Pin numbers apply to K Package)

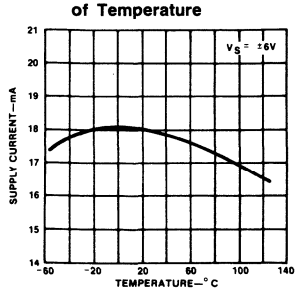
OP05750S

Voltage Gain as a Function of RADJ (Figure 3)



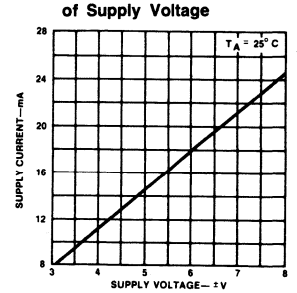
OP05760S

Supply Current as a Function of Temperature



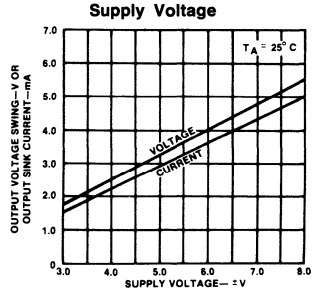
OP05770S

Supply Current as a Function of Supply Voltage



OP05780S

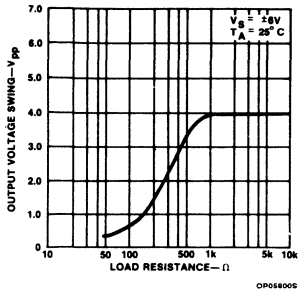
Output Voltage and Current Swing as a Function of Supply Voltage



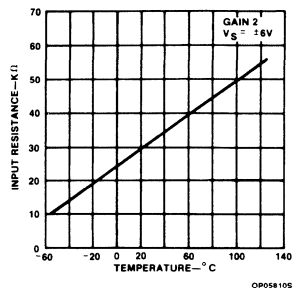
OP05790S

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

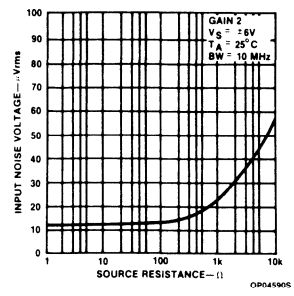
Output Voltage Swing as a Function of Load Resistance



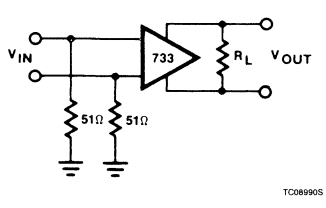
Input Resistance as a Function of Temperature

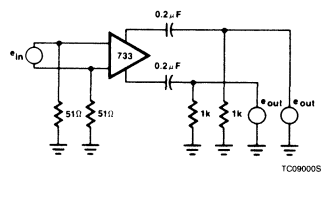


Input Noise Voltage as a Function of Source Resistance



TEST CIRCUITS $T_A = 25°C$, unless otherwise specified.

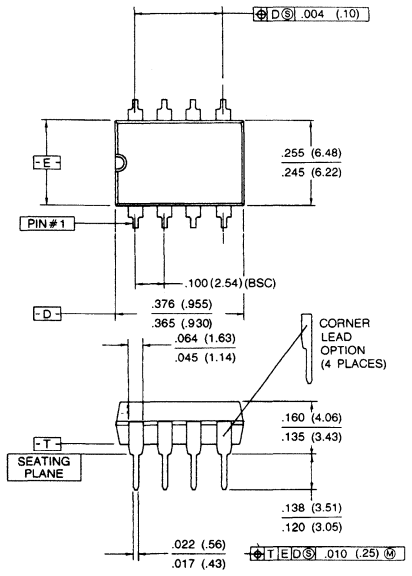


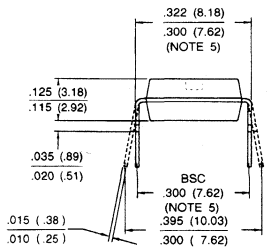


PACKAGE INFORMATION

Package outlines
Soldering

8-PIN PLASTIC PDIP (N PACKAGE)



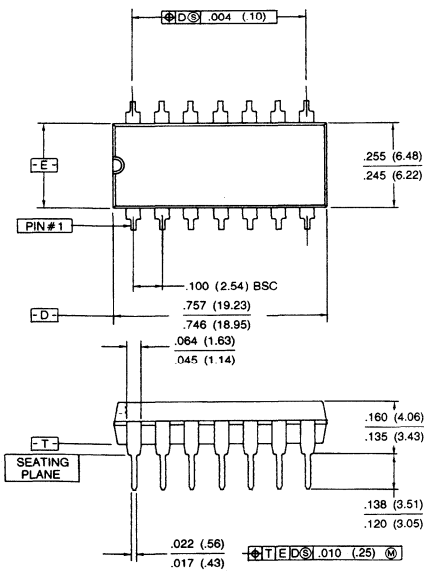


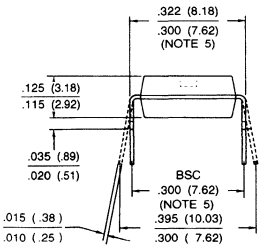
NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AB for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 8 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #8 when viewed from the top.

853-0404 81230

PO00312S

14-PIN PLASTIC DIP (N PACKAGE)



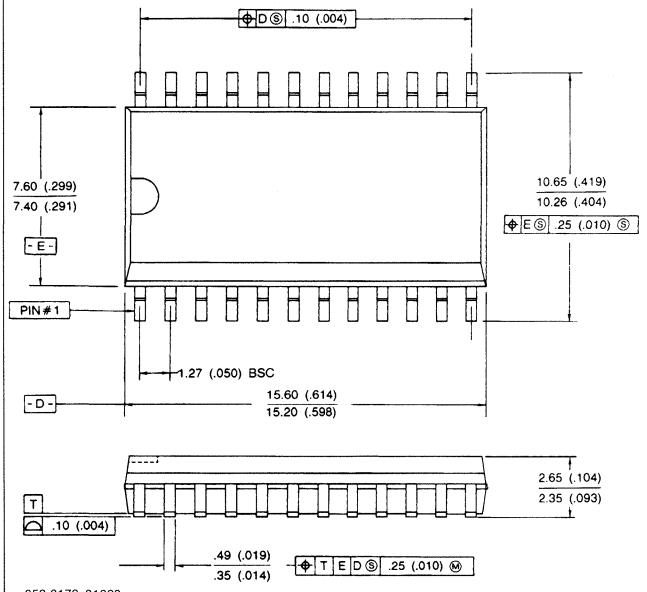


NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AC for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 14 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from the top.

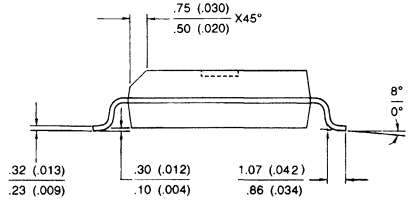
853-0405 81231

PO00330S

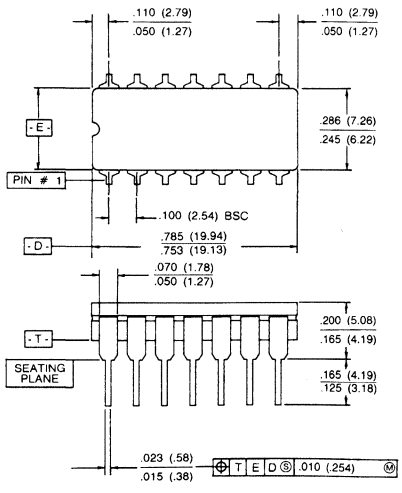
24-PIN PLASTIC SOL (D PACKAGE)



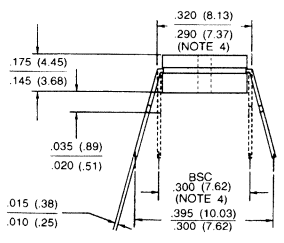
NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AD for standard small outline (SO) package, 24 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.



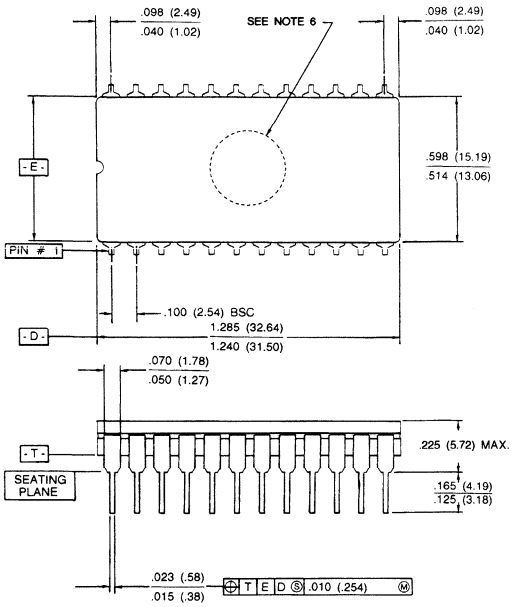
14-PIN CERDIP (F PACKAGE)

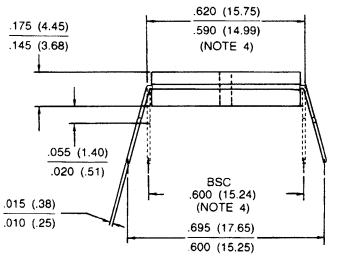


NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from the top.



24-PIN CERDIP (F PACKAGE)



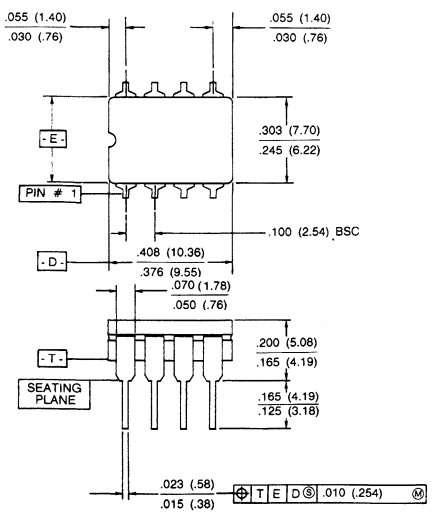


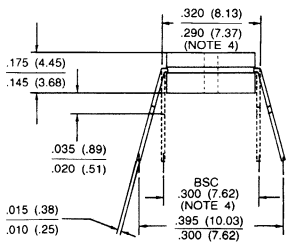
NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top.

853-0588 84221

PO00464S

8-PIN CERDIP (FE PACKAGE)



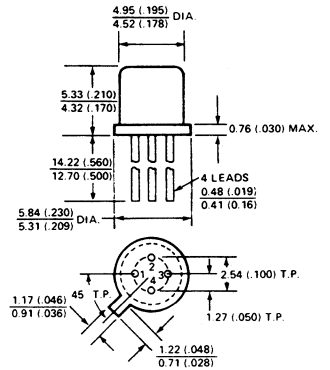


NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #8 when viewed from the top.

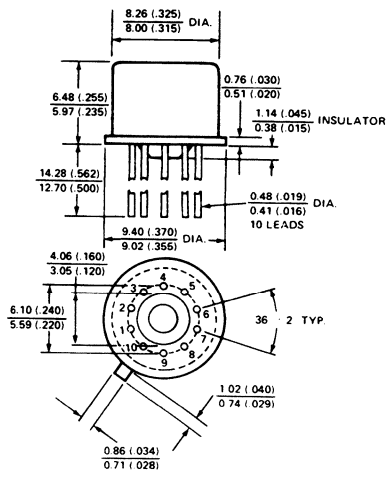
853-0580 81594

PO00480S

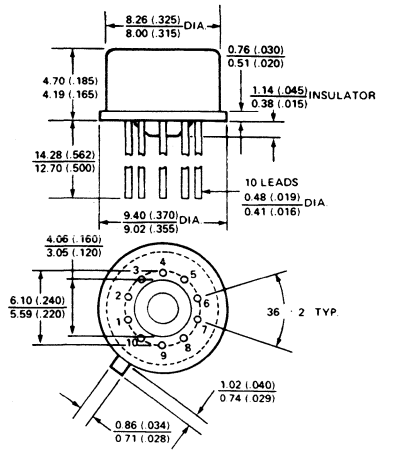
4-PIN HERMETIC TO-72 HEADER (E PACKAGE)



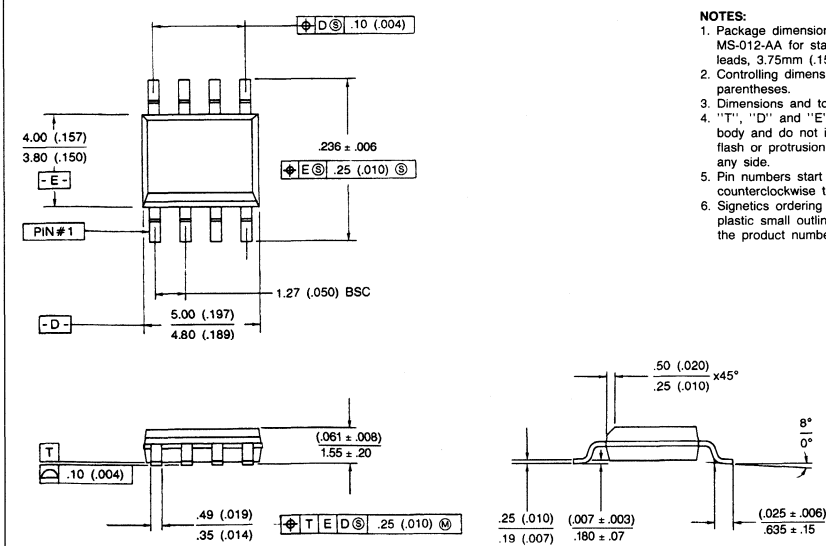
10-PIN HERMETIC TO-5/100 HEADER TALL CAN (H PACKAGE)



10-PIN HERMETIC TO-5/100 HEADER SHORT CAN (H PACKAGE)

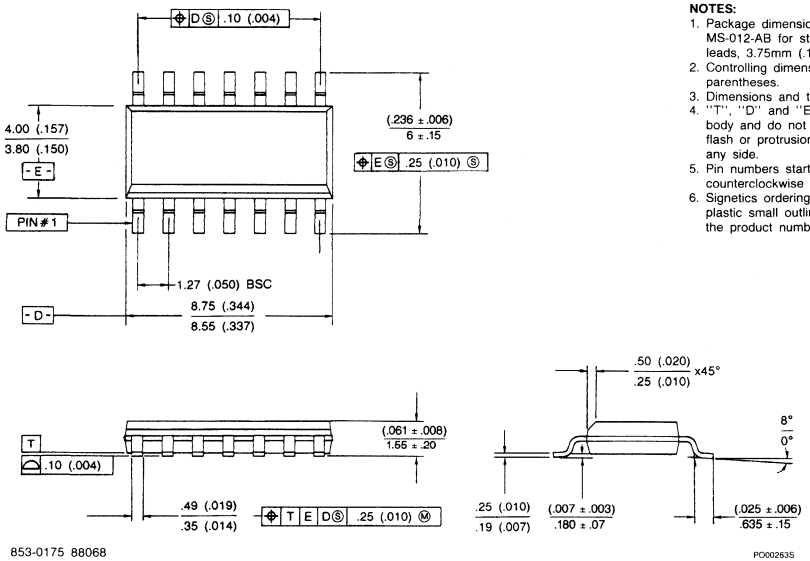


8-PIN PLASTIC SO (D PACKAGE)



NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AA for standard small outline (SO) package, 8 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #8 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

14-PIN PLASTIC SO (D PACKAGE)



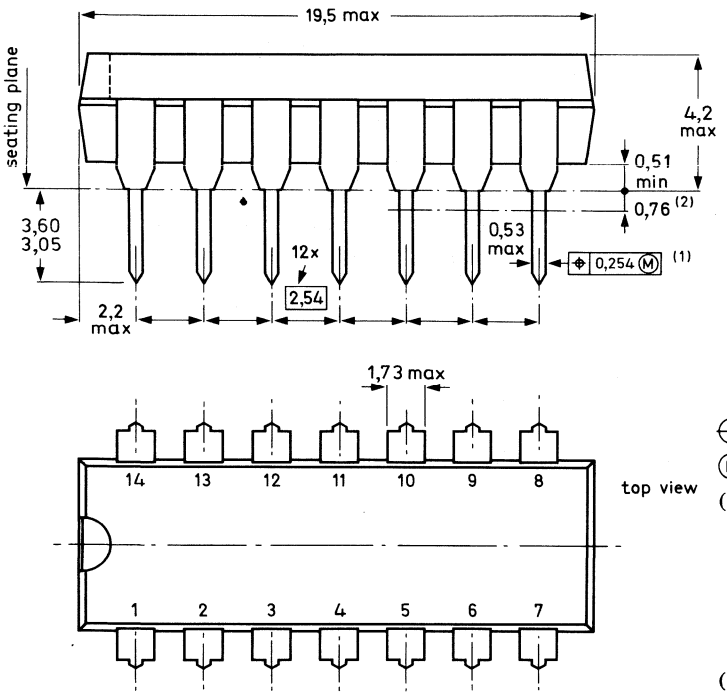
853-0175 88068

PO00263S

NOTES:

1. Package dimensions conform to JEDEC specification MS-012-AB for standard small outline (SO) package, 14 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

14-LEAD DUAL IN-LINE; PLASTIC (SOT27)



Dimensions in mm

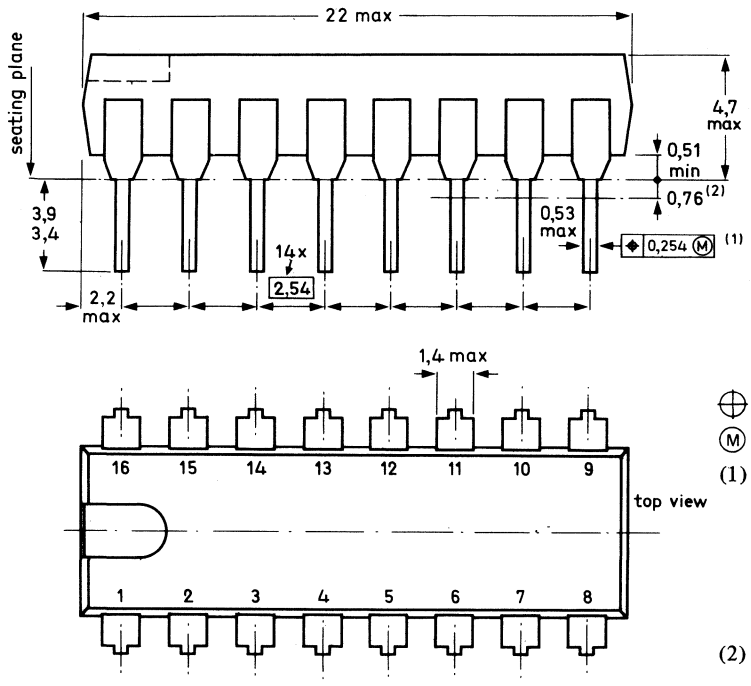
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

16-LEAD DUAL IN-LINE; PLASTIC (SOT38)



Dimensions in mm

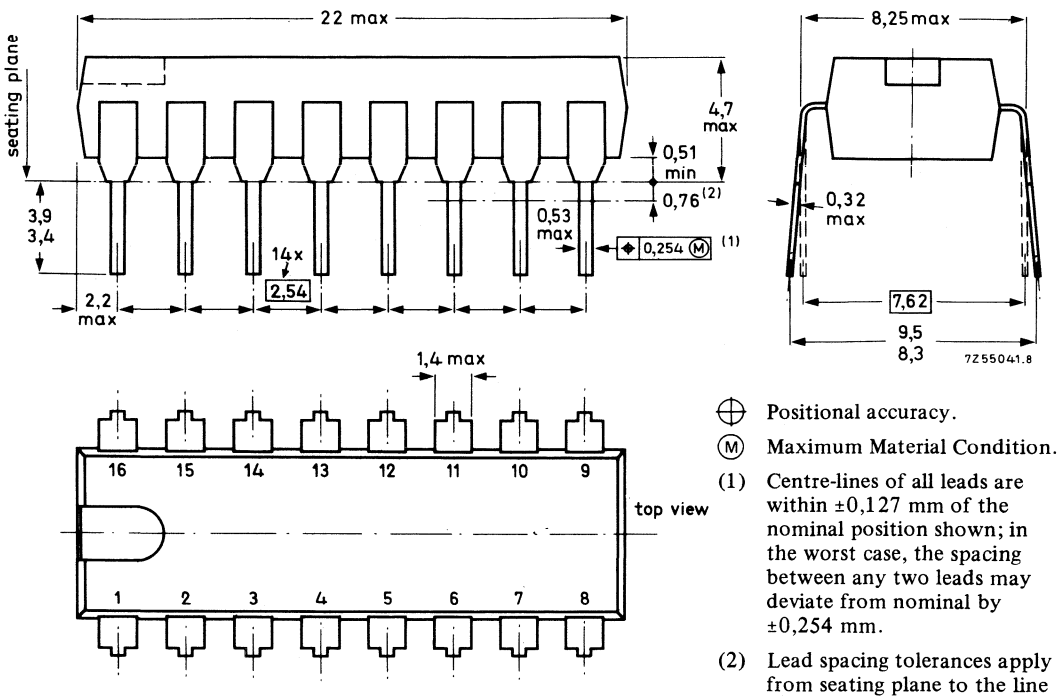
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

16-LEAD DUAL IN-LINE; PLASTIC WITH INTERNAL HEAT SPREADER (SOT38)



Dimensions in mm

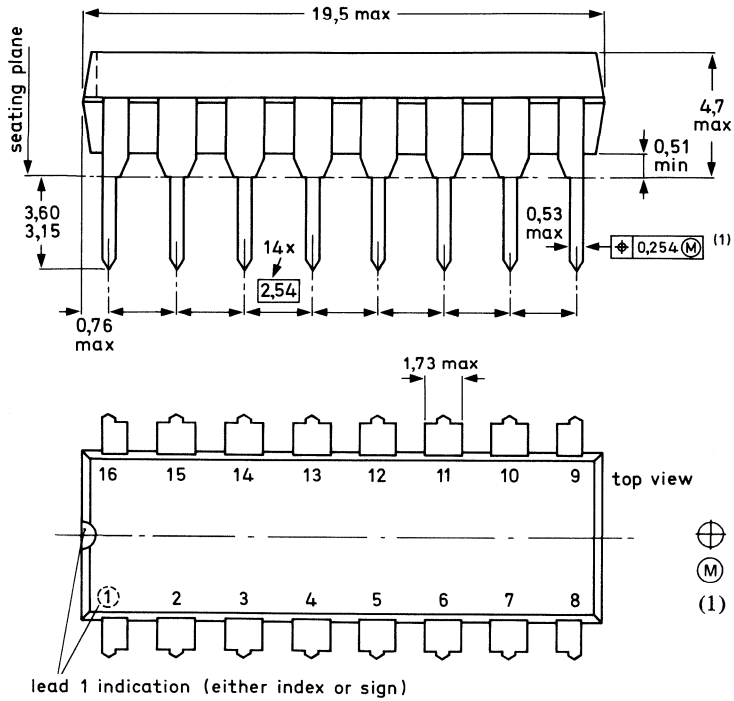
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

16-LEAD DUAL IN-LINE; PLASTIC (SOT38D)



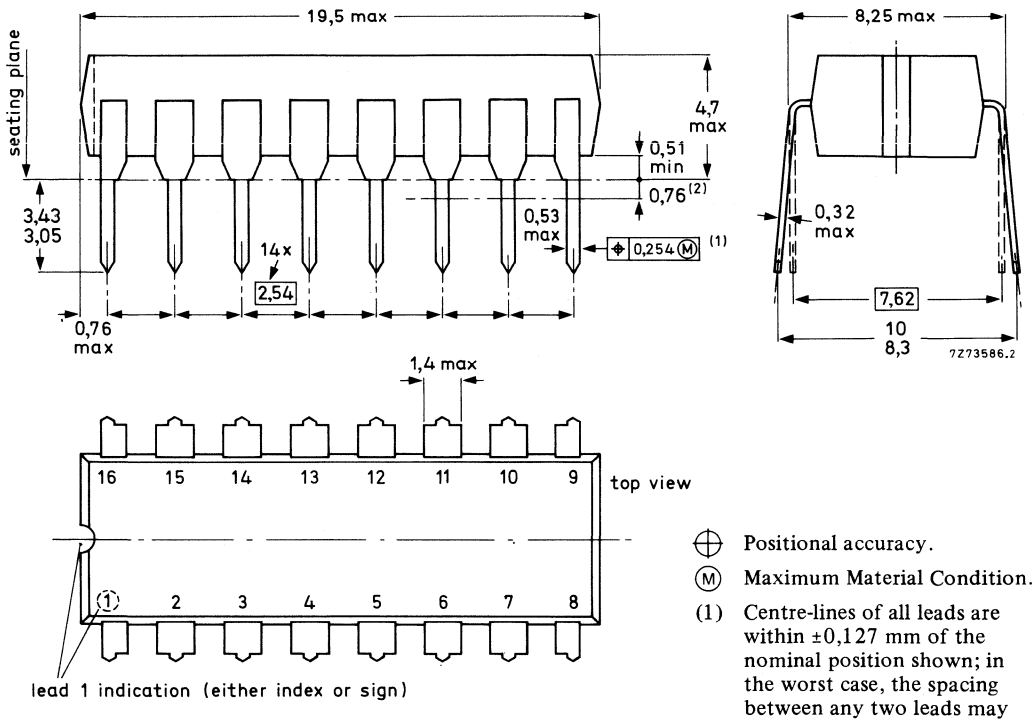
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

Dimensions in mm

16-LEAD DUAL IN-LINE; PLASTIC (SOT38Z)



⊕ Positional accuracy.

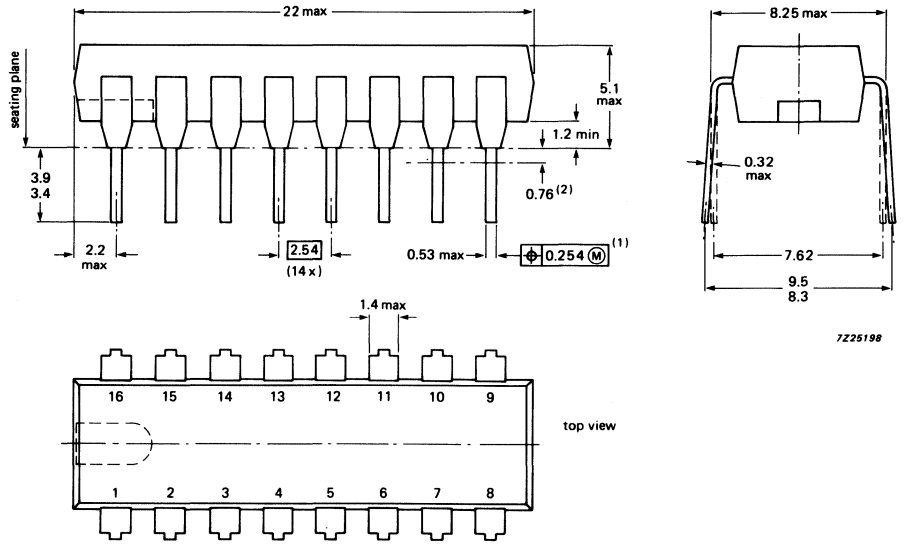
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

16-LEAD DUAL IN-LINE; PLASTIC (OPPOSITE BENT LEADS) (SOT38WBE)

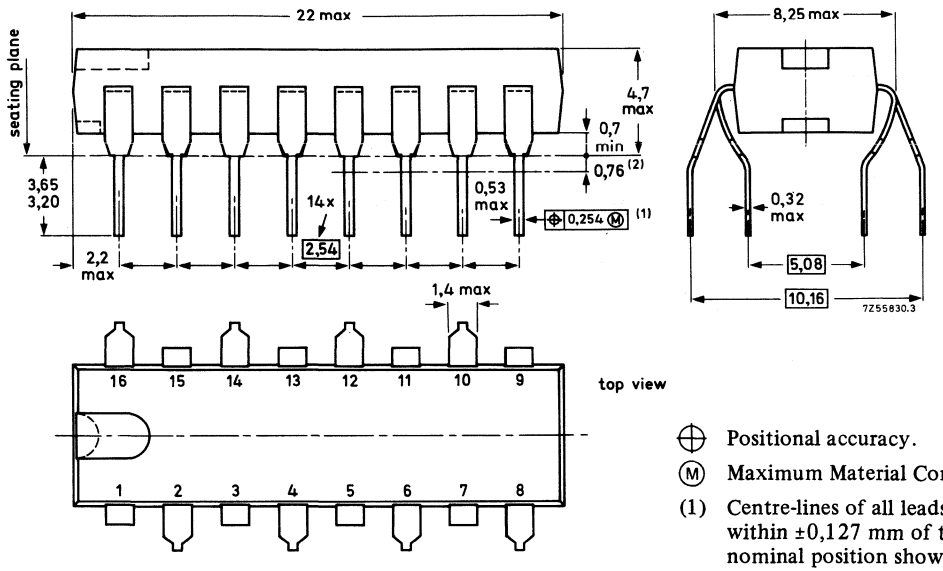


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

16-LEAD QUADRUPLE IN-LINE; PLASTIC (SOT58)



⊕ Positional accuracy.

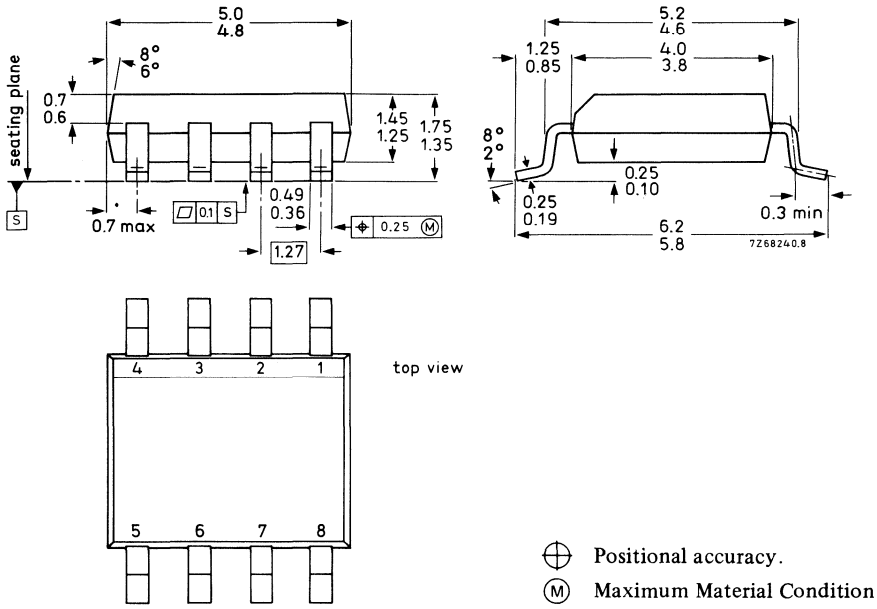
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

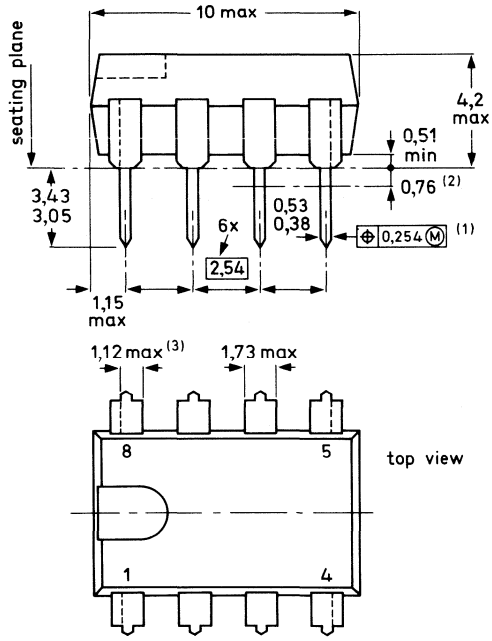
Dimensions in mm

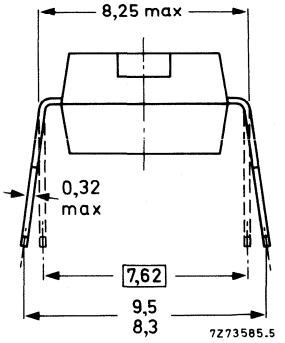
8-LEAD MINI-PACK; PLASTIC (SO8; SOT96A)



Dimensions in mm

8-LEAD DUAL IN-LINE; PLASTIC (SOT97)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

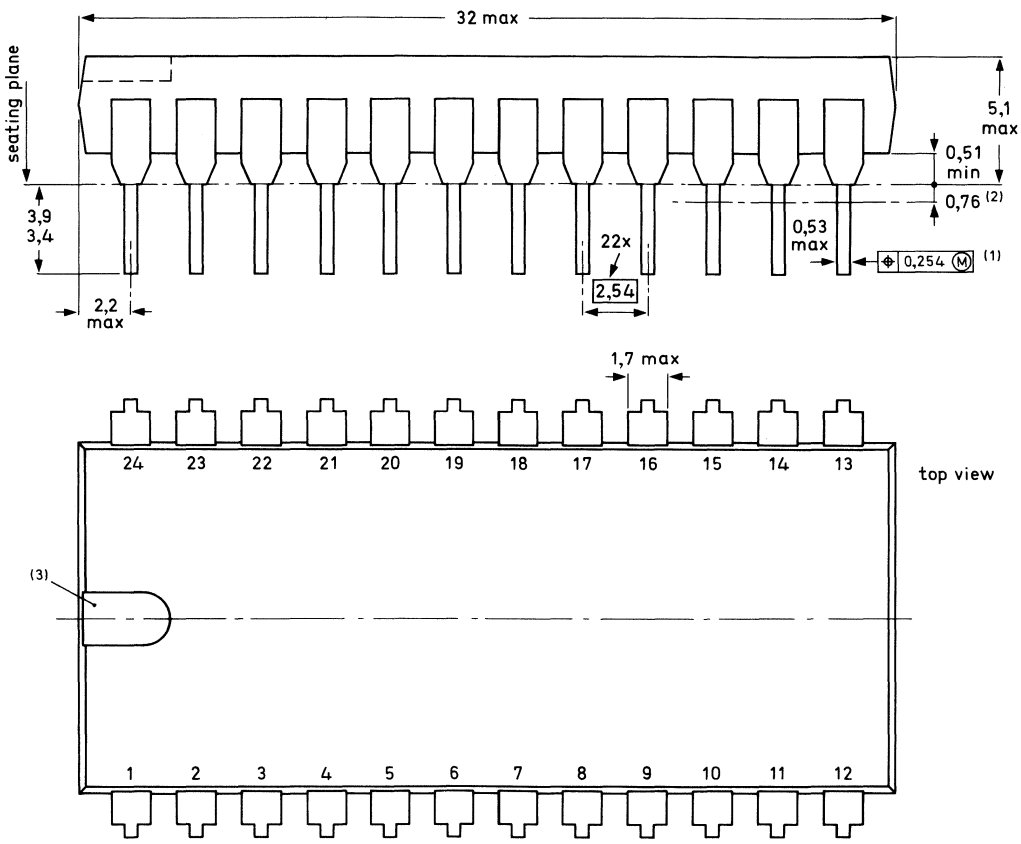
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Only for devices with asymmetrical end-leads.

Dimensions in mm

24-LEAD DUAL IN-LINE; PLASTIC (SOT101A, B, F, G, L)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

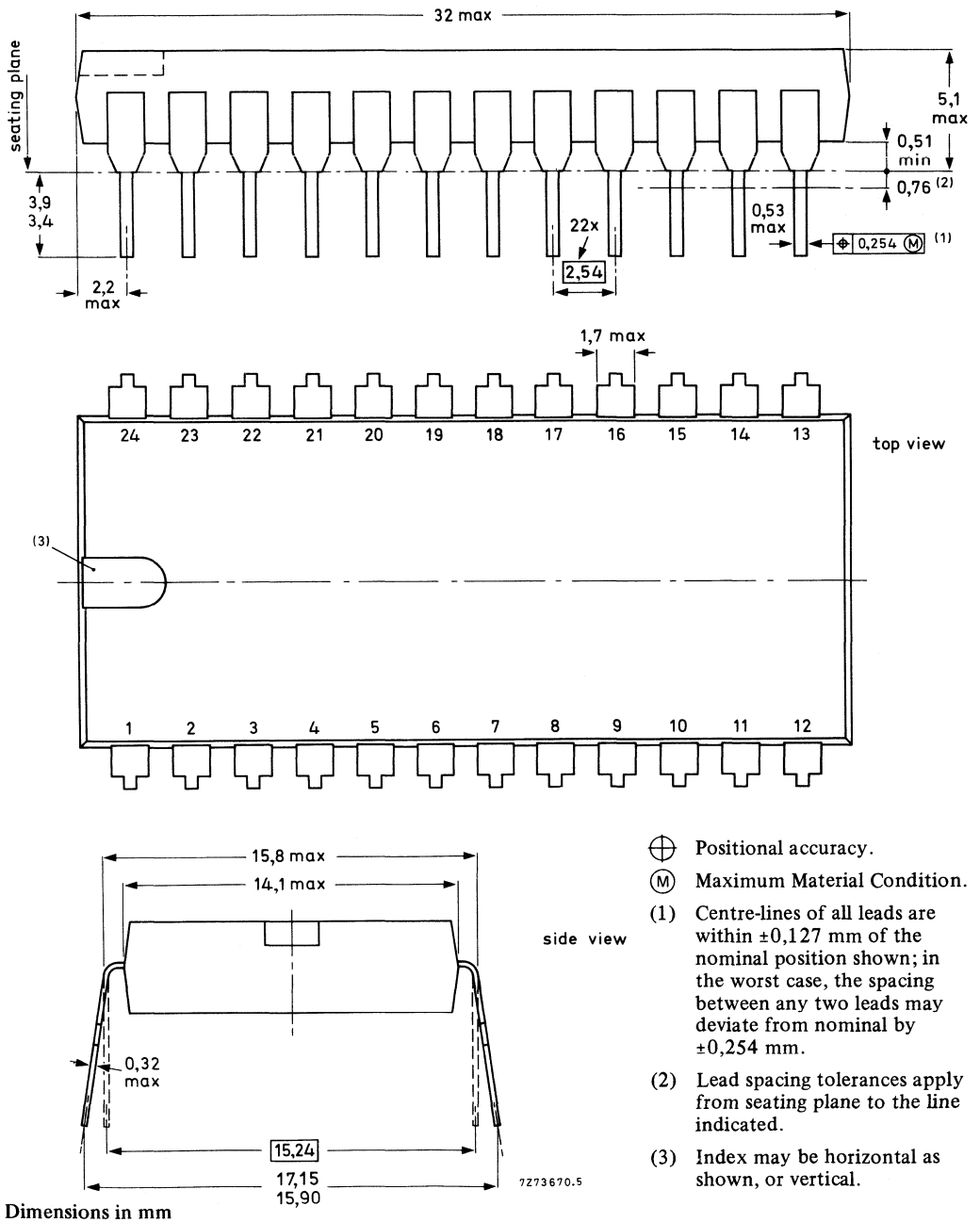
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

24-LEAD DUAL IN-LINE; PLASTIC WITH INTERNAL HEAT SPREADER (SOT101A, B, F, G, L)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

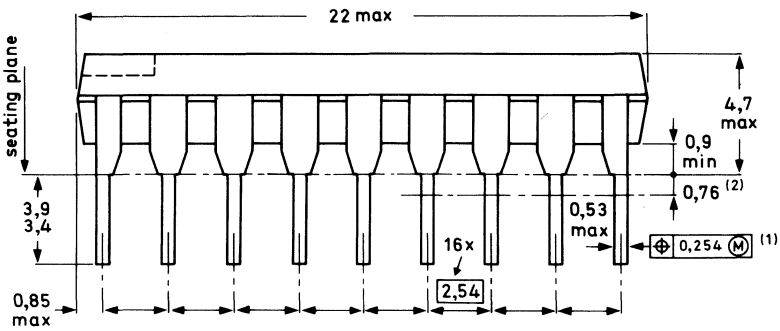
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

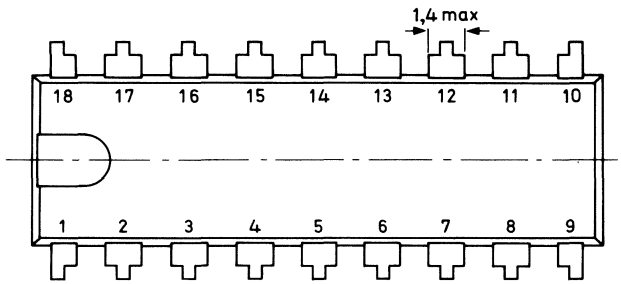
(2) Lead spacing tolerances apply from seating plane to the line indicated.

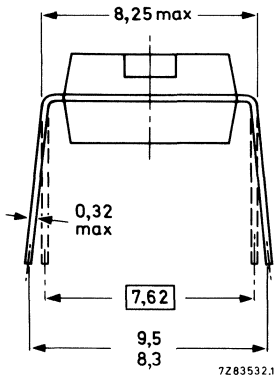
(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

18-LEAD DUAL IN-LINE; PLASTIC (SOT102[1])







⊕ Positional accuracy.

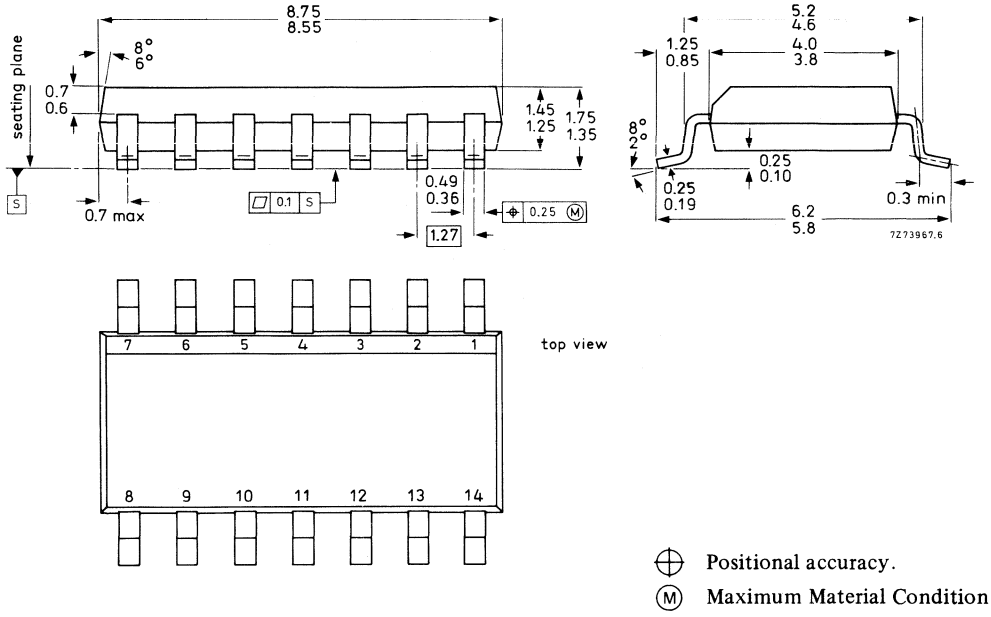
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

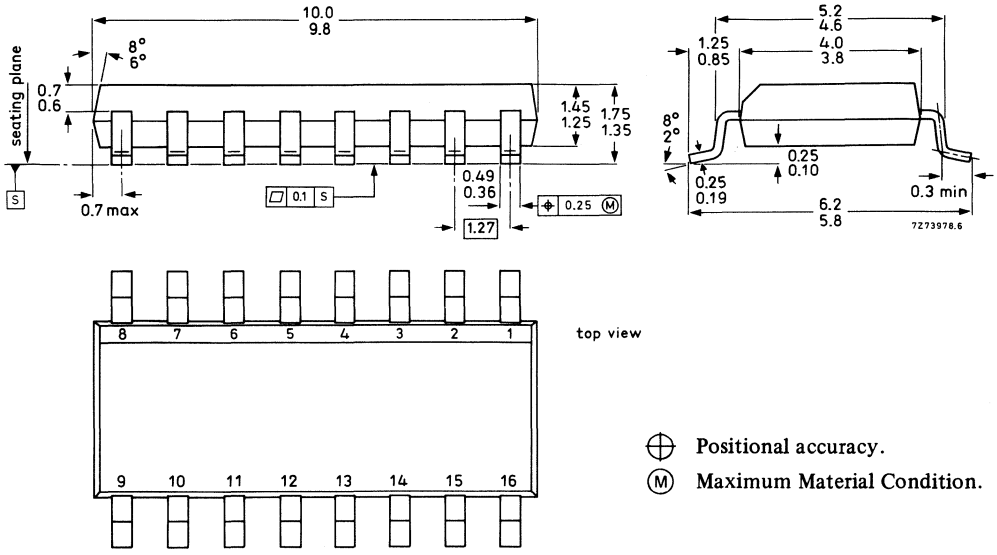
Dimensions in mm

14-LEAD MINI-PACK; PLASTIC (SO14; SOT108A)



Dimension in mm

16-LEAD MINI-PACK; PLASTIC (SO16; SOT109A)

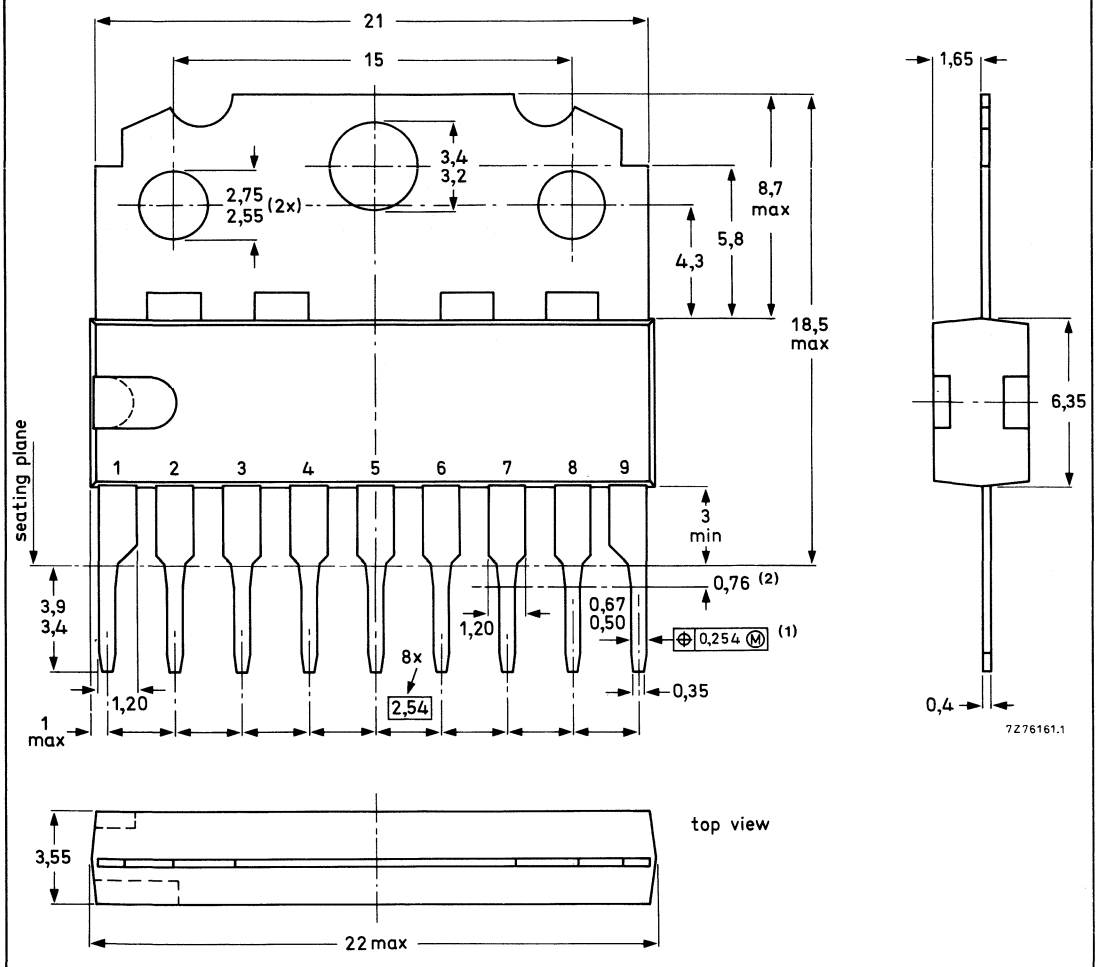


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

9-LEAD SINGLE IN-LINE; PLASTIC (SOT110B)



⊕ Positional accuracy.

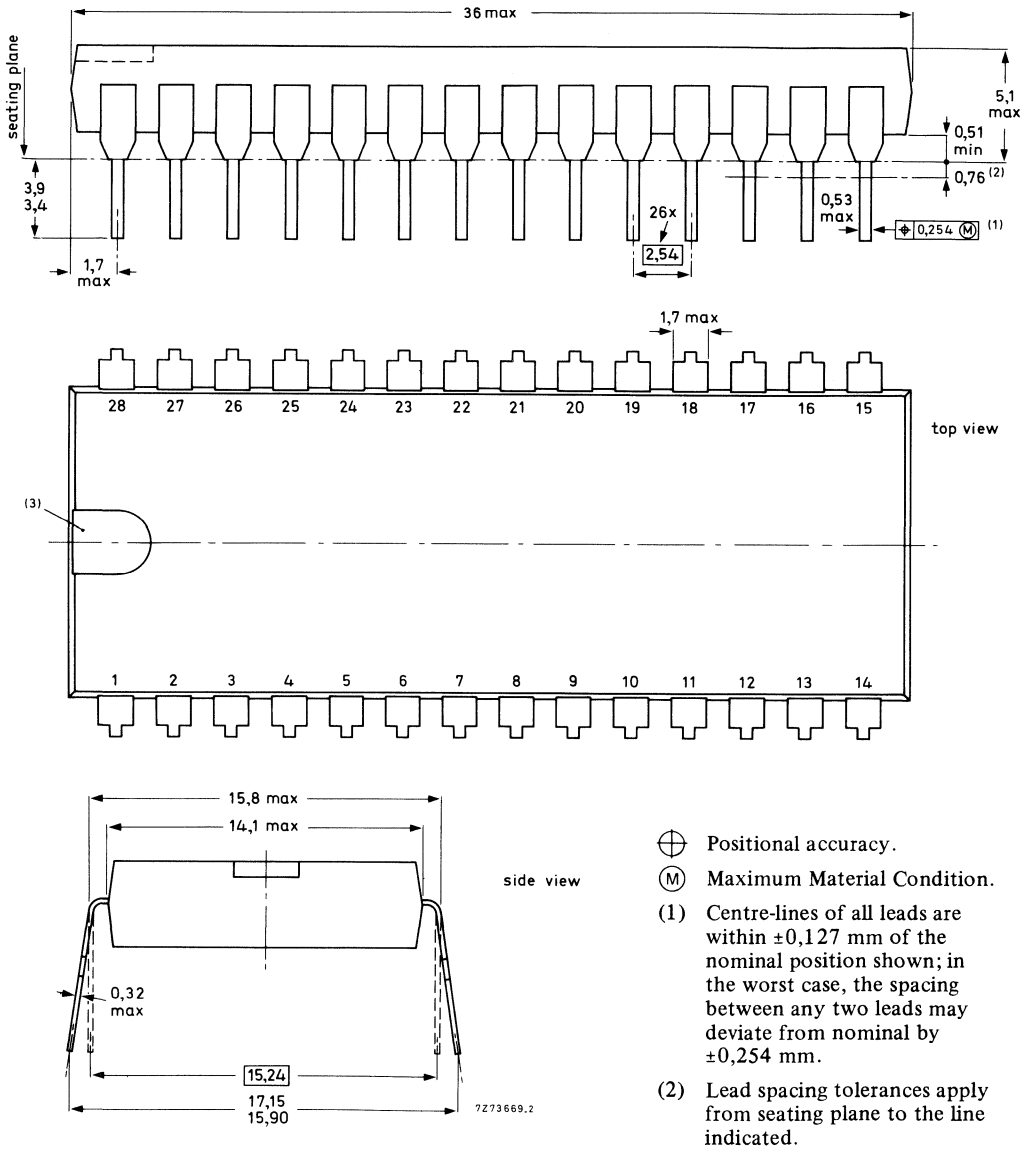
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

28-LEAD DUAL IN-LINE; PLASTIC (SOT117)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

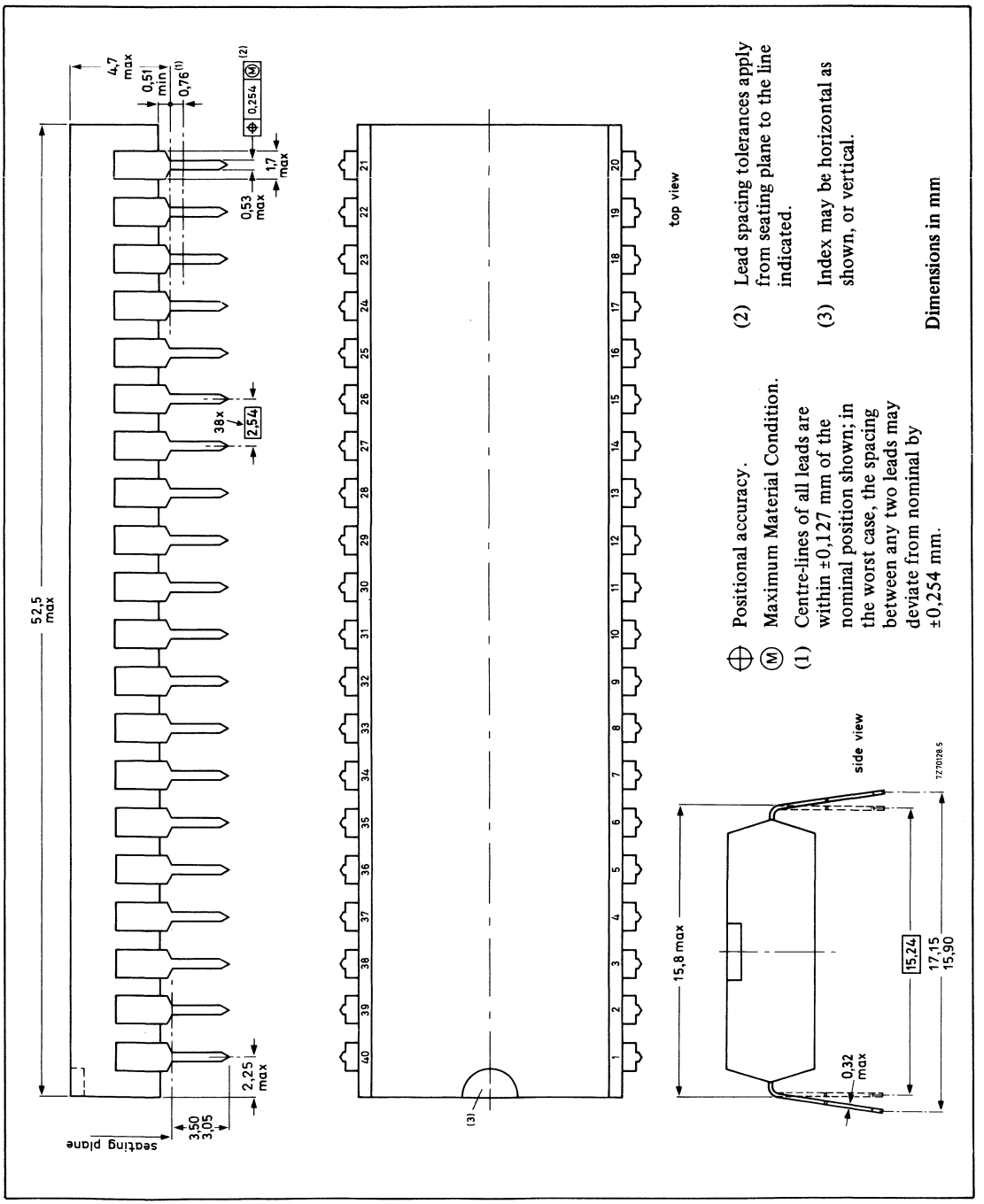
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

40-LEAD DUAL IN-LINE; PLASTIC (SOT129)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

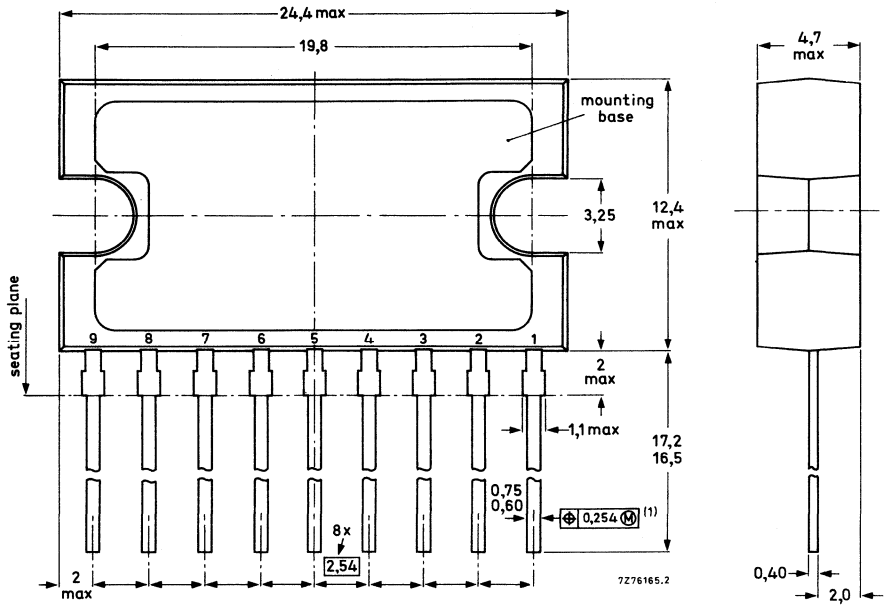
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

9-LEAD SINGLE IN-LINE; PLASTIC POWER (SOT131)



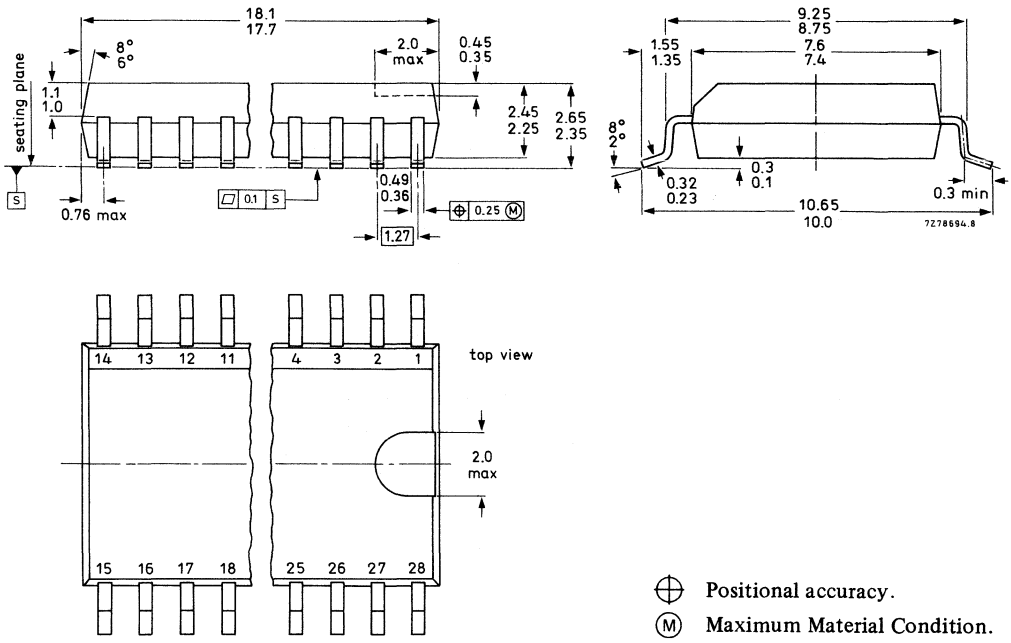
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

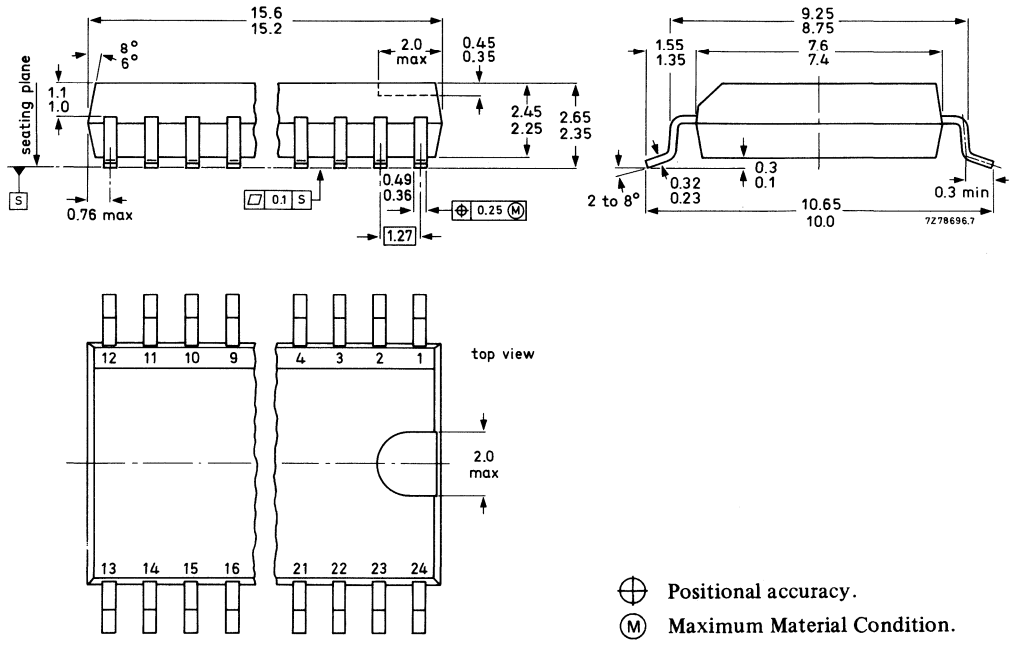
Dimensions in mm

28-LEAD MINI-PACK; PLASTIC (SO28; SOT136A)



Dimensions in mm

24-LEAD MINI-PACK; PLASTIC (SO24; SOT137A)

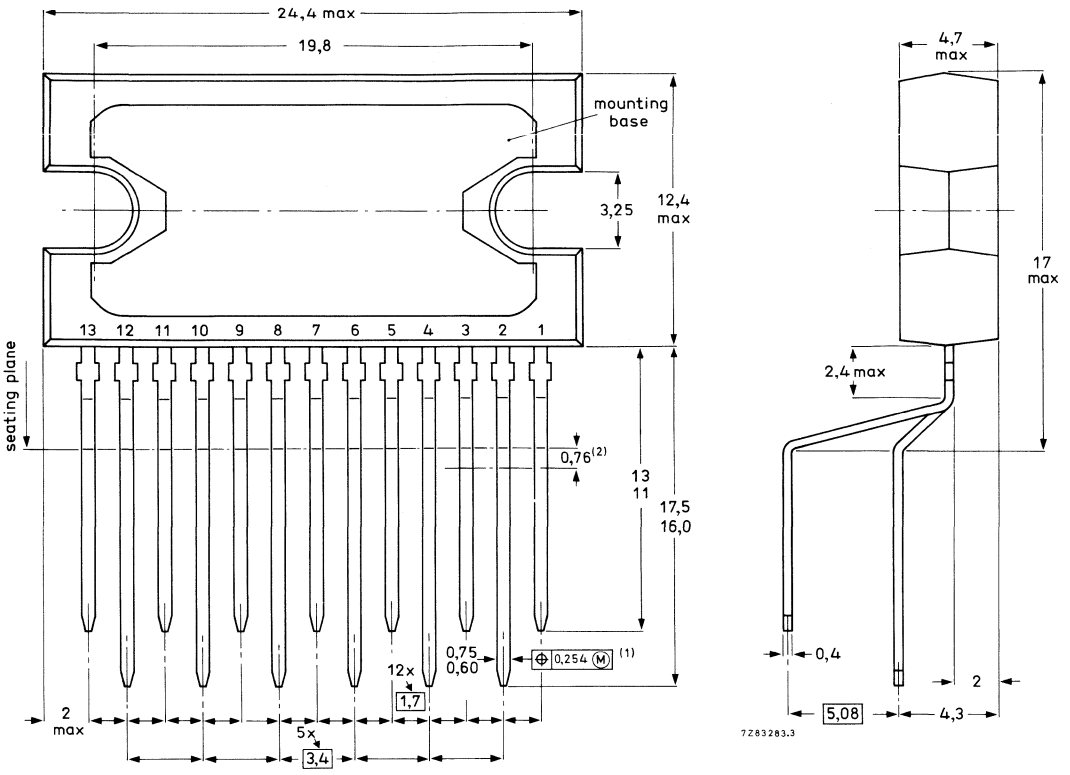


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

13-LEAD SIL-BENT-TO-DIL; PLASTIC POWER (SOT141B,C)



⊕ Positional accuracy.

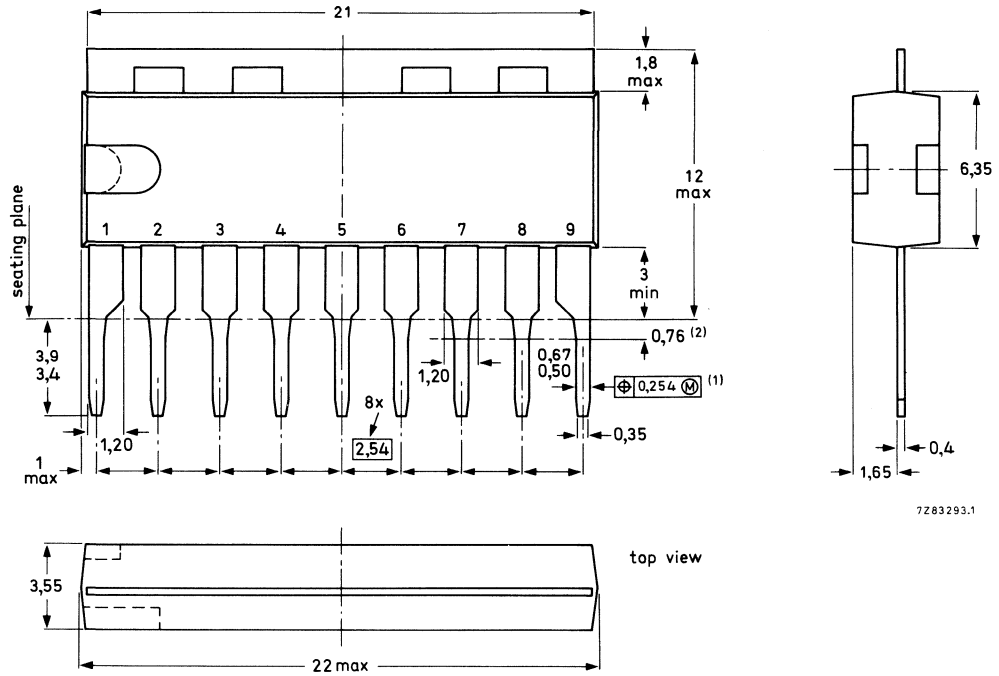
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

9-LEAD SINGLE IN-LINE; PLASTIC (SOT142)



⊕ Positional accuracy.

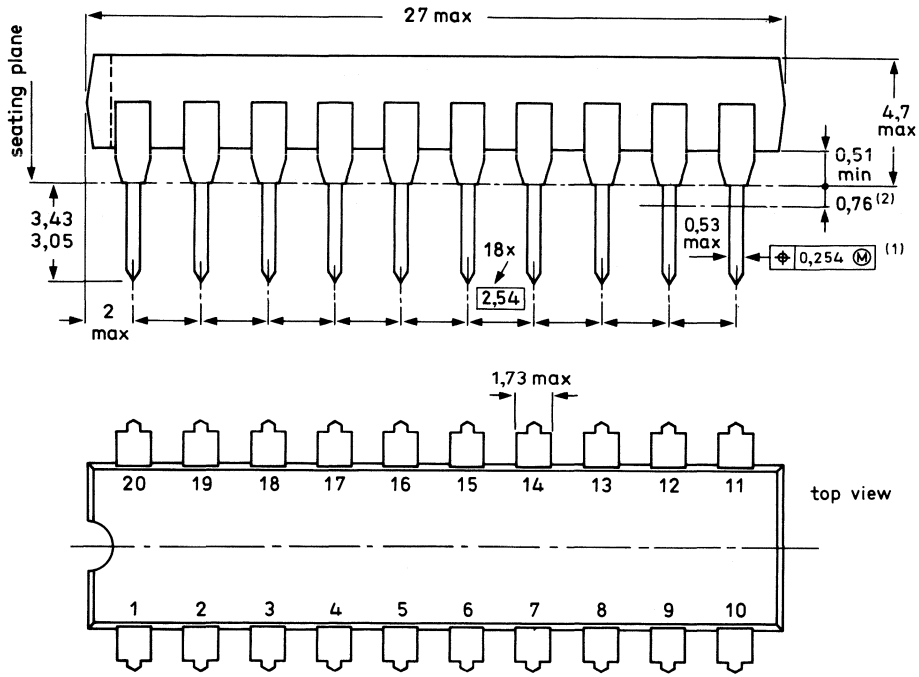
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

20-LEAD DUAL IN-LINE; PLASTIC (SOT146)



⊕ Positional accuracy.

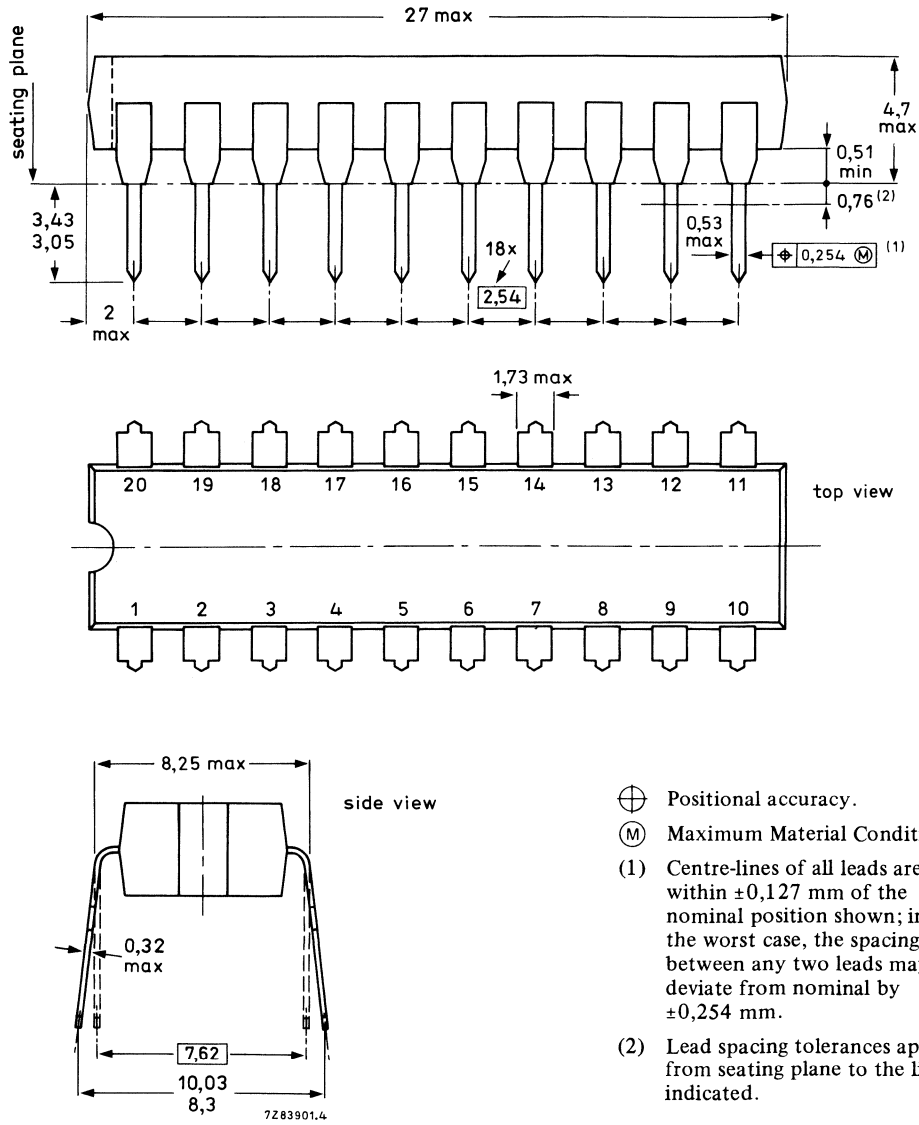
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

20-LEAD DUAL IN-LINE; PLASTIC WITH INTERNAL HEAT SPREADER (SOT146EE7)



⊕ Positional accuracy.

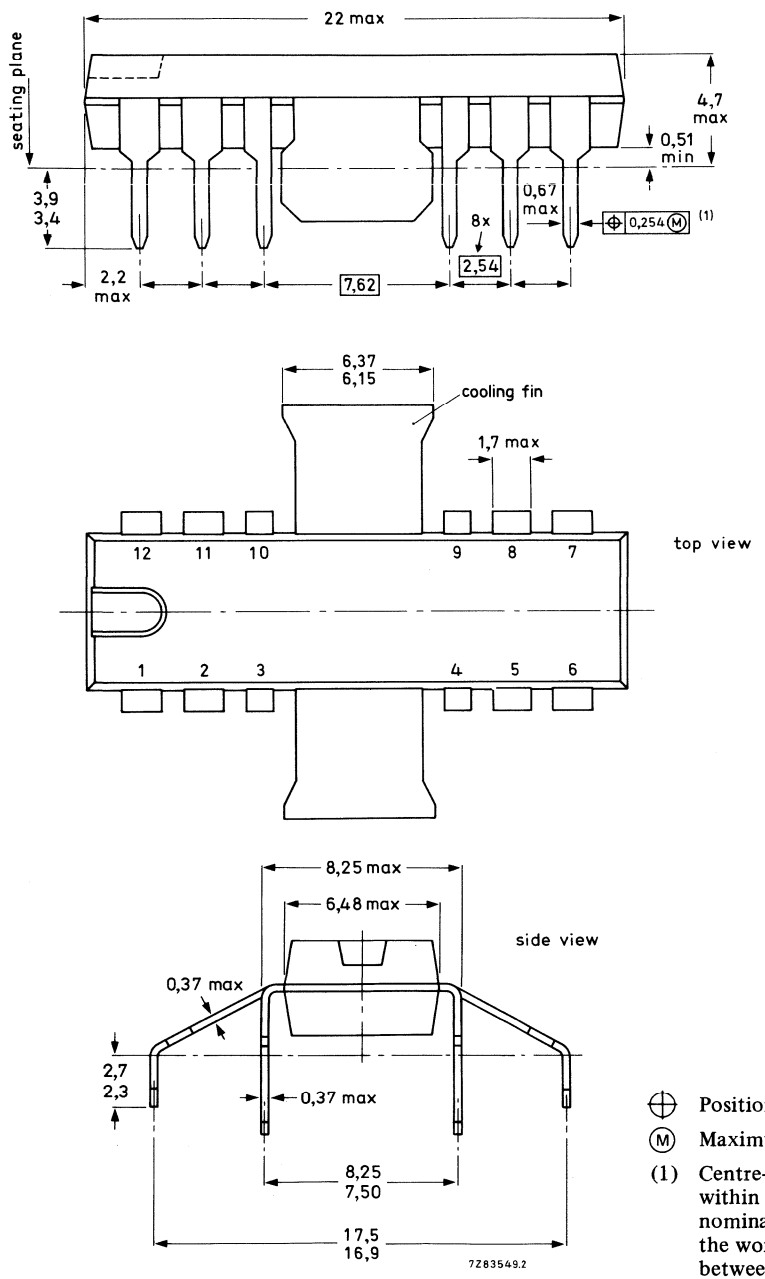
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

12-LEAD DUAL IN-LINE; PLASTIC WITH METAL COOLING FIN (SOT150)



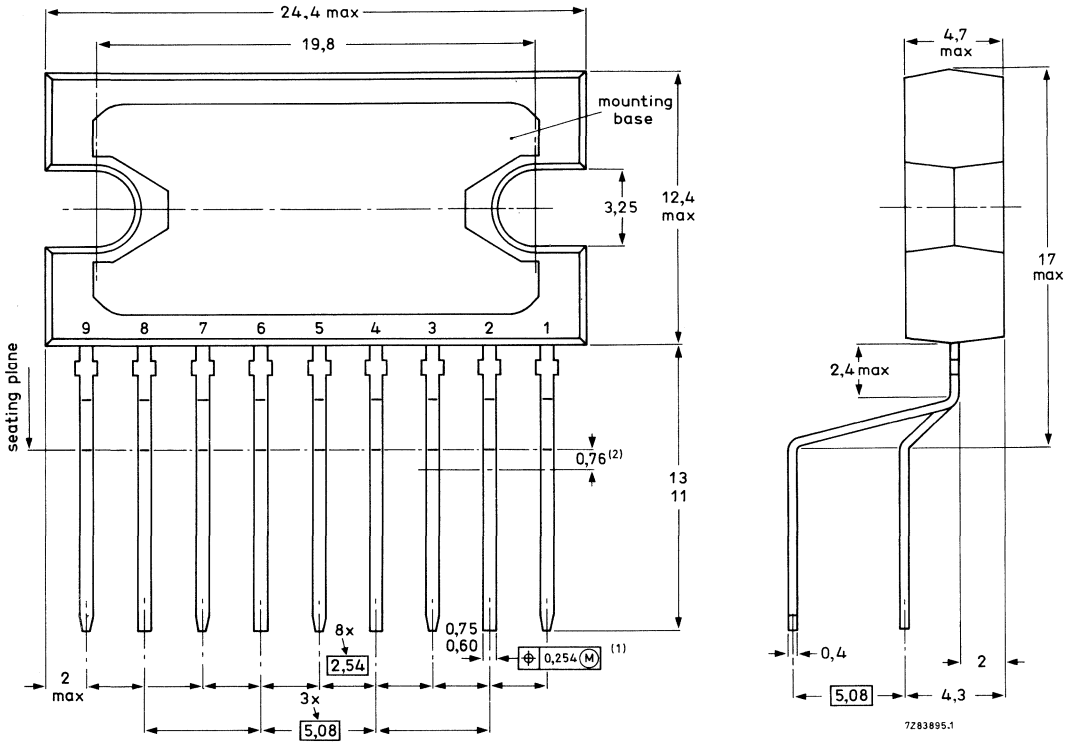
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

Dimensions in mm

9-LEAD SIL-BENT-TO-DIL; PLASTIC POWER (SOT157)



⊕ Positional accuracy.

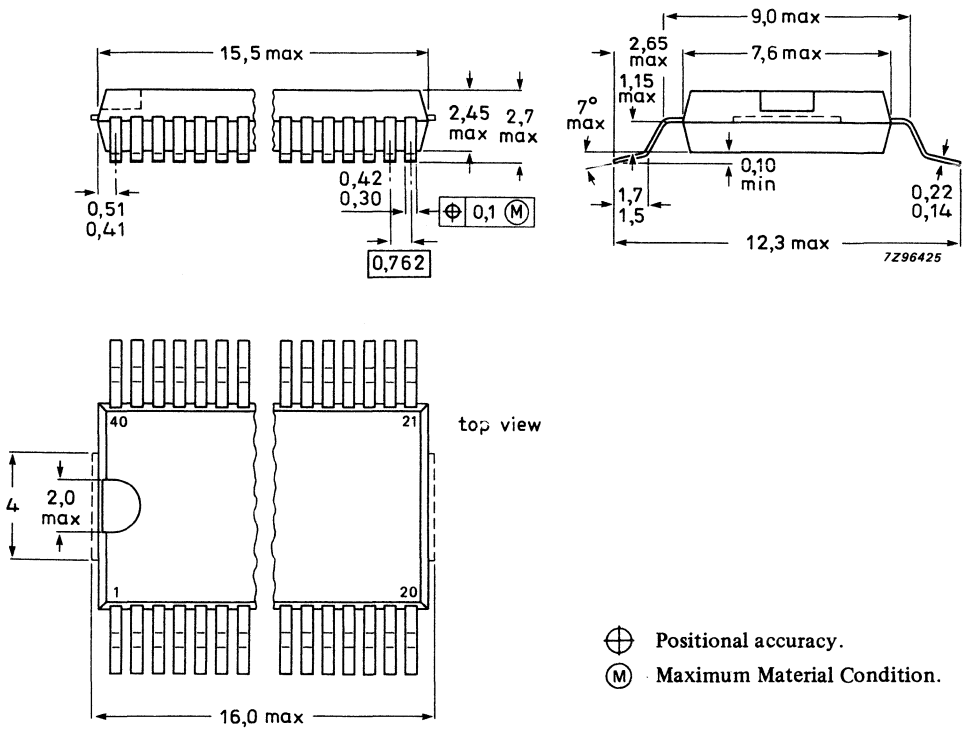
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

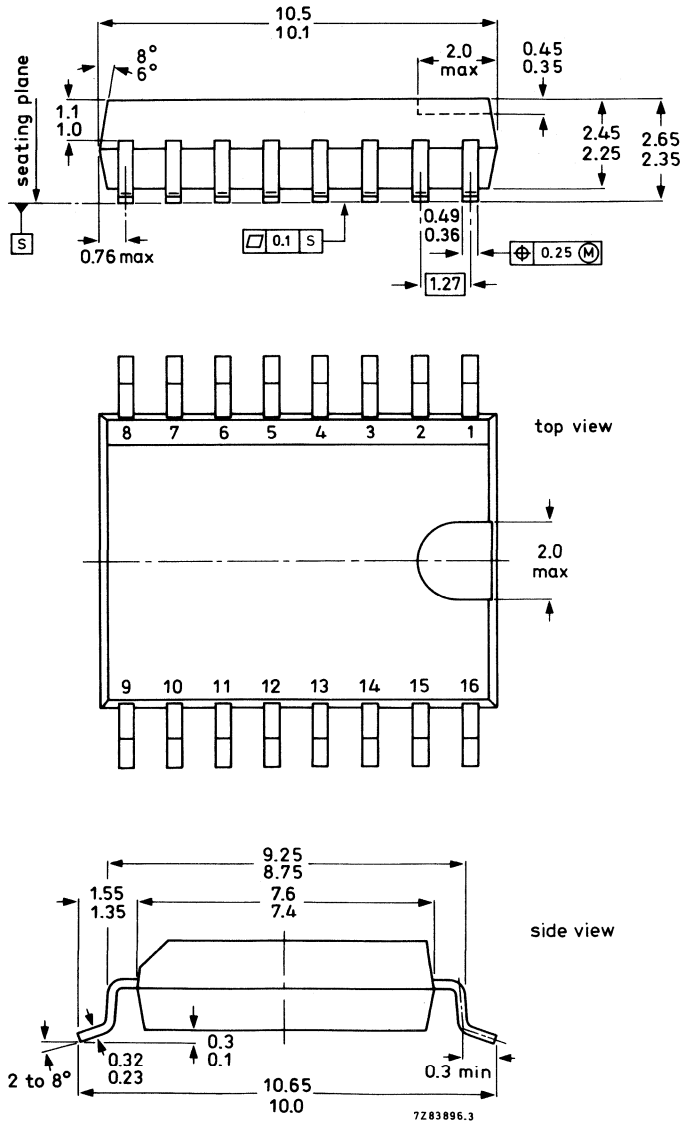
Dimensions in mm

40-LEAD MINI-PACK; PLASTIC (VSO40; SOT158A)



Dimensions in mm

16-LEAD MINI-PACK; PLASTIC (SO16L; SOT162A)

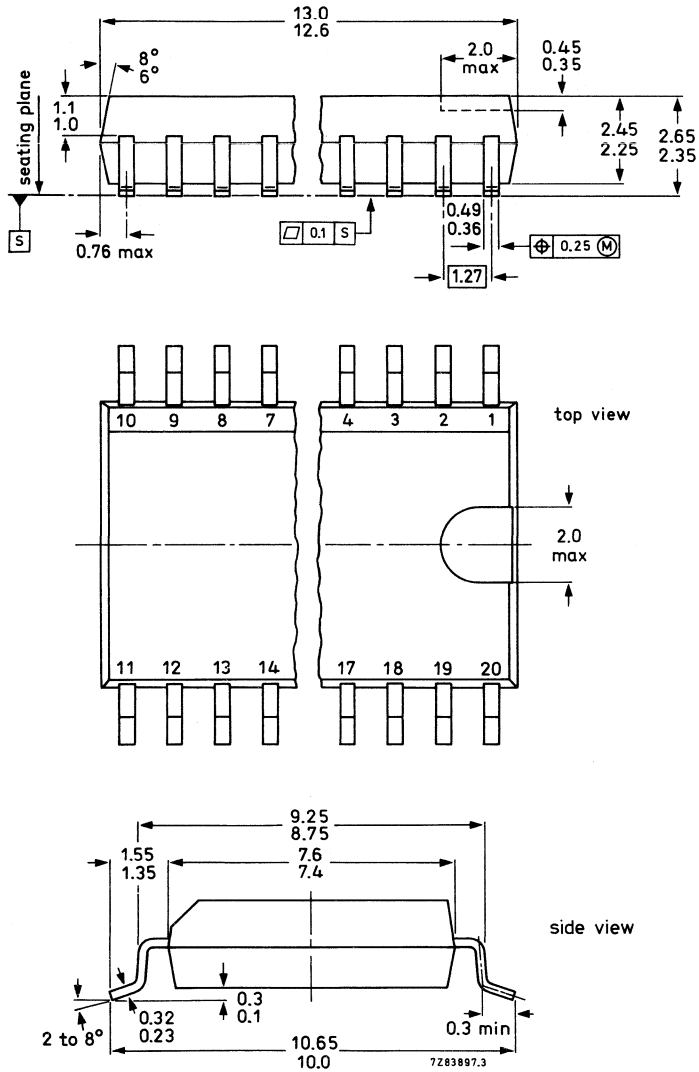


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

20-LEAD MINI-PACK; PLASTIC (SO20; SOT163A)

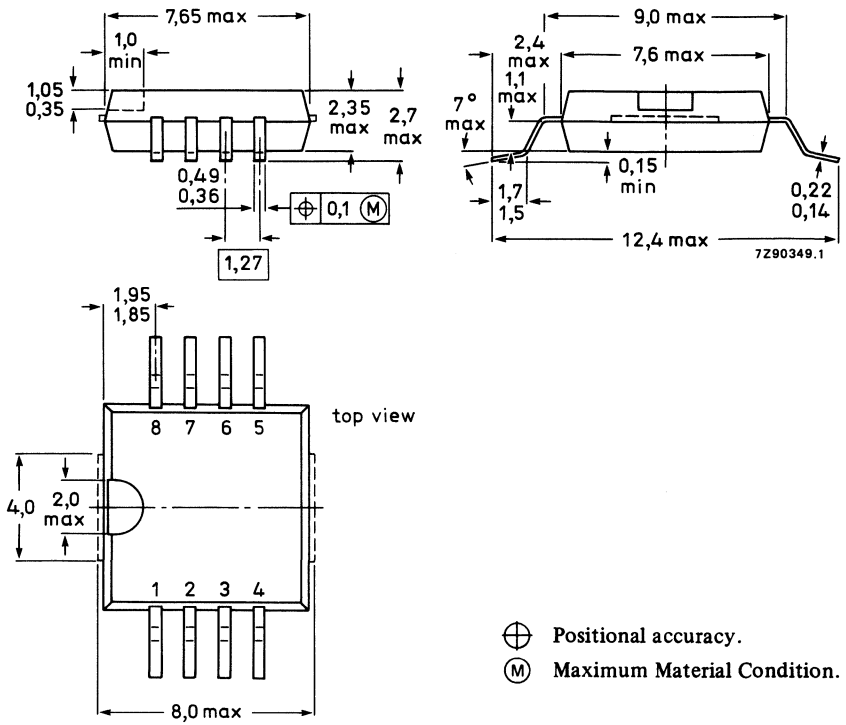


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

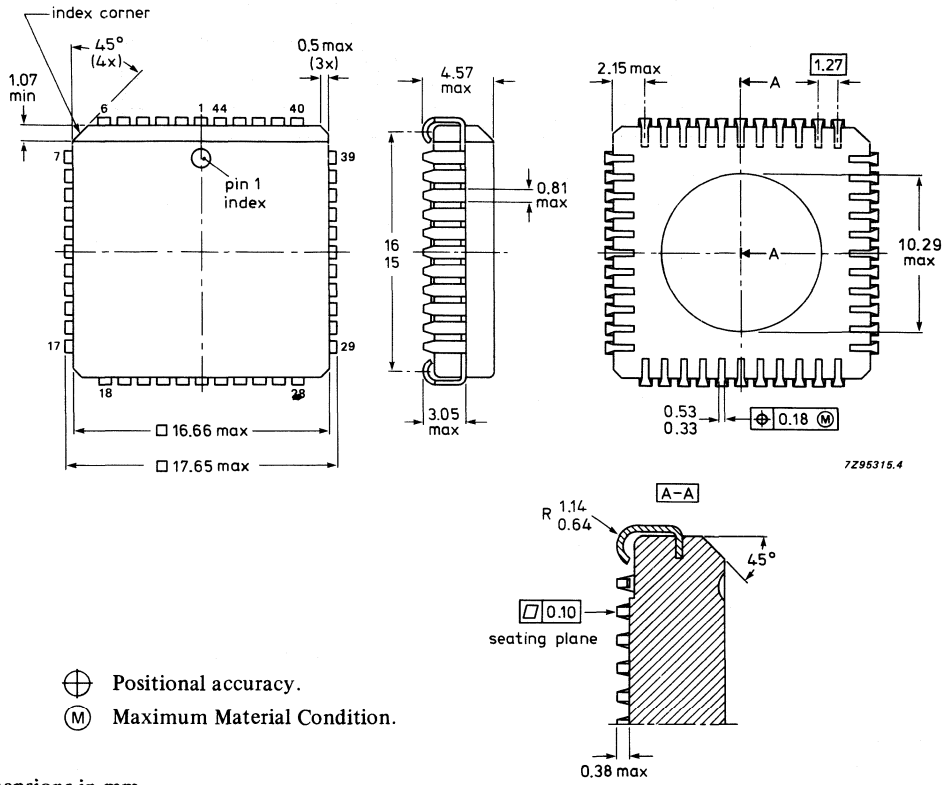
Dimensions in mm

8-LEAD MINI-PACK; PLASTIC (SO8L; SOT176A)



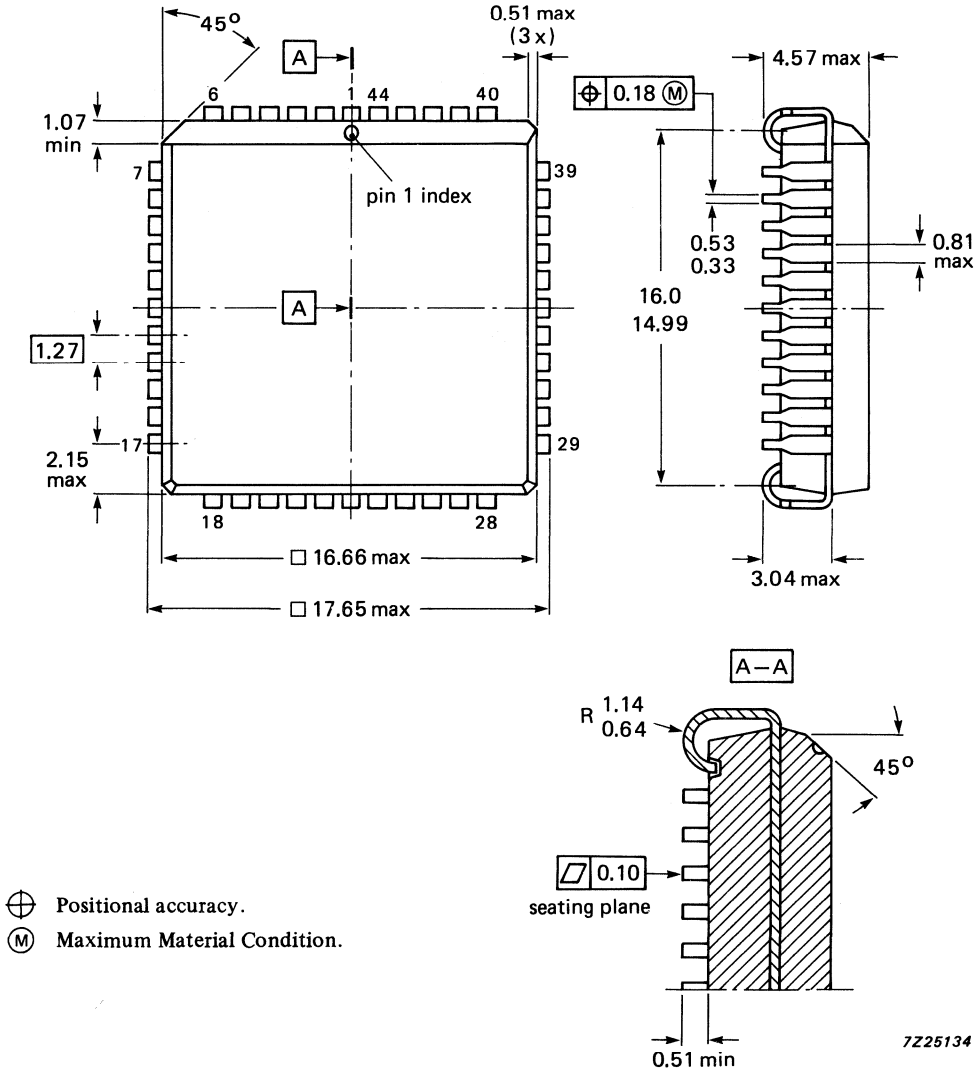
Dimensions in mm

44-LEAD PLASTIC LEADED CHIP CARRIER (PLCC); 'PEDESTAL' VERSION (SOT187)



Dimensions in mm

44-LEAD PLASTIC LEADED CHIP CARRIER (PLCC); 'POCKET' VERSION (SOT187AA)

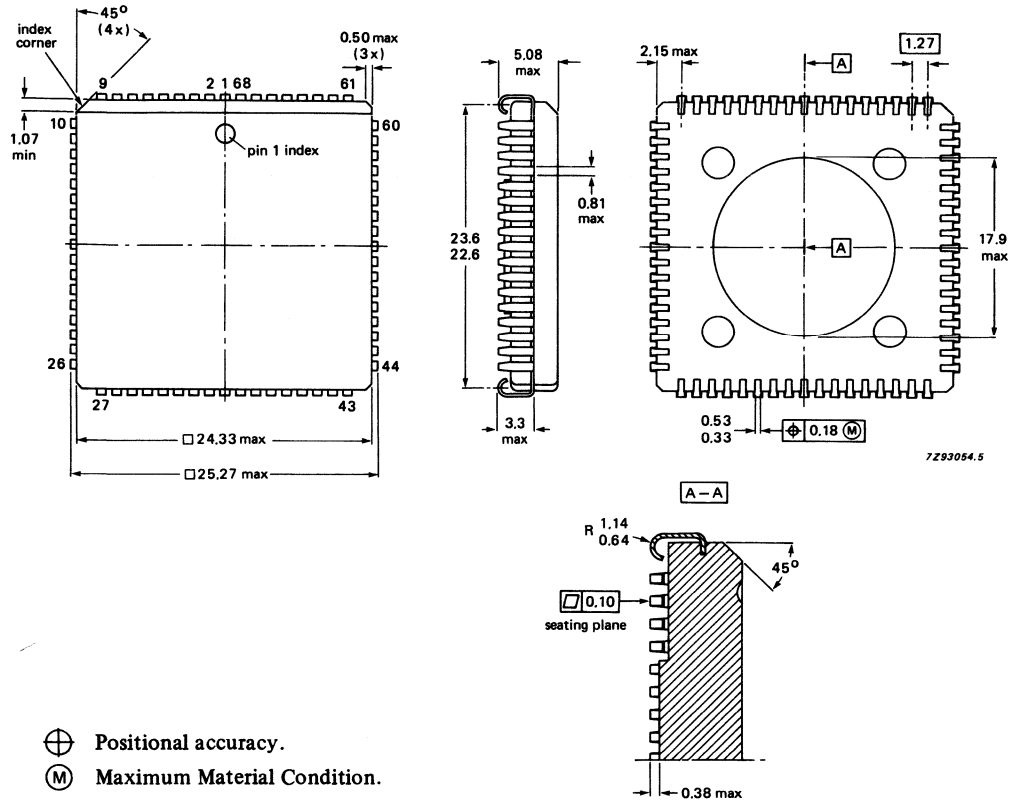


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

68-LEAD PLASTIC LEADED CHIP CARRIER (PLCC); 'PEDESTAL' VERSION (SOT188)

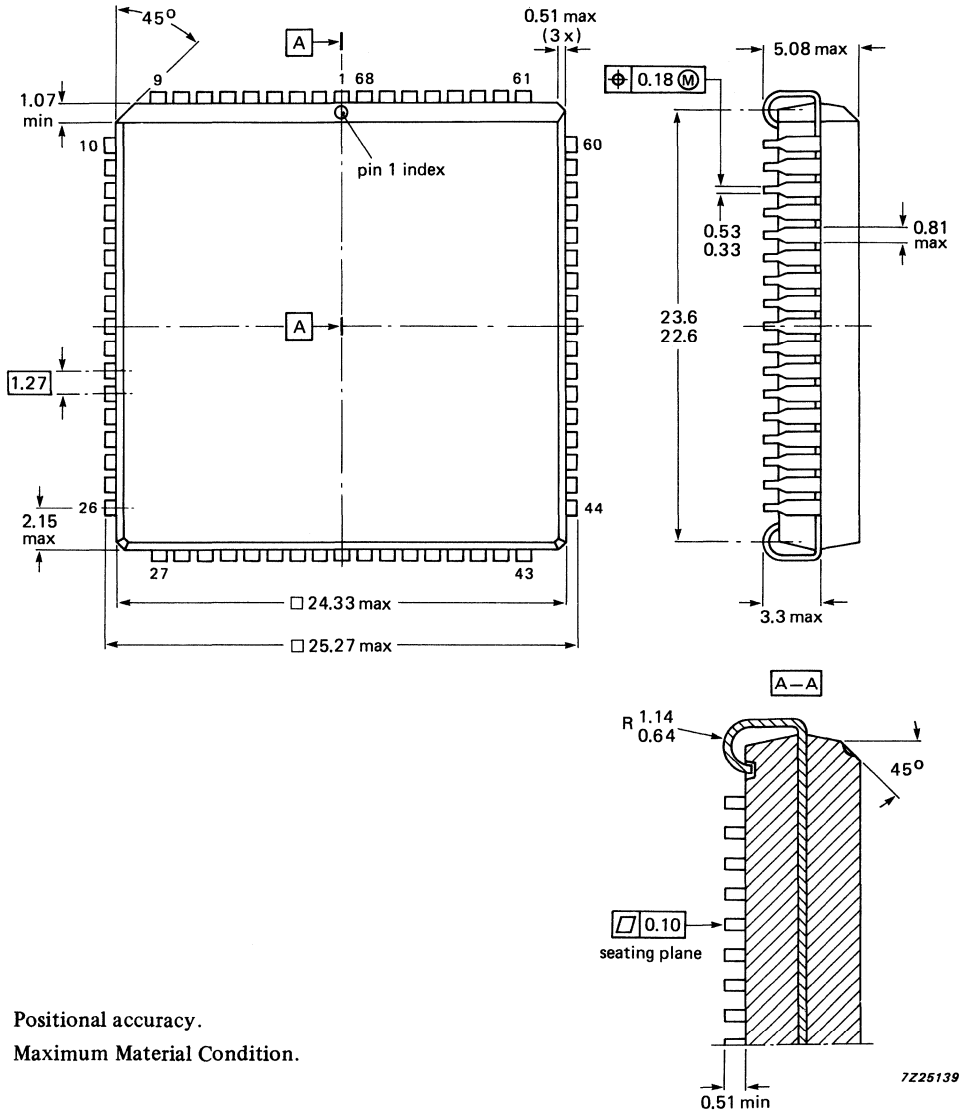


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

68-LEAD PLASTIC LEADED CHIP CARRIER (PLCC); 'POCKET' VERSION (SOT188AA)

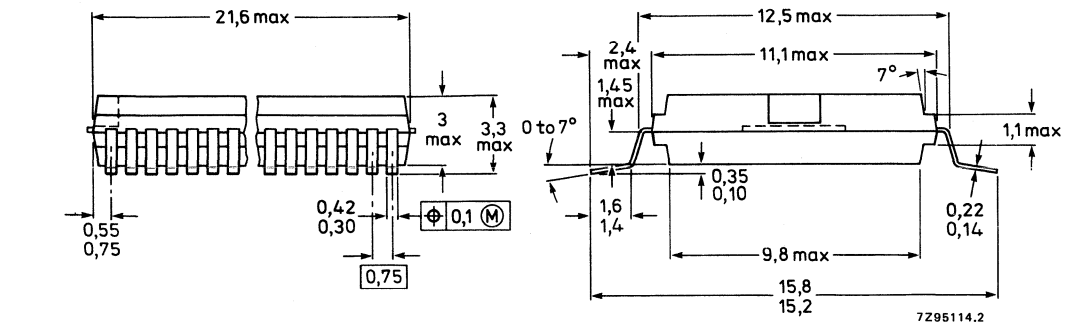


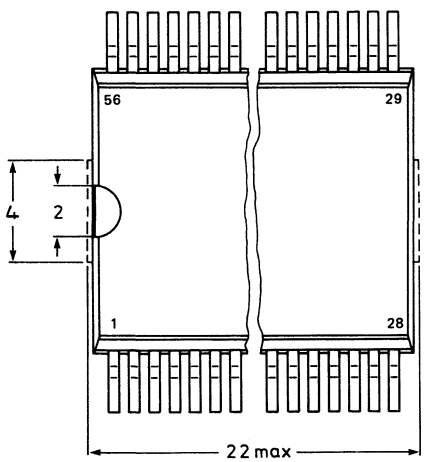
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

56-LEAD MINI-PACK; PLASTIC (VSO56; SOT190)





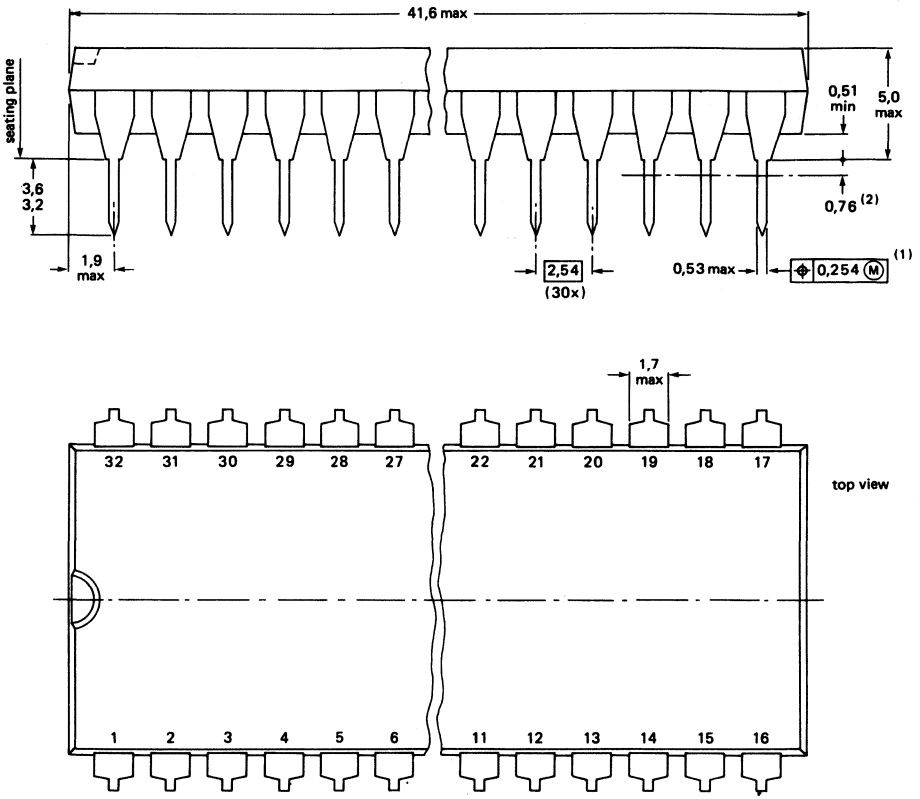
top view

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

32-LEAD DUAL IN-LINE; PLASTIC WITH INTERNAL HEAT SPREADER (SOT201)



⊕ Positional accuracy.

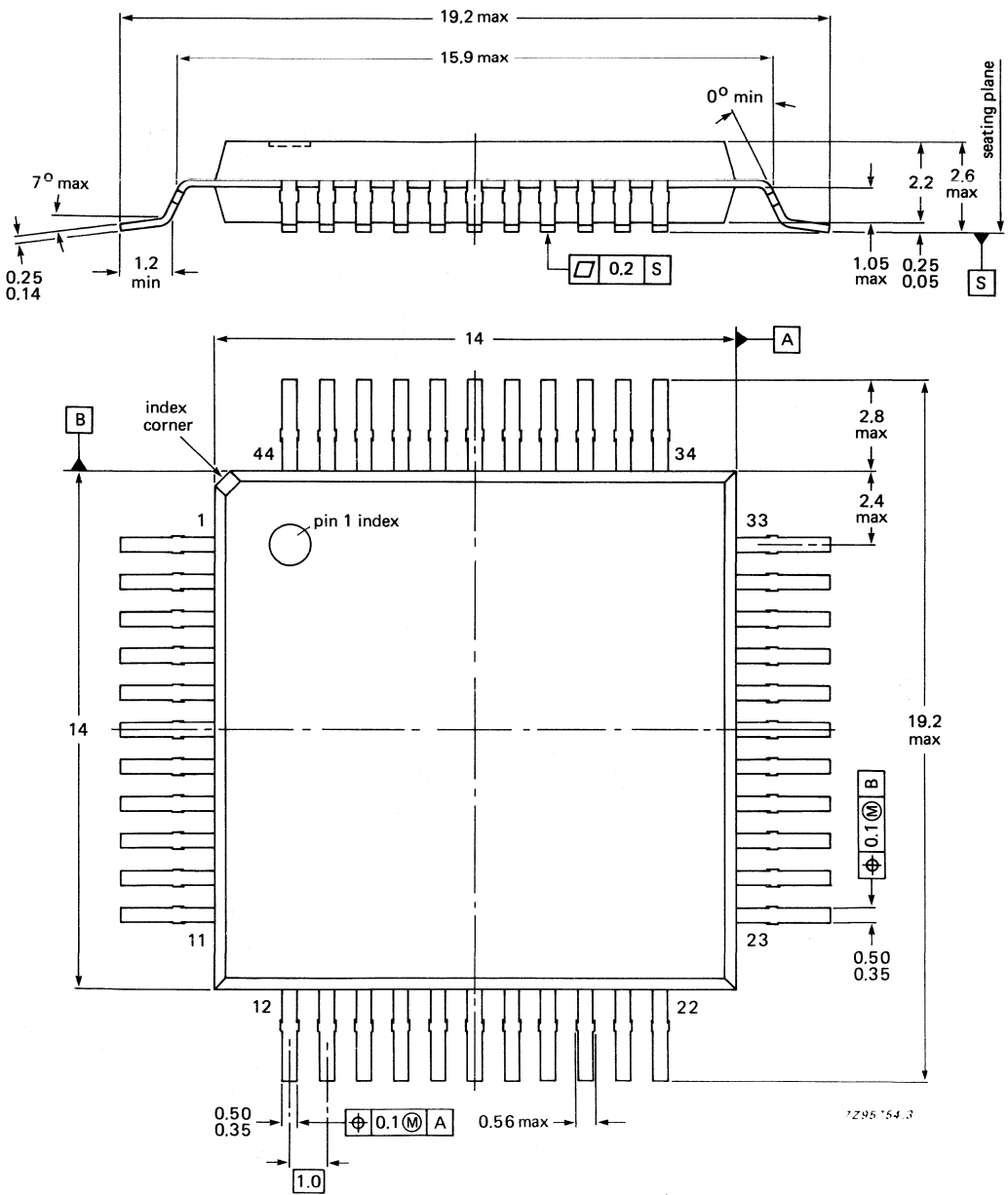
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

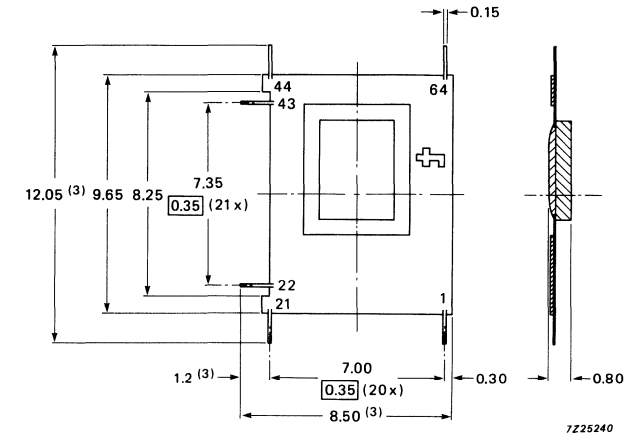
Dimensions in mm

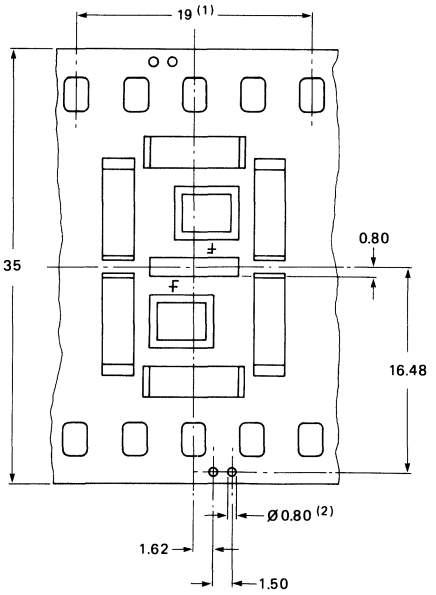
44-LEAD QUAD FLAT-PACK; PLASTIC (SOT205A)

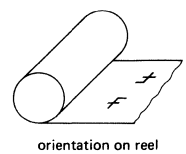


Dimensions in mm

64-LEAD TAPE-AUTOMATED-BONDING (TAB) MODULE (SOT267A,C,D)







(1) 1 pattern = 4 perforation pitch intervals (contains two modules)
(2) Circuit-test holes
(3) Fixed by the user

Dimensions in mm

SOLDERING

SOLDERING PLASTIC MINI-PACKS

1. By hand-held soldering iron or pulse-heated solder tool

Fix the component by first soldering two, diagonally opposite end leads. Apply the heating tool to the flat part of the lead only. Contact time must be limited to 10 seconds at up to 300 °C. When using proper tools, all other leads can be soldered in one operation within 2 to 5 seconds at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages).

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to substrate by dipping or by an extra thick tin/lead plating before package placement.

2. By wave

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 seconds, if allowed to cool to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

3. By solder paste reflow

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing, for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 seconds according to method. Typical reflow temperatures range from 215 to 250 °C.

Pre-heating is necessary to dry paste and evaporate binding agent.

Pre-heating duration: 45 minutes at 45 °C.

4. Repairing soldered joints

The same precaution and limits apply as in (1) above.

SOLDERING PLASTIC DUAL IN-LINE PACKAGES

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

SOLDERING TAB MODULES

1. Fluxing

(a) a flux that does not have to be removed,
or
(b) a water-soluble flux.

2. Soldering

The reflow soldering method using a pulse-heated soldering tool is usually suitable. Limit the soldering operation to 3 seconds at 250 °C at the leads.

3. Cleaning

Avoid cleaning if possible.

If cleaning is necessary, use cold or hot water. A detergent may be added to the water. Finally rinse with de-ionized water.

Do not use ultrasonic cleaning methods as these may damage the inner or outer leads.

Do not use solvents.

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DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of six series of handbooks:

INTEGRATED CIRCUITS

DISCRETE SEMICONDUCTORS

DISPLAY COMPONENTS

PASSIVE COMPONENTS*

PROFESSIONAL COMPONENTS**

MATERIALS*

The contents of each series are listed on pages iii to viii.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

When ratings or specifications differ from those published in the preceding edition they are indicated with arrows in the page margin. Where application is given it is advisory and does not form part of the product specification.

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Product specialists are at your service and enquiries will be answered promptly.

* Will replace the Components and materials (green) series of handbooks.
** Will replace the Electron tubes (blue) series of handbooks.

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This series of handbooks comprises:

code	handbook title
IC01	**Radio, audio and associated systems** Bipolar, MOS
IC02a/b	**Video and associated systems** Bipolar, MOS
IC03	**ICs for Telecom** Bipolar, MOS Subscriber sets, Cordless Telephones
IC04	**HE4000B logic family** CMOS
IC05	**Advanced Low-power Schottky (ALS) Logic Series**
IC06	**High-speed CMOS; PC74HC/HCT/HCU** Logic family
IC07	**Advanced CMOS logic (ACL)**
IC08	**ECL 10K and 100K logic families**
IC09N	**TTL logic series**
IC10	**Memories** MOS, TTL, ECL
IC11	**Linear Products**
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IC13	**Semi-custom** Programmable Logic Devices (PLD)
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Supplement to IC15	**FAST TTL logic series**
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current code	new code	handbook title
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S2b	**SC03***	**Thyristors and triacs**
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S4a	**SC05**	**Low-frequency power transistors and hybrid IC power modules**
S4b	**SC06**	**High-voltage and switching power transistors**
S5	**SC07**	**Small-signal field-effect transistors**
S6	**SC08** **SC09**	**RF power transistors** **RF power modules**
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S8a	**SC11***	**Light emitting diodes**
S8b	**SC12**	**Optocouplers**
S9	**SC13***	**PowerMOS transistors**
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S15**	**SC16**	**Laser diodes**
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S14	**SC18***	**Liquid crystal displays and driver ICs for LCDs**

* Not yet issued with the new code in this series of handbooks.
** New handbook in this series; will be issued shortly.

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C3	**DC04***	**Loudspeakers**
C20	**DC05***	**Wire-wound components for TVs and monitors**

* These handbooks are currently issued in another series; they are not yet issued in the Display Components series of handbooks.

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C11	**PA02**	**Varistors, thermistors and sensors**
C12	**PA03**	**Potentiometers and switches**
C7	**PA04***	**Variable capacitors**
C22	**PA05***	**Film capacitors**
C15	**PA06***	**Ceramic capacitors**
C9	**PA07***	**Piezoelectric quartz devices**
C13	**PA08***	**Fixed resistors**

* Not yet issued with the new code in this series of handbooks.

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T2a	*	**Transmitting tubes for communications, glass types**
T2b	*	**Transmitting tubes for communications, ceramic types**
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T4	*	**Magnetrons for microwave heating**
T5	**PC02****	**Cathode-ray tubes**
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T9	**PC04****	**Photo and electron multipliers**
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T12	**PC07**	**Vidicon and Newvicon camera tubes and deflection units**
T13	**PC08**	**Image intensifiers**
T15	**PC09****	**Dry reed switches**
C8	**PC10**	**Variable mains transformers; annular fixed transformers**
	PC11	**Solid state image sensors and peripheral integrated circuits**

* These handbooks will not be reissued.
** Not yet issued with the new code in this series of handbooks.

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C4, C5	MA01*	**Soft Ferrites**
C16	MA02**	**Permanent magnet materials**
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* Handbooks C4 and C5 will be reissued as one handbook having the new code MA01.

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